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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u67jbd100e

7.2 Pin description

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
RESET/PIO0_0	3	4	8 [8]	I; PU	I	**RESET —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
					IO	**PIO0_0 —** General-purpose digital input/output pin.
PIO0_1	4	5	9 [6]	I; PU	IO	**PIO0_1 —** General-purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration.
					O	**CLKOUT —** Clockout pin.
					O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					O	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal.
PIO0_2	11	14	19 [6]	I; PU	IO	**PIO0_2 —** General-purpose port 0 input/output 2.
					IO	**SSP0_SSEL —** Slave select for SSP0.
					I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
					-	**R_0 —** Reserved.
PIO0_3	14	19	30 [6]	I; PU	IO	**PIO0_3 —** General-purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. A HIGH level during reset starts the USB device enumeration.
					I	**USB_VBUS —** Monitors the presence of USB bus power.
					-	**R_1 —** Reserved.
PIO0_4	15	20	31 [7]	IA	IO	**PIO0_4 —** General-purpose port 0 input/output 4 (open-drain).
					IO	**I2C0_SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
					-	**R_2 —** Reserved.
PIO0_5	16	21	32 [7]	IA	IO	**PIO0_5 —** General-purpose port 0 input/output 5 (open-drain).
					IO	**I2C0_SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
					-	**R_3 —** Reserved.

8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 50 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 AHB multilayer matrix

The AHB multilayer matrix supports three masters, the M0+ core, the DMA, and the USB. All masters can access all slaves (peripherals and memories).

- Digital filter with programmable filter constant on all pins. The minimum filter constant is 1/50 MHz = 20 ns.

8.9.2 Standard I/O pad configuration

Figure 9 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input digital filter selectable on all pins. In addition, a 10 ns digital glitch filter is selectable on pins with analog function.
- Analog input

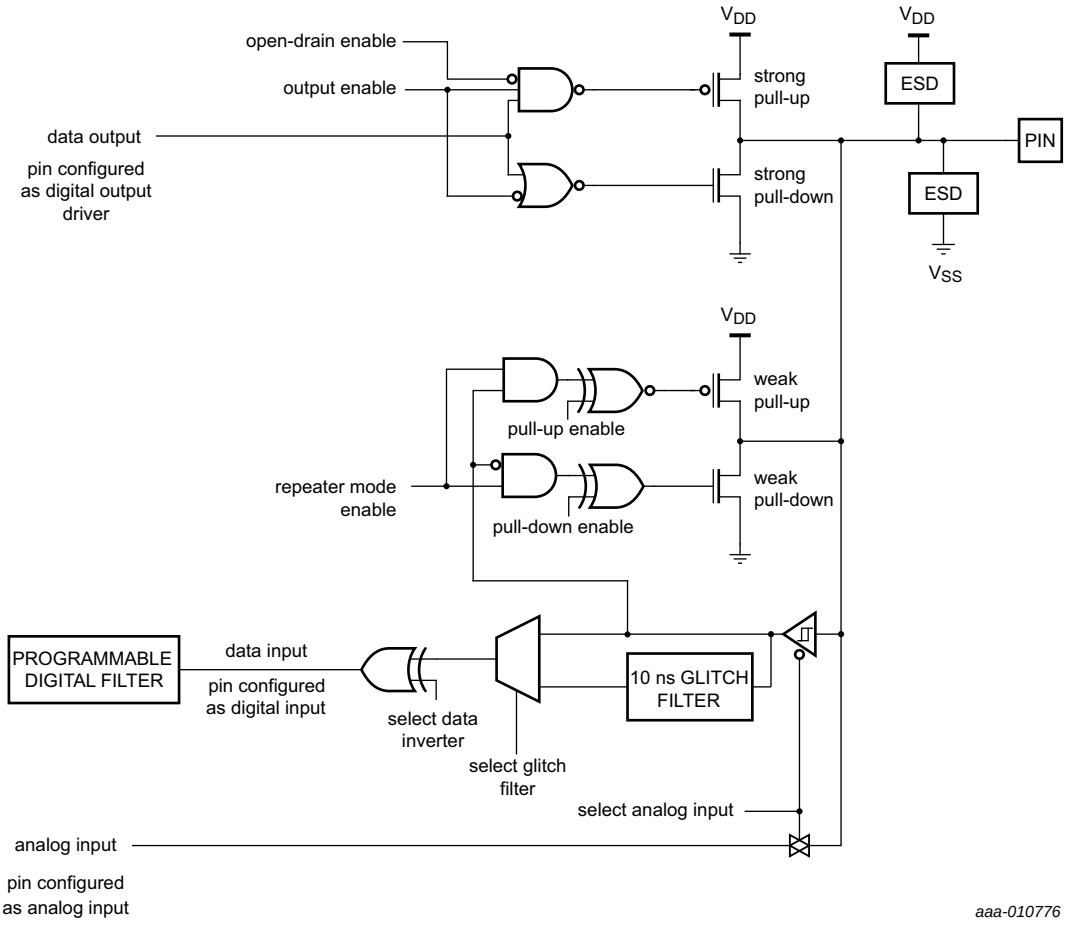


Fig 9. Standard I/O pin configuration

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

8.14 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The USB interface consists of a full-speed device controller with on-chip PHY (PHYsical layer) for device functions.

Remark: Configure the part in default power mode with the power profiles before using the USB (see Section 8.25.7.1 “Power profiles”). Do not use the USB when the part runs in performance, efficiency, or low-power mode.

8.14.1 Full-speed USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

8.14.1.1 Features

- Dedicated USB PLL available.
- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 10 physical (5 logical) endpoints including one control endpoint.
- Single and double buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from Deep-sleep mode and Power-down mode on USB activity and remote wake-up.
- Supports SoftConnect functionality through internal pull-up resistor.
- Internal 33 Ω series termination resistors on USB_DP and USB_DM lines eliminate the need for external series resistors.
- Supports Link Power Management (LPM).
- Supports XTAL-less low-speed mode using the 1% accurate IRC as the clock source for the USB PLL. For board connection changes in low-speed mode, see Section 14.3.1 “USB Low-speed operation”.

8.15 USART0

Remark: The LPC11U6x contains two distinctive types of UART interfaces: USART0 is software-compatible with the USART interface on the LPC11U1x/LPC11U2x/LPC11U3x parts. USART1 to USART4 use a different register interface.

The USART0 includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART0 uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

8.19.2 General purpose external event counter/timers (CT32B0/1 and CT16B0/1)

The LPC11U6x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.19.2.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- PWM output function.
- Match outputs and capture inputs serve as hardware triggers for ADC conversions.

8.20 System tick timer (SysTick)

The ARM Cortex-M0+ includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

8.21 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

8.21.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

8.25.2 Power domains

The LPC11U6x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power (V_{DD}) is used to operate the RTC whenever V_{DD} is present. Therefore, there is no power drain from the RTC battery when V_{DD} is available and $V_{DD} \geq$ VBAT + 0.3 V.

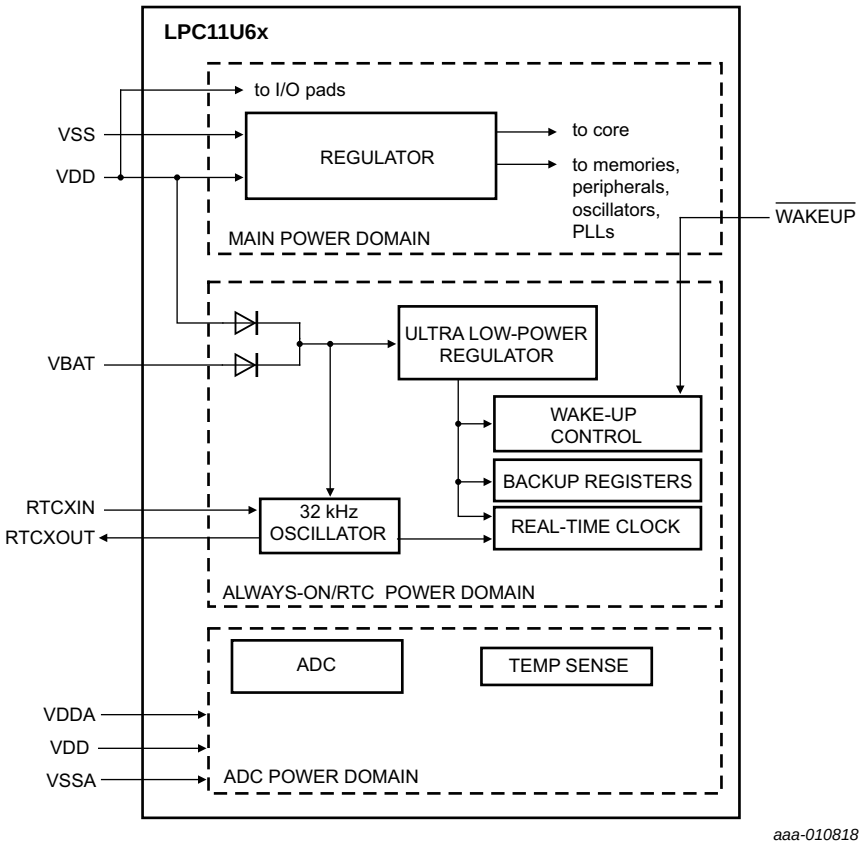


Fig 11. Power distribution

8.25.3 Integrated oscillators

The LPC11U6x include the following independent oscillators: the system oscillator, the Internal RC oscillator (IRC), the watchdog oscillator, and the 32 kHz RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC11U6x operates from the internal RC oscillator until software switches to a different clock source. The IRC allows the system to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 10 for an overview of the LPC11U6x clock generation.

8.25.6 Wake-up process

The LPC11U6x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

8.25.7 Power control

The LPC11U6x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.25.7.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11U6x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

Remark: When using the USB, configure the LPC11U6x in Default mode.

8.25.7.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	$V_{DD} \geq 2.4$ V; 5 V tolerant pins [14] [15]	0	-	5	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage		0.05 V_{DD}	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V;	4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [16]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$ [16]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.4 V ≤ V_{DD} ≤ 3.6 V	−10	−50	−85	µA
		$V_{DD} < V_I < 5$ V	0	0	0	µA
High-drive output pins configured as digital pin (PIO0_7 and PIO1_31); see Figure 13						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	$V_{DD} \geq 2.4$ V [14] [15]	0	-	5	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage		0.05 V_{DD}	-	-	V

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OLS}	LOW-level short-circuit output current	drive LOW; pad connected to ground	-	-	125	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; pad connected to ground	-	-	125	mA
Oscillator pins						
$V_{i(xtal)}$	crystal input voltage		−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage		−0.5	1.8	1.95	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN [20]	−0.5	-	3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT [20]	−0.5	-	3.6	V
Pin capacitance						
C_{io}	input/output capacitance	pins with analog and digital functions [21]	-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5) [21]	-	-	2.5	pF
		pins with digital functions only [21]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] For USB operation: 3.0 V ≤ V_{DD} ≤ 3.6 V.

[3] T_{amb} = 25 °C.

[4] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[5] IRC enabled; system oscillator disabled; system PLL disabled.

[6] System oscillator enabled; IRC disabled; system PLL disabled.

[7] BOD disabled.

[8] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[9] IRC enabled; system oscillator disabled; system PLL enabled.

[10] IRC disabled; system oscillator enabled; system PLL enabled.

[11] All oscillators and analog blocks turned off.

[12] WAKEUP pin pulled HIGH externally.

[13] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[14] Including voltage on outputs in tri-state mode.

[15] Tri-state outputs go into tri-state mode in Deep power-down mode.

[16] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

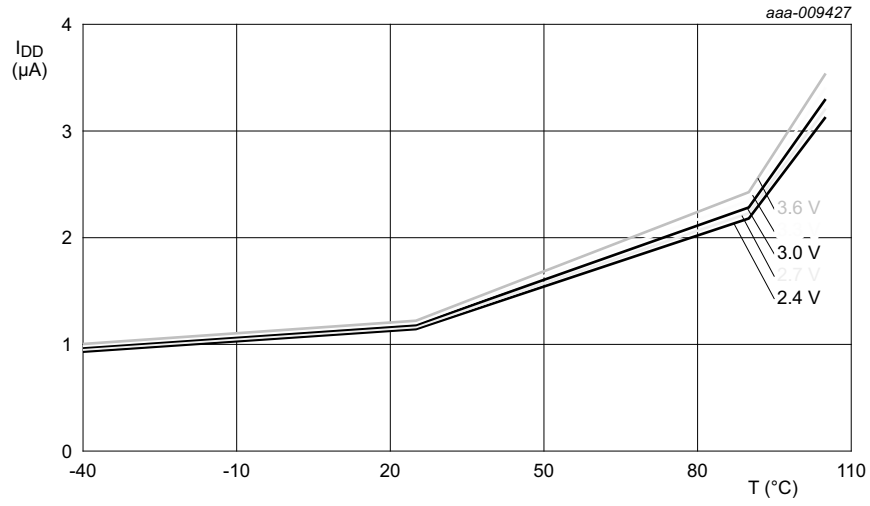
[17] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 13.

[18] To V_{SS}.

[19] The parameter values specified are simulated and absolute values.

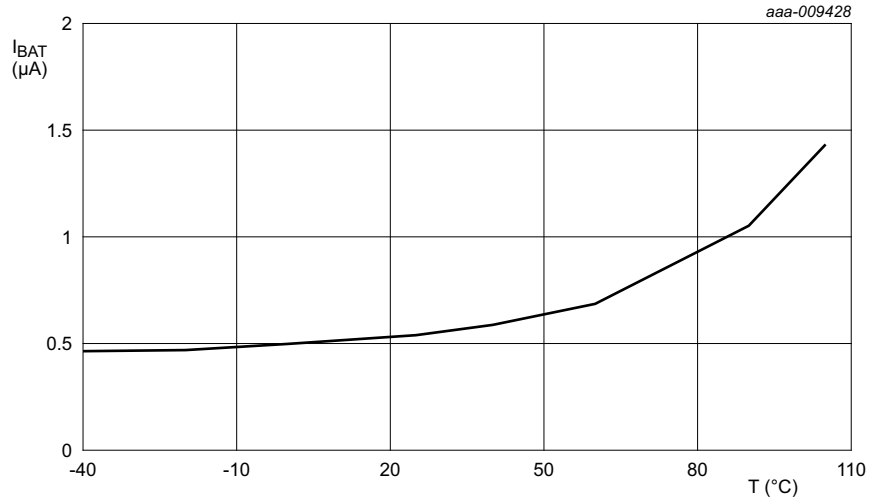
[20] The input voltage of the RTC oscillator is limited as follows: $V_{i(rtcx)}$, $V_{o(rtcx)}$ < max(VBAT, V_{DD}).

[21] Including bonding pad capacitance.



Conditions: RTC running; VBAT = 0 V

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: RTC not running; V_{BAT} = 3.0 V; V_{DD} floating.

Fig 20. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature

12. Dynamic characteristics

12.1 Flash/EEPROM memory

Table 10. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	[1]	10000	100000	-	cycles
t_{ret}	retention time	powered	10	20	-	years
		unpowered	20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors	95	100	105	ms
t_{prog}	programming time	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes to the flash. T_{amb} <= +85 °C. Flash programming with IAP calls (see LPC11U6x *user manual*).

Table 11. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance		100000	1000000	-	cycles
t_{ret}	retention time	powered	100	200	-	years
		unpowered	150	300	-	years
t_{prog}	programming time	64 bytes	-	2.9	-	ms

12.2 External clock for the oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.95 V (see Table 8). For connecting the oscillator to the XTAL pins, also see Section 14.4.

Table 12. Dynamic characteristic: external clock (XTALIN input)

T_{amb} = −40 °C to +105 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

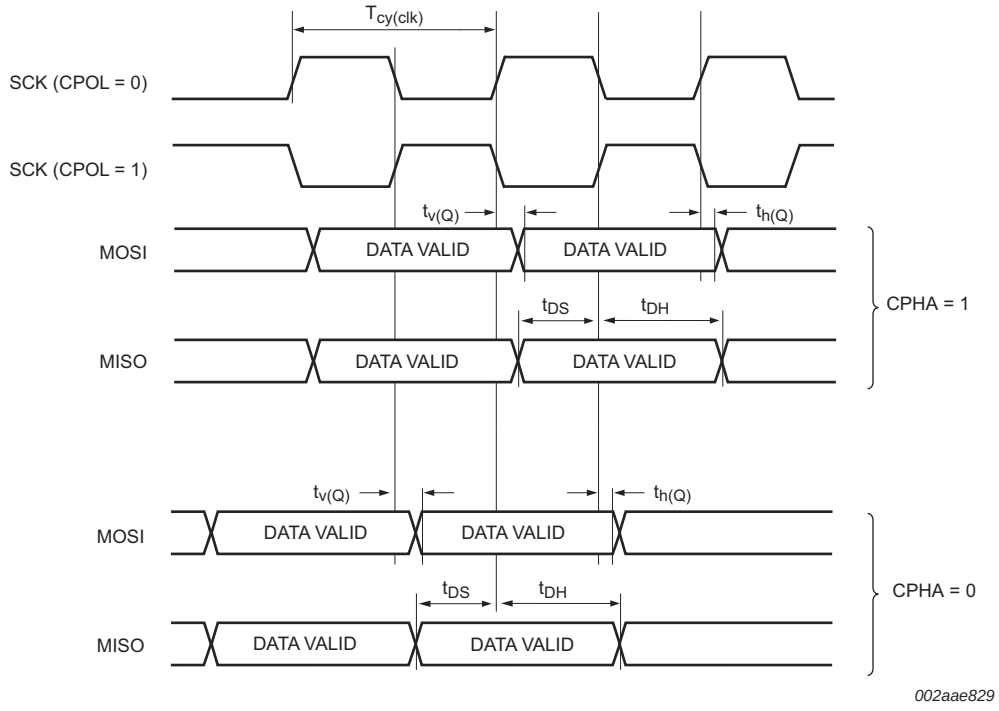


Fig 32. SSP master timing in SPI mode

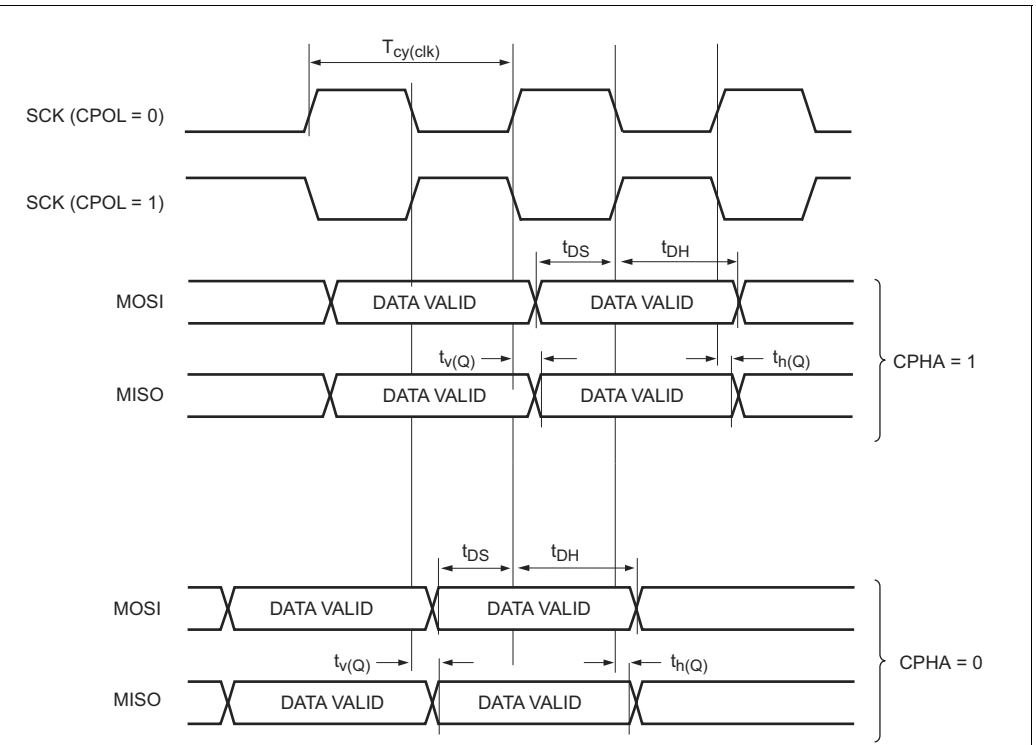


Fig 33. SSP slave timing in SPI mode

13. Characteristics of analog peripherals

Table 21. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 2				
		assertion	-	2.54	-	V
		de-assertion	-	2.68	-	V
		interrupt level 3				
		assertion	-	2.82	-	V
		de-assertion	-	2.93	-	V
		reset level 2				
		assertion	-	2.34	-	V
		de-assertion	-	2.49	-	V
		reset level 3				
		assertion	-	2.62	-	V
		de-assertion	-	2.77	-	V

[1] Interrupt and reset levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC11U6x *user manual*. Interrupt levels 0 and 1 are reserved.

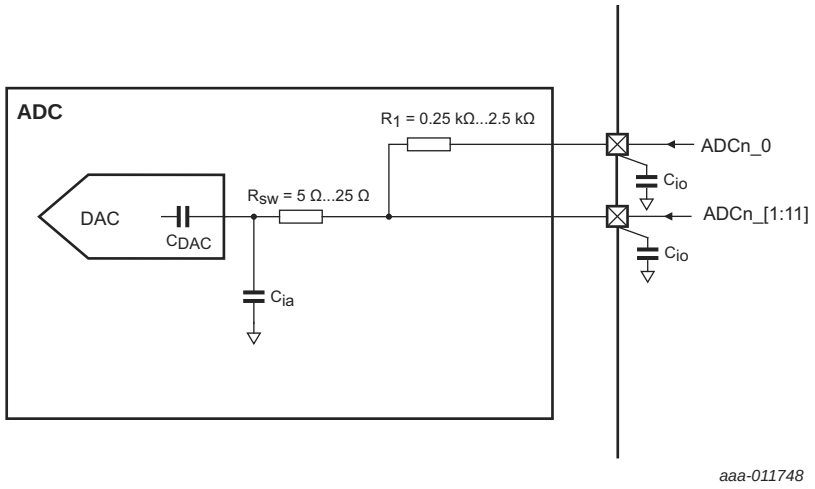


Fig 36. ADC input impedance

Table 23. Temperature sensor static and dynamic characteristics
V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C [1]	-	±5	-	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C	-	±4	-	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value [2]	-	14	-	µs

[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models).

Table 24. Temperature sensor Linear-Least-Square (LLS) fit parameters
V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range	Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C	-	-2.36	-	mV/°C
LLS intercept	T_{amb} = −40 °C to +105°C	-	606	-	mV

14. Application information

14.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 22:

- The ADC input trace must be short and as close as possible to the LPC11U6x chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- If the ADC and the digital core share a power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

14.2 Typical wake-up times

Table 25. Typical wake-up times
V_{DD} = 3.3 V; T_{amb} = 25 °C

Power modes	Wake-up time
Sleep mode (12 MHz)[1][2]	2.6 μs
Deep-sleep mode[1][3]	4.4 μs
Power-down mode[1][3]	86.8 μs
Deep Power-down mode[4]	276 μs

[1] The wake-up time measured is the time between when a GPIO input pin is triggered to wake up the device from the low-power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[2] IRC enabled, all peripherals off.

[3] WatchDog oscillator disabled, Brown-Out Detect (BOD) disabled.

[4] Wake-up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when a wake-up pin is triggered to wake up the device from the low-power modes and when a GPIO output pin is set in the reset handler.

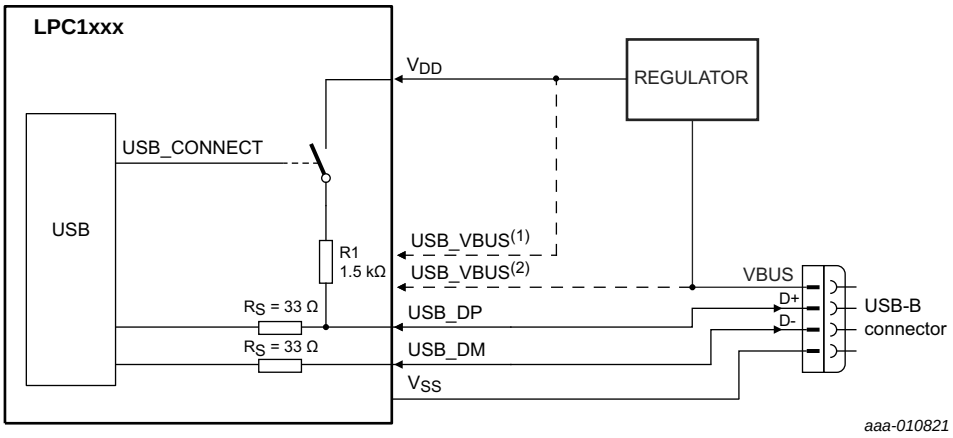
14.3 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 38) or bus-powered device (see Figure 39).

On the LPC11U6x, the PIO0_3/USB_VBUS pin is 5 V tolerant only when V_{DD} is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when V_{DD} = 0 V.

If V_{DD} is always at operating level while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where V_{DD} can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.



Two options exist for connecting VBUS to the USB_VBUS pin:

(1) Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.

(2) Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to supply V_{DD}. Since the PIO0_3/USB_VBUS pin is only 5 V tolerant when V_{DD} is at operating level, this connection can degrade the performance of the part over its lifetime. Simulation shows that lifetime is reduced to 15 years at T_{amb} = 45 °C and 8 years at T_{amb} = 55 °C assuming that USB_VBUS = 5 V is applied continuously while V_{DD} = 0 V.

Fig 39. USB interface on a bus-powered device

Remark: When a self-powered circuit is used without connecting VBUS, configure the PIO0_3/USB_VBUS pin for GPIO (PIO0_3) and provide software that can detect the host presence through some other mechanism before enabling USB_CONNECT and the SoftConnect feature. Enabling the SoftConnect without host presence leads to USB compliance failure.

14.3.1 USB Low-speed operation

The USB device controller can be used in low-speed mode supporting 1.5 Mbit/s data exchange with a USB host controller.

Remark: To operate in low-speed mode, change the board connections as follows:

1. Connect USB_DP to the D- pin of the connector.
2. Connect USB_DM to the D+ pin of the connector.

Use the IRC as clock source for the USB PLL to generate 48 MHz, then set the USB clock divider USBCLKDIV to 8 for a 6 MHz USB clock (see Figure 10 “Clock generation”).

External 10 Ω resistors are recommended in low-speed mode to reduce over-shoots and accommodate for 5 m cable length required for USB-IF testing.

External components and models used in oscillation mode are shown in Figure 42 and in Table 26 and Table 27. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} must be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 42 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 26).

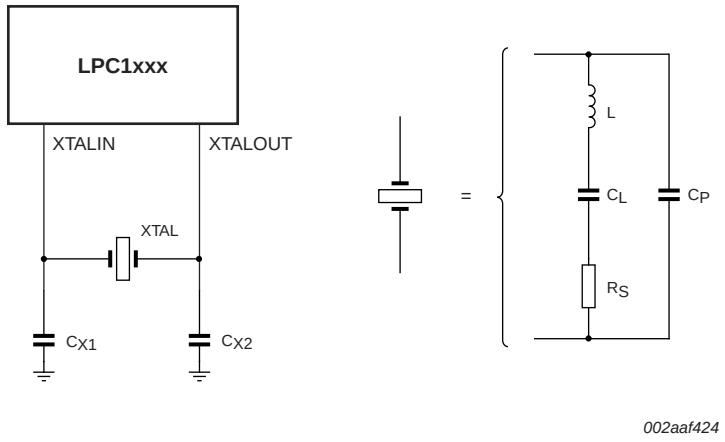


Fig 42. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 26. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

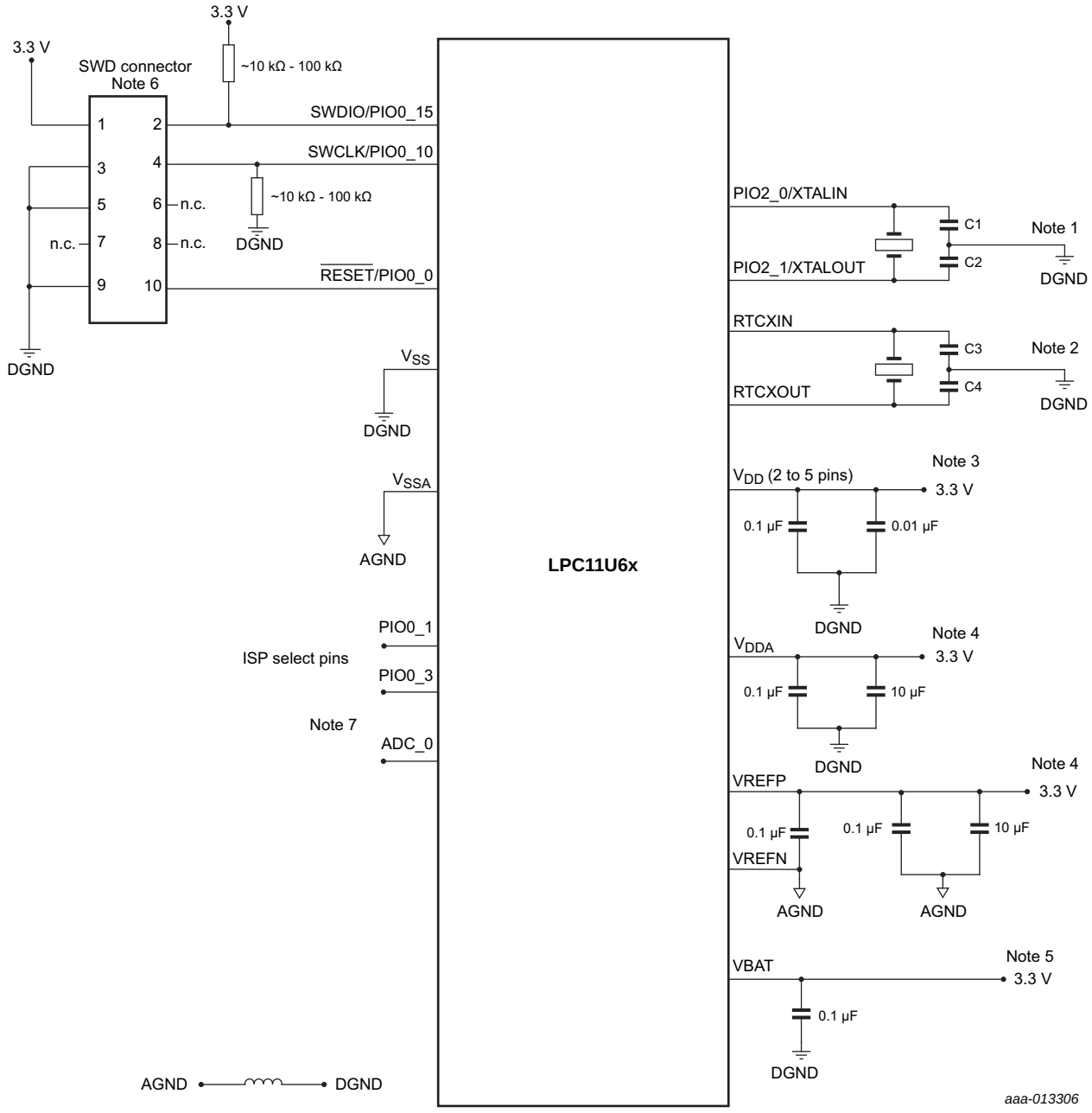
Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 27. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.5 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Smaller values of C_{x1} and C_{x2} should be chosen according to the increase in parasitics of the PCB layout.



(1) See Section 14.4 “XTAL input and crystal oscillator component selection” for the values of C1 and C2.

(2) See Section 14.6 “RTC oscillator component selection” for the values of C3 and C4.

(3) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(4) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(5) Position the decoupling capacitor of 0.1 µF as close as possible to the VBAT pin. Tie VBAT to V_{DD} if not used.

(6) Uses the ARM 10-pin interface for SWD.

(7) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

Fig 44. Power, clock, and debug connections

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