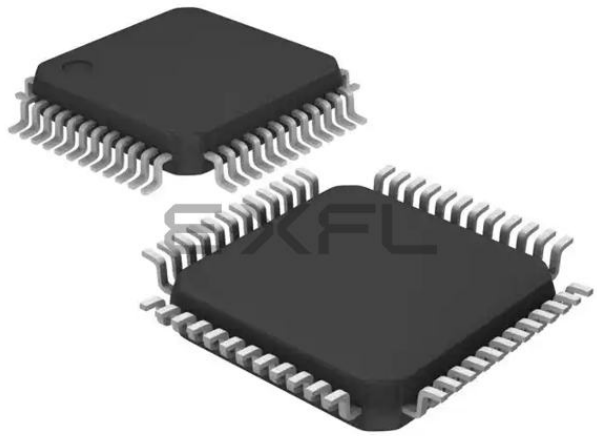

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u67jbd48e

- Power profiles.
- Flash In-Application Programming (IAP) and In-System Programming (ISP).
- 32-bit integer division routines.

- Digital peripherals:
  - Simple DMA engine with 16 channels and programmable input triggers.
  - High-speed GPIO interface connected to the ARM Cortex-M0+ IO bus with up to 80 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and programmable glitch filter and digital filter.
  - Pin interrupt and pattern match engine using eight selectable GPIO pins.
  - Two GPIO group interrupt generators.
  - CRC engine.
- Configurable PWM/timer subsystem (two 16-bit and two 32-bit standard counter/timers, two State-Configurable Timers (SCTimer/PWM)) that provides:
  - Up to four 32-bit and two 16-bit counter/timers or two 32-bit and six 16-bit counter/timers.
  - Up to 21 match outputs and 16 capture inputs.
  - Up to 19 PWM outputs with 6 independent time bases.
- Windowed WatchDog timer (WWDT).
- Real-time Clock (RTC) in the always-on power domain with separate battery supply pin and 32 kHz oscillator.
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 2 Msamples/s. The ADC supports two independent conversion sequences.
  - Temperature sensor.
- Serial interfaces:
  - Up to five USART interfaces, all with DMA, synchronous mode, and RS-485 mode support. Four USARTs use a shared fractional baud generator.
  - Two SSP controllers with DMA support.
  - Two I^2C-bus interfaces. One I^2C-bus interface with specialized open-drain pins supports I2C Fast-mode plus.
  - USB 2.0 full-speed device controller with on-chip PHY. XTAL-less low-speed mode supported.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - On-chip 32 kHz oscillator for RTC.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz. Oscillator pins are shared with the GPIO pins.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal.
  - A second, dedicated PLL is provided for USB.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.

5. Marking

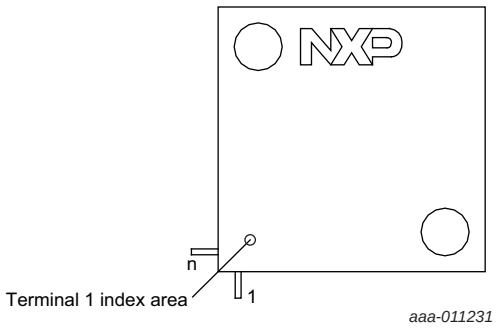


Fig 1. LQFP64/100 package marking

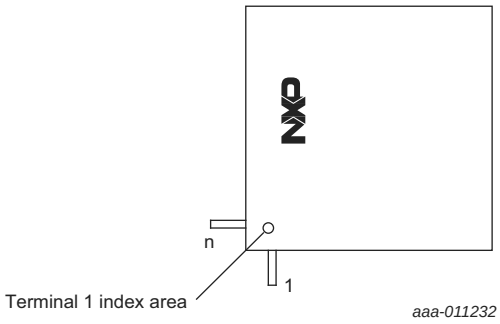


Fig 2. LQFP48 package marking

The LPC11U6x devices typically have the following top-side marking for LQFP100 packages:

LPC11U6xJBD100

xxxxxx xx

xxxyywwxR[x]

The LPC11U6x devices typically have the following top-side marking for LQFP64 packages:

LPC11U6xJ

xxxxxx xx

xxxyywwxR[x]

The LPC11U6x devices typically have the following top-side marking for LQFP48 packages:

LPC11U6xJ

xx xx

xxxyy

wwxR[x]

Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year. Field ‘R’ states the chip revision.

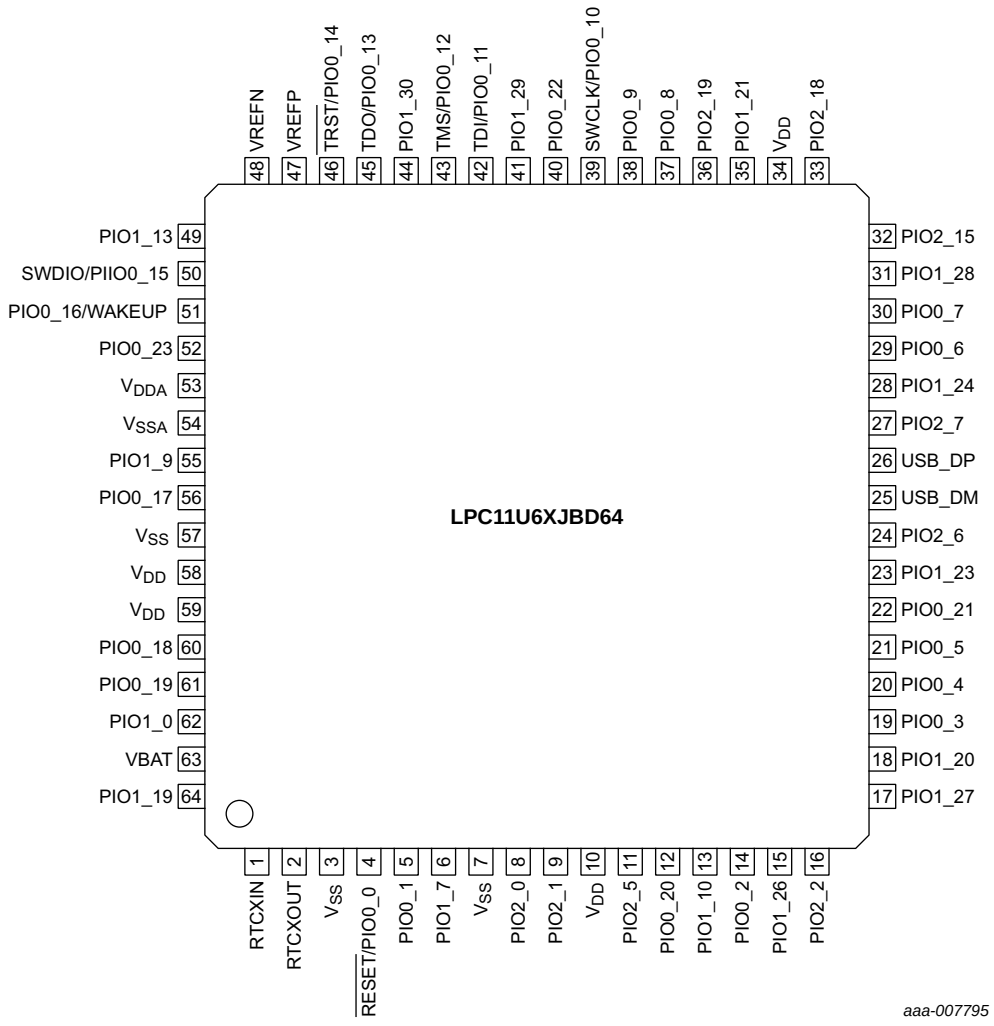


Fig 5. LQFP64 pinning

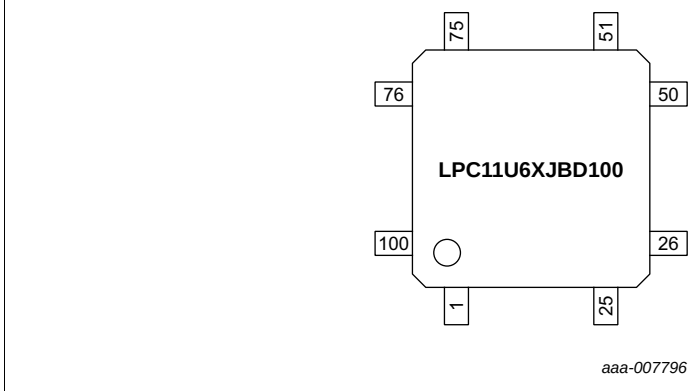


Fig 6. LQFP100 pinning

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO1_14	-	-	79	[6]	I; PU	IO	**PIO1_14 —** General-purpose digital input/output pin.
						IO	**I2C1_SDA —** I^2C1-bus data input/output (not open-drain).
						O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
						-	**R_23 —** Reserved.
PIO1_15	-	-	87	[6]	I; PU	IO	**PIO1_15 —** General-purpose digital input/output pin.
						IO	**SSP0_SSEL —** Slave select for SSP0.
						O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	**R_24 —** Reserved.
PIO1_16	-	-	96	[6]	I; PU	IO	**PIO1_16 —** General-purpose digital input/output pin.
						IO	**SSP0_MISO —** Master In Slave Out for SSP0.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	**R_25 —** Reserved.
PIO1_17	-	-	34	[6]	I; PU	IO	**PIO1_17 —** General-purpose digital input/output pin.
						I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
						I	**U0_RXD —** Receiver input for USART0.
						-	**R_26 —** Reserved.
PIO1_18	-	-	43	[6]	I; PU	IO	**PIO1_18 —** General-purpose digital input/output pin.
						I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						O	**U0_TXD —** Transmitter output for USART0.
						-	**R_27 —** Reserved.
PIO1_19	-	64	4	[6]	I; PU	IO	**PIO1_19 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U2\_CTS}}$ —** Clear To Send input for USART2.
						O	**SCT0_OUT0 —** SCTimer0/PWM output 0.
						-	**R_28 —** Reserved.
PIO1_20	13	18	29	[6]	I; PU	IO	**PIO1_20 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U0\_DSR}}$ —** Data Set Ready input for USART0.
						IO	**SSP1_SCK —** Serial clock for SSP1.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO1_21	25	35	56	[6]	I; PU	IO	**PIO1_21 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U0\_DCD}}$ —** Data Carrier Detect input for USART0.
						IO	**SSP1_MISO —** Master In Slave Out for SSP1.
						I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
PIO1_22	-	-	80	[3]	I; PU	IO	**PIO1_22 —** General-purpose digital input/output pin.
						IO	**SSP1_MOSI —** Master Out Slave In for SSP1.
						I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
						AI	**ADC_4 —** A/D converter, input channel 4.
						-	**R_29 —** Reserved.

8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 50 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 AHB multilayer matrix

The AHB multilayer matrix supports three masters, the M0+ core, the DMA, and the USB. All masters can access all slaves (peripherals and memories).

Table 4. PWM resources *…continued*

PWM outputs			Peripheral	Pin functions available for PWM			Match registers used
LQFP100	LQFP64	LQFP48		LQFP100	LQFP64	LQFP48	
3	3	3	CT32B1	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	4
4	4	3	SCTIMER0/ PWM	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	up to 5
4	2	-	SCTIMER1/ PWM	SCT1_OUT0, SCT1_OUT1, SCT1_OUT2, SCT1_OUT3	SCT1_OUT2, SCT1_OUT3	-	up to 5

The standard timers and the SCTimers combine to up to eight independent timers. Each SCTimer can be configured either as one 32-bit timer or two independently counting 16-bit timers which use the same input clock. The following combinations are possible:

Table 5. Timer configurations

32-bit timers	Resources	16-bit timers	Resources
4	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer, SCTimer1/PWM as 32-bit timer	2	CT16B0, CT16B1
2	CT32B0, CT32B1	6	CT16B0, CT16B1, SCTimer0/PWM as two 16-bit timers, SCTimer1/PWM as two 16-bit timers
3	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer (or SCTimer1/PWM as 32-bit timer)	4	CT16B0, CT16B1, SCTimer1/PWM as two 16-bit timers (or SCTimer0/PWM as two 16-bit timers)

8.19.1 State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM)

The state configurable timer can create timed output signals such as PWM outputs triggered by programmable events. Combinations of events can be used to define timer states. The SCTimer/PWM can control the timer operations, capture inputs, change states, and toggle outputs triggered only by events entirely without CPU intervention.

If multiple states are not implemented, the SCTimer/PWM simply operates as one 32-bit or two 16-bit timers with match, capture, and PWM functions.

Table 7. Thermal resistance value (C/W): ±15 %

Symbol	Parameter	Conditions	Typ	Unit
LQFP64				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	58	°C/W
		1 m/s	51	°C/W
		2.5 m/s	47	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	81	°C/W
		1 m/s	66	°C/W
		2.5 m/s	60	°C/W
θjc	thermal resistance junction-to-case		18	°C/W
θjb	thermal resistance junction-to-board		23	°C/W
LQFP100				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	49	°C/W
		1 m/s	44	°C/W
		2.5 m/s	41	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	66	°C/W
		1 m/s	55	°C/W
		2.5 m/s	51	°C/W
θjc	thermal resistance junction-to-case		18	°C/W
θjb	thermal resistance junction-to-board		24	°C/W

11. Static characteristics

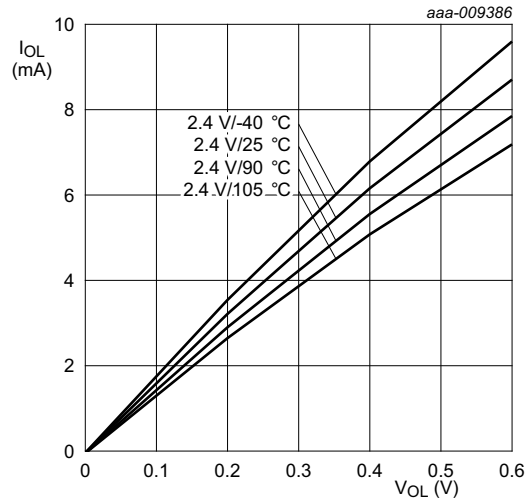
Table 8. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

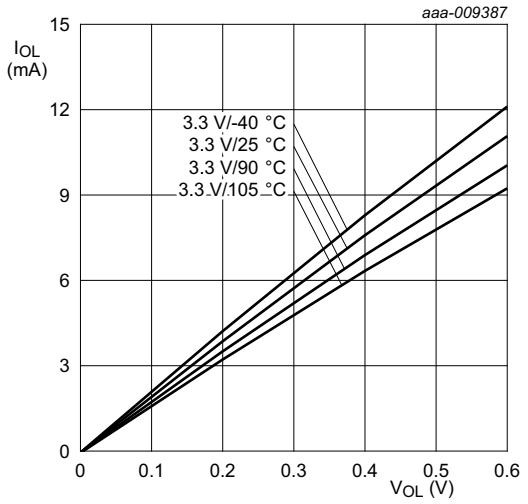
Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)	[2]	2.4	3.3	3.6	V
V_{DDA}	analog supply voltage		2.4	3.3	3.6	V
V_{ref}	reference voltage	on pin VREFP	2.4	-	V_{DDA}	V
V_{BAT}	battery supply voltage		2.4	3.3	3.6	V

Table 9. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
RTC	-	0.02	0.10	-
WWDT	-	0.05	0.17	Main clock selected as clock source for the WDT.
I2C0	-	0.05	0.22	-
I2C1	-	0.05	0.18	-
SSP0	-	0.15	0.59	-
SSP1	-	0.15	0.58	-
USART0	-	0.31	1.19	-
USART1	-	0.12	0.50	-
USART2	-	0.13	0.49	-
USART3 + USART4	-	0.21	0.81	-
USB	-	0.43	0.72	Register interface disabled in SYSAHBCLKCTRL.
USB PHY	0.54	-	-	
ADC0	-	2.15	2.68	Register interface disabled in SYSAHBCLKCTRL and analog block disabled in PDRUNCFG registers. Power consumption measured while the ADC is sampling a single channel with an ADC clock of 12 MHz or 48 MHz.
Temperature sensor	0.18	-	-	-
DMA	-	0.28	1.1	-
CRC	-	0.04	0.14	-

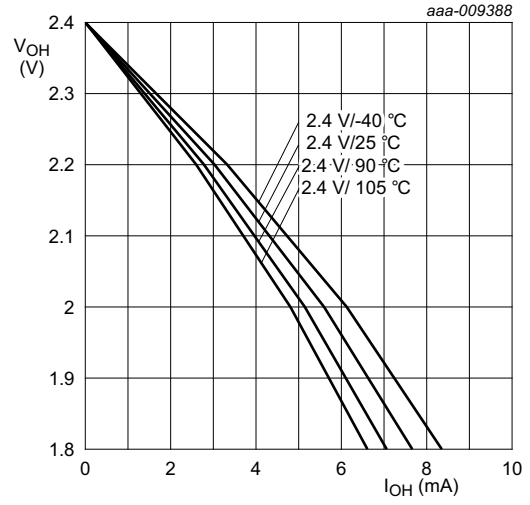


Conditions: V_{DD} = 2.4 V; standard port pins and high-drive pins PIO0_7 and PIO1_31.

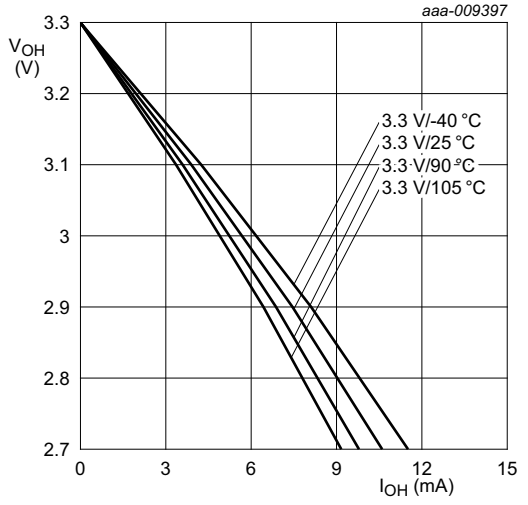


Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pins PIO0_7 and PIO1_31.

Fig 25. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 2.4 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 26. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

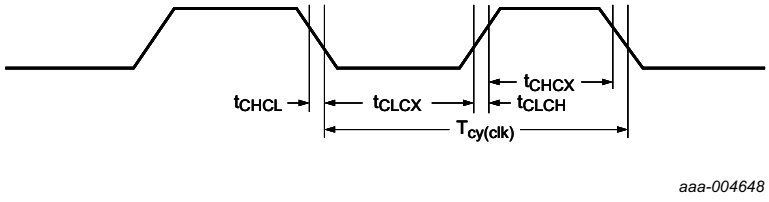


Fig 29. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.3 Internal oscillators

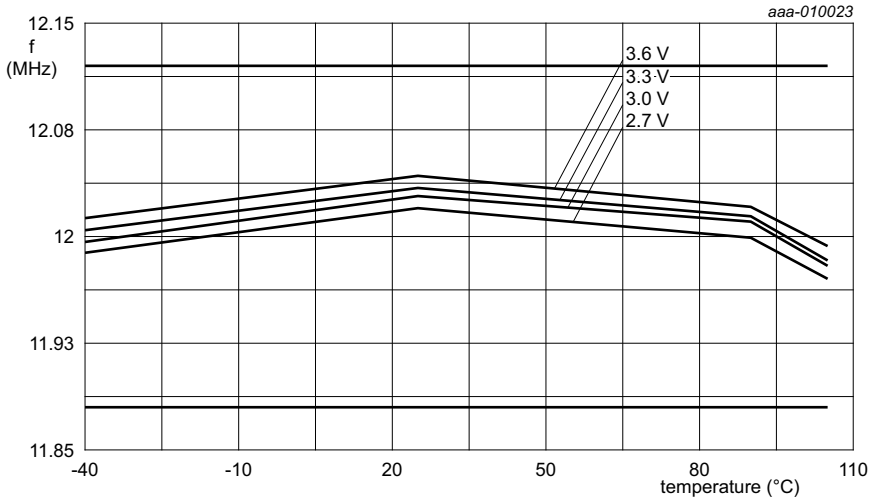
Table 13. Dynamic characteristics: IRC

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	−25 °C ≤ T_{amb} ≤ +85 °C	12 - 1%	12	12 + 1 %	MHz
		−40 °C ≤ T_{amb} < −25 °C	12 - 2%	12	12 + 1 %	MHz
		85 °C < T_{amb} ≤ 105 °C	12 - 1.5 %	12	12 + 1.5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −25 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 30. Typical Internal RC oscillator frequency versus temperature

Table 14. Dynamic characteristics: WatchDog oscillator

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; [2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register [2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] See the LPC11U6x *user manual.*

12.4 I/O pins

Table 15. Dynamic characteristics: I/O pins[1]
T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

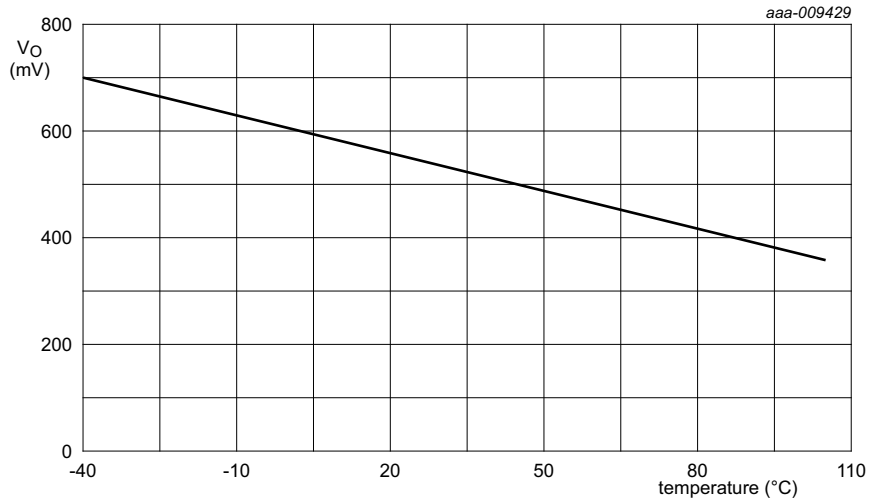
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.5 I²C-bus

Table 16. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus; on pins PIO0_4 and PIO0_5	0	1	MHz
t_f	fall time [4][5][6][7]	of both SDA and SCL signals	-	300	ns
		Standard-mode			
		Fast-mode	20 + 0.1 × C_b	300	ns
		Fast-mode Plus; on pins PIO0_4 and PIO0_5	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	µs
		Fast-mode	1.3	-	µs
		Fast-mode Plus; on pins PIO0_4 and PIO0_5	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	µs
		Fast-mode	0.6	-	µs
		Fast-mode Plus; on pins PIO0_4 and PIO0_5	0.26	-	µs



V_{DDA} = 3.3 V; measured on a typical silicon sample.

Fig 37. Typical LLS fit of the temperature sensor output voltage

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin is greater than 0.7 V_{DD} to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

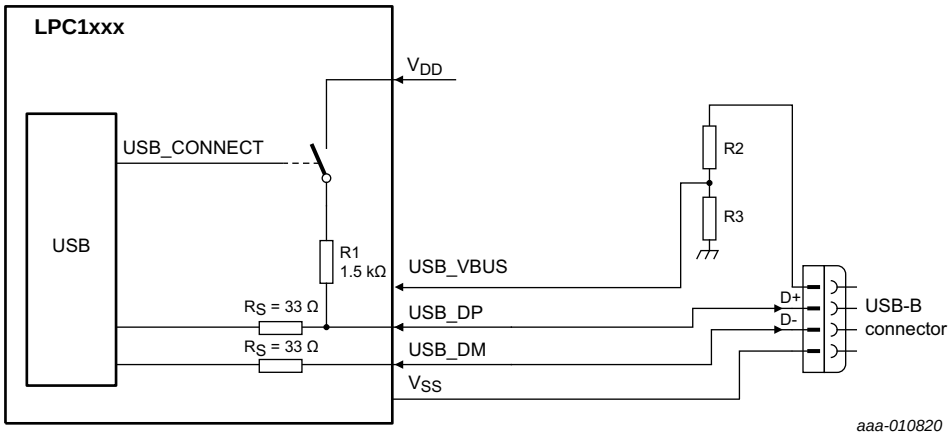


Fig 38. USB interface on a self-powered device where USB_VBUS = 5 V

The USB_CONNECT function can be enabled internally by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required for the USB_CONNECT functionality.

External components and models used in oscillation mode are shown in Figure 42 and in Table 26 and Table 27. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} must be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 42 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 26).

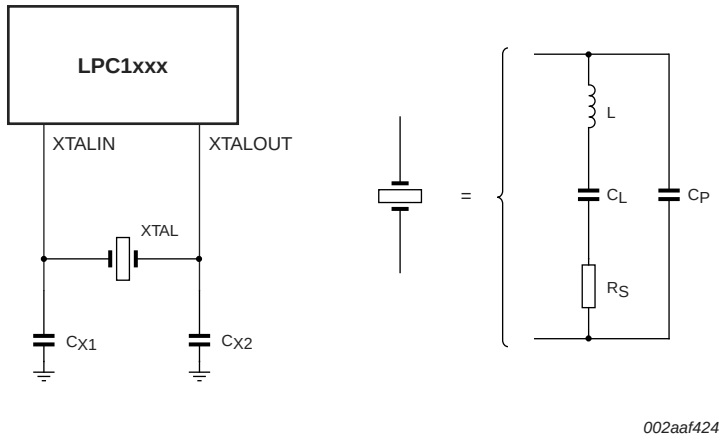


Fig 42. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 26. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 27. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.6 RTC oscillator component selection

The 32 kHz crystal must be connected to the part via the RTCXIN and RTCXOUT pins as shown in Figure 43. If the RTC is not used, the RTCXIN pin can be grounded.

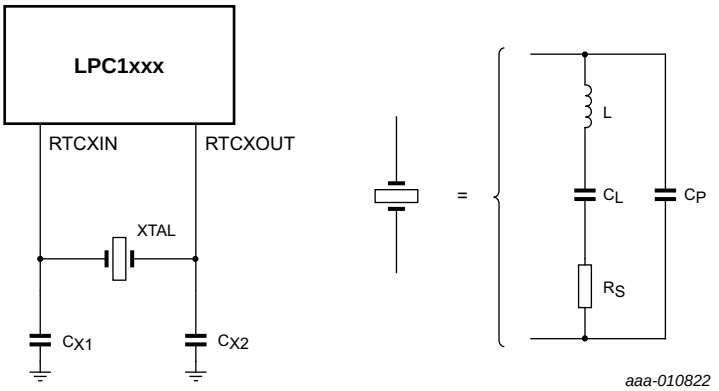


Fig 43. RTC oscillator components

Select C_{x1} and C_{x2} based on the external 32 kHz crystal used in the application circuitry. The pad capacitance C_P of the RTCXIN and RTCXOUT pad is 3 pF. If the load capacitance of the external crystal is C_L, the optimal C_{x1} and C_{x2} can be selected as:

$C_{x1} = C_{x2} = 2 \times C_L - C_P$

14.7 Connecting power, clocks, and debug functions

Figure 44 shows the basic board connections used to power the LPC11U6x, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.

14.9 Pin states in different power modes

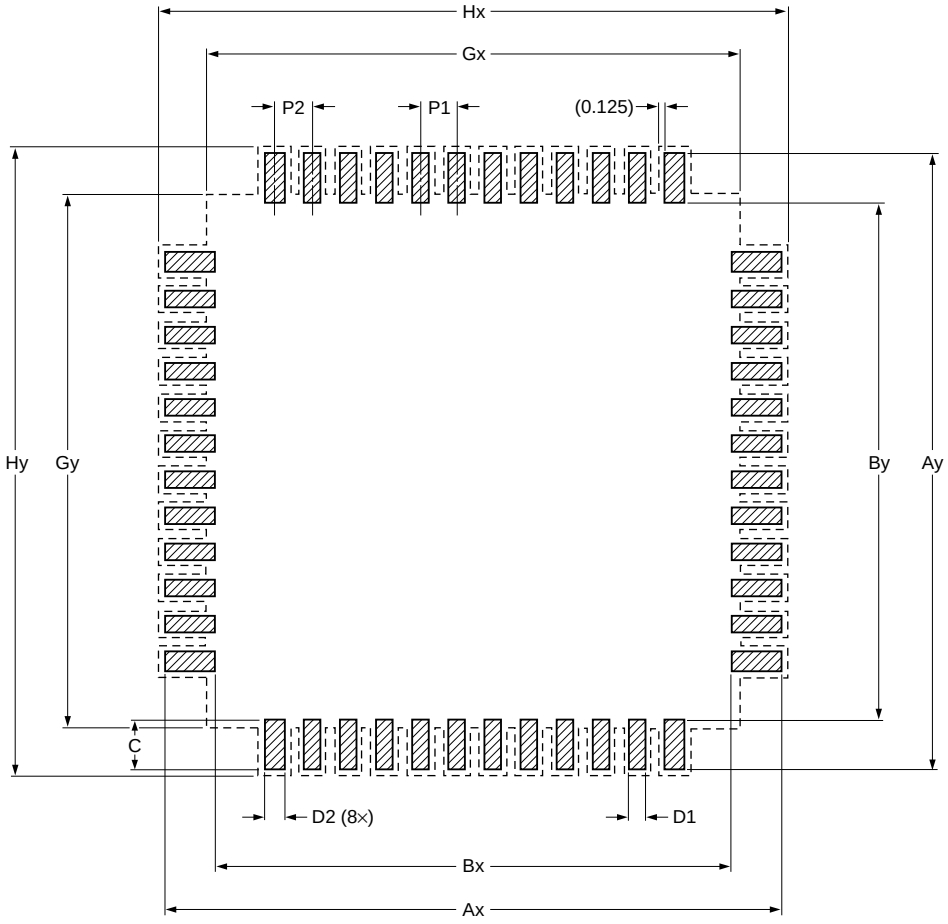
Table 29. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/Power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_4, PIO0_5 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, the $\overline{\text{RESET}}$ pin needs an external pull-up to reduce power consumption.
PIO0_16/ WAKEUP	As configured in the IOCON[1]. WAKEUP function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

16. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

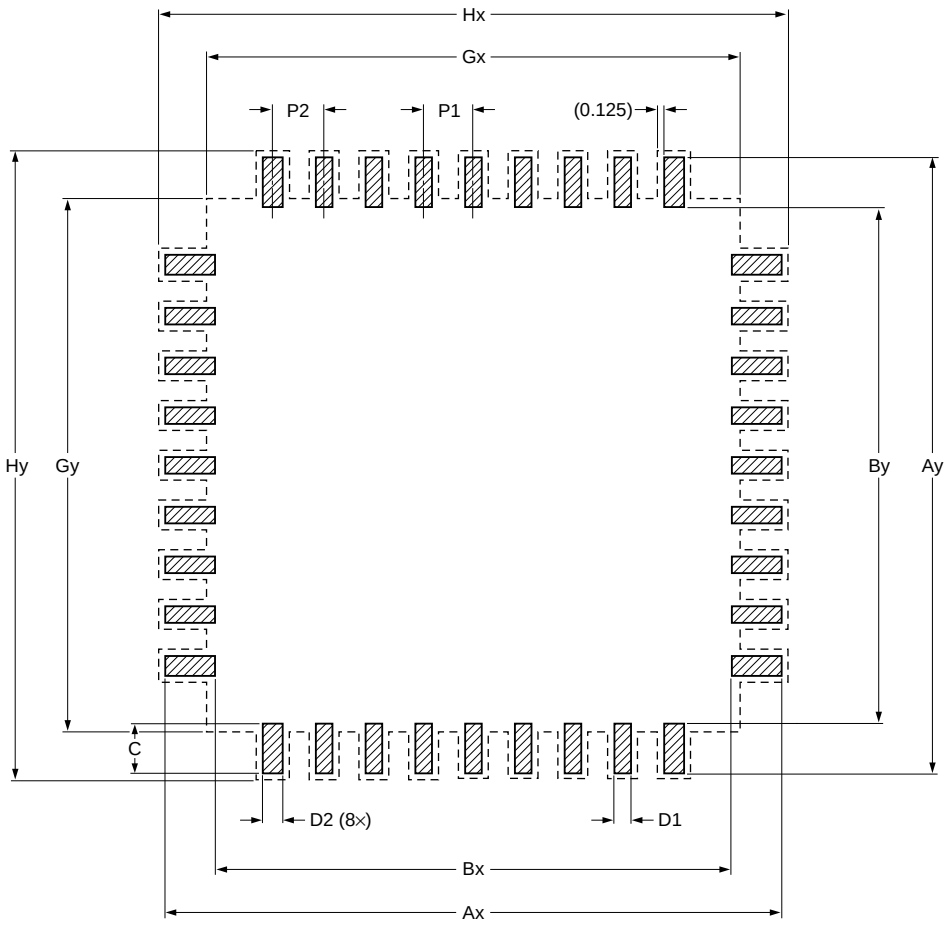
DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 48. Reflow soldering for the LQFP48 package

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 50. Reflow soldering for the LQFP100 package

17. References

[1] LPC11U6x User manual UM10732:
http://www.nxp.com/documents/user_manual/UM10732.pdf

[2] LPC11U6x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC11U6X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

21. Contents

continued >>