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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u67jbd64e

7. Pinning information

7.1 Pinning

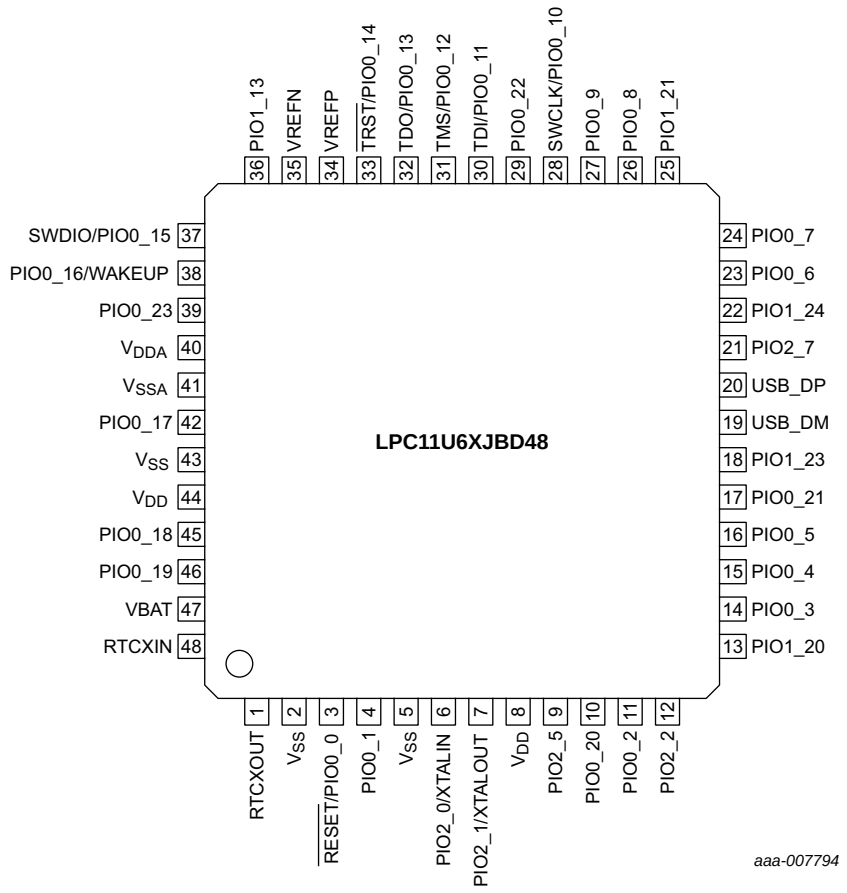


Fig 4. LQFP48 pinning

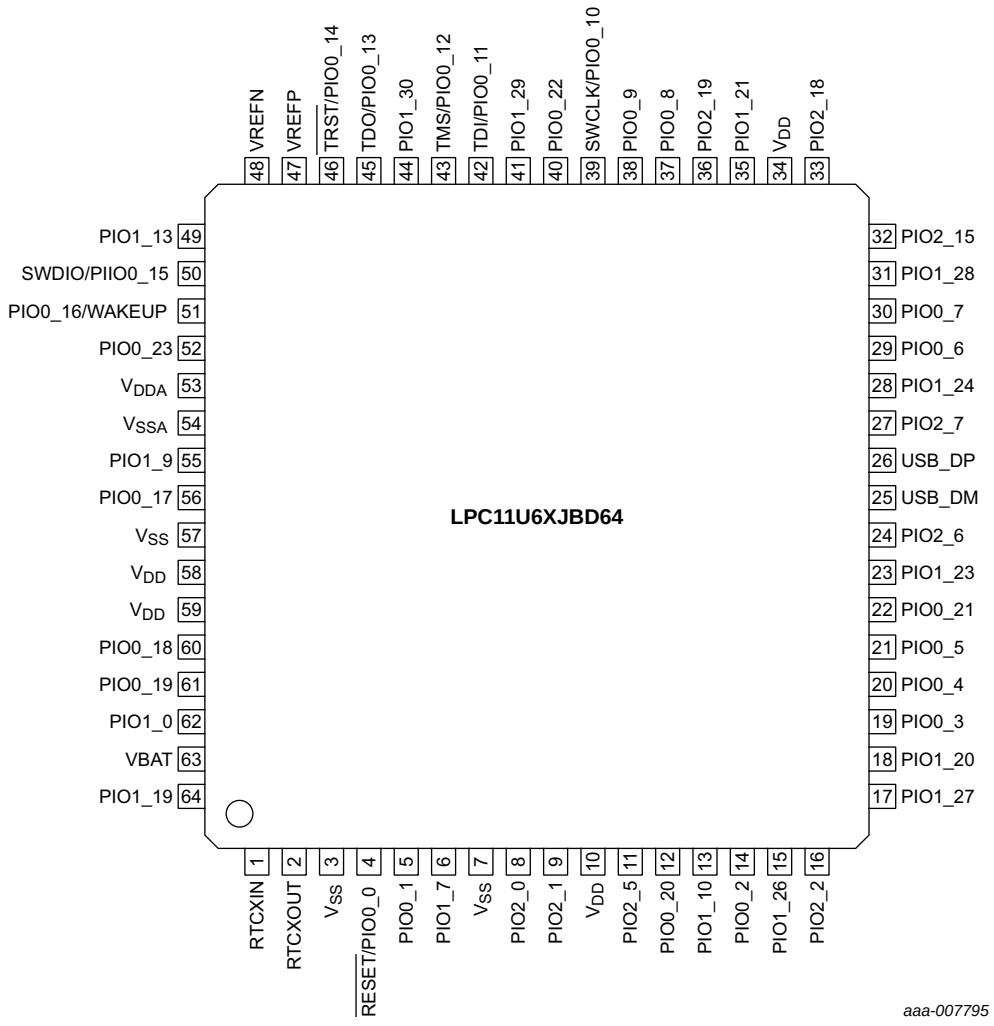


Fig 5. LQFP64 pinning

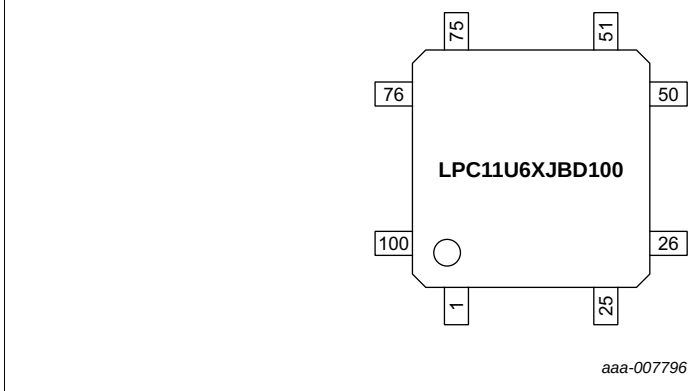


Fig 6. LQFP100 pinning

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO1_14	-	-	79	[6]	I; PU	IO	**PIO1_14 —** General-purpose digital input/output pin.
						IO	**I2C1_SDA —** I^2C1-bus data input/output (not open-drain).
						O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
						-	**R_23 —** Reserved.
PIO1_15	-	-	87	[6]	I; PU	IO	**PIO1_15 —** General-purpose digital input/output pin.
						IO	**SSP0_SSEL —** Slave select for SSP0.
						O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	**R_24 —** Reserved.
PIO1_16	-	-	96	[6]	I; PU	IO	**PIO1_16 —** General-purpose digital input/output pin.
						IO	**SSP0_MISO —** Master In Slave Out for SSP0.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	**R_25 —** Reserved.
PIO1_17	-	-	34	[6]	I; PU	IO	**PIO1_17 —** General-purpose digital input/output pin.
						I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
						I	**U0_RXD —** Receiver input for USART0.
						-	**R_26 —** Reserved.
PIO1_18	-	-	43	[6]	I; PU	IO	**PIO1_18 —** General-purpose digital input/output pin.
						I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						O	**U0_TXD —** Transmitter output for USART0.
						-	**R_27 —** Reserved.
PIO1_19	-	64	4	[6]	I; PU	IO	**PIO1_19 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U2\_CTS}}$ —** Clear To Send input for USART2.
						O	**SCT0_OUT0 —** SCTimer0/PWM output 0.
						-	**R_28 —** Reserved.
PIO1_20	13	18	29	[6]	I; PU	IO	**PIO1_20 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U0\_DSR}}$ —** Data Set Ready input for USART0.
						IO	**SSP1_SCK —** Serial clock for SSP1.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO1_21	25	35	56	[6]	I; PU	IO	**PIO1_21 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U0\_DCD}}$ —** Data Carrier Detect input for USART0.
						IO	**SSP1_MISO —** Master In Slave Out for SSP1.
						I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
PIO1_22	-	-	80	[3]	I; PU	IO	**PIO1_22 —** General-purpose digital input/output pin.
						IO	**SSP1_MOSI —** Master Out Slave In for SSP1.
						I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
						AI	**ADC_4 —** A/D converter, input channel 4.
						-	**R_29 —** Reserved.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100	Reset state[1]	Type	Description of pin functions
PIO1_23	18	23	35 [6]	I; PU	IO	**PIO1_23 —** General-purpose digital input/output pin.
					O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					IO	**SSP1_SSEL —** Slave select for SSP1.
					O	**U2_TXD —** Transmitter output for USART2.
PIO1_24	22	28	42 [6]	I; PU	IO	**PIO1_24 —** General-purpose digital input/output pin.
					O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
					IO	**I2C1_SDA —** I^2C-bus data input/output (not open-drain).
PIO1_25	-	-	100 [6]	I; PU	IO	**PIO1_25 —** General-purpose digital input/output pin.
					O	**U2_$\overline{\text{RTS}}$ —** Request To Send output for USART2.
					IO	**U2_SCLK —** Serial clock input/output for USART2 in synchronous mode.
					I	**SCT0_IN0 —** SCTimer0/PWM input 0.
					-	**R_30 —** Reserved.
PIO1_26	-	15	20 [6]	I; PU	IO	**PIO1_26 —** General-purpose digital input/output pin.
					O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					I	**U0_RXD —** Receiver input for USART0.
					-	**R_19 —** Reserved.
PIO1_27	-	17	22 [6]	I; PU	IO	**PIO1_27 —** General-purpose digital input/output pin.
					O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					O	**U0_TXD —** Transmitter output for USART0.
					-	**R_20 —** Reserved.
					IO	**SSP1_SCK —** Serial clock for SSP1.
PIO1_28	-	31	46 [6]	I; PU	IO	**PIO1_28 —** General-purpose digital input/output pin.
					I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					IO	**U0_SCLK —** Serial clock input/output for USART in synchronous mode.
					O	**U0_$\overline{\text{RTS}}$ —** Request To Send output for USART0.
PIO1_29	-	41	63 [3]	I; PU	IO	**PIO1_29 —** General-purpose digital input/output pin.
					IO	**SSP0_SCK —** Serial clock for SSP0.
					I	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.
					O	**U0_$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART0.
					AI	**ADC_10 —** A/D converter, input channel 10.
PIO1_30	-	44	67 [6]	I; PU	IO	**PIO1_30 —** General-purpose digital input/output pin.
					IO	**I2C1_SCL —** I^2C1-bus clock input/output (not open-drain).
					I	**SCT0_IN3 —** SCTimer0/PWM input 3.
					-	**R_31 —** Reserved.
PIO1_31	-	-	48 [5]	I; PU	IO	**PIO1_31 —** General-purpose digital input/output pin (high-current output driver).

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO2_13	-	-	26	[6]	I; PU	IO	**PIO2_13 —** General-purpose digital input/output pin.
						I	**U4_CTS —** Clear To Send input for USART4.
PIO2_14	-	-	27	[6]	I; PU	IO	**PIO2_14 —** General-purpose digital input/output pin.
						I	**SCT1_IN2 —** SCTimer1/PWM input 2.
PIO2_15	-	32	49	[6]	I; PU	IO	**PIO2_15 —** General-purpose digital input/output pin.
						I	**SCT1_IN3 —** SCTimer1/PWM input 3.
PIO2_16	-	-	50	[6]	I; PU	IO	**PIO2_16 —** General-purpose digital input/output pin.
						O	**SCT1_OUT0 —** SCTimer1/PWM output 0.
PIO2_17	-	-	51	[6]	I; PU	IO	**PIO2_17 —** General-purpose digital input/output pin.
						O	**SCT1_OUT1 —** SCTimer1/PWM output 1.
PIO2_18	-	33	52	[6]	I; PU	IO	**PIO2_18 —** General-purpose port 2 input/output 18.
						O	**SCT1_OUT2 —** SCTimer1/PWM output 2.
PIO2_19	-	36	57	[6]	I; PU	IO	**PIO2_19 —** General-purpose port 2 input/output 19.
						O	**SCT1_OUT3 —** SCTimer1/PWM output 3.
PIO2_20	-	-	75	[6]	I; PU	IO	**PIO2_20 —** General-purpose port 2 input/output 20.
PIO2_21	-	-	76	[6]	I; PU	IO	**PIO2_21 —** General-purpose port 2 input/output 21.
PIO2_22	-	-	77	[6]	I; PU	IO	**PIO2_22 —** General-purpose port 2 input/output 22.
PIO2_23	-	-	1	[6]	I; PU	IO	**PIO2_23 —** General-purpose port 2 input/output 23.
$\overline{\text{RSTOUT}}$	-	-	88	[6]	IA	IO	Internal reset status output.
USB_DP	20	26	39	[9]	F	-	USB bidirectional D+ line. Pad includes internal 33 Ω series termination resistor.
USB_DM	19	25	38	[9]	F	-	USB bidirectional D− line. Pad includes internal 33 Ω series termination resistor.
RTCXIN	48	1	5	[2]	-	-	RTC oscillator input. This input should be grounded if the RTC is not used.
RTCXOUT	1	2	6	[2]	-	-	RTC oscillator output.
VREFP	34	47	73		-	-	ADC positive reference voltage. If the ADC is not used, tie VREFP to V_{DD}.
VREFN	35	48	74		-	-	ADC negative voltage reference. If the ADC is not used, tie VREFN to V_{SS}.
V_{DDA}	40	53	84		-	-	Analog voltage supply. V_{DDA}should typically be the same voltages as V_{DD} but should be isolated to minimize noise and error. V_{DDA} should be tied to V_{DD} if the ADC is not used.
V_{DD}	44, 8	58, 10, 34, 59	92, 14, 71, 54, 93		-	-	Supply voltage to the internal regulator and the external rail.

Table 4. PWM resources *…continued*

PWM outputs			Peripheral	Pin functions available for PWM			Match registers used
LQFP100	LQFP64	LQFP48		LQFP100	LQFP64	LQFP48	
3	3	3	CT32B1	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	4
4	4	3	SCTIMER0/ PWM	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	up to 5
4	2	-	SCTIMER1/ PWM	SCT1_OUT0, SCT1_OUT1, SCT1_OUT2, SCT1_OUT3	SCT1_OUT2, SCT1_OUT3	-	up to 5

The standard timers and the SCTimers combine to up to eight independent timers. Each SCTimer can be configured either as one 32-bit timer or two independently counting 16-bit timers which use the same input clock. The following combinations are possible:

Table 5. Timer configurations

32-bit timers	Resources	16-bit timers	Resources
4	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer, SCTimer1/PWM as 32-bit timer	2	CT16B0, CT16B1
2	CT32B0, CT32B1	6	CT16B0, CT16B1, SCTimer0/PWM as two 16-bit timers, SCTimer1/PWM as two 16-bit timers
3	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer (or SCTimer1/PWM as 32-bit timer)	4	CT16B0, CT16B1, SCTimer1/PWM as two 16-bit timers (or SCTimer0/PWM as two 16-bit timers)

8.19.1 State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM)

The state configurable timer can create timed output signals such as PWM outputs triggered by programmable events. Combinations of events can be used to define timer states. The SCTimer/PWM can control the timer operations, capture inputs, change states, and toggle outputs triggered only by events entirely without CPU intervention.

If multiple states are not implemented, the SCTimer/PWM simply operates as one 32-bit or two 16-bit timers with match, capture, and PWM functions.

8.27 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC11U6x is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	[2]	–0.5	4.6	V
V_{DDA}	analog supply voltage		–0.5	4.6	V
V_{ref}	reference voltage	on pin VREFP	–0.5	4.6	V
V_{BAT}	battery supply voltage		–0.5	4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present [3][4]	–0.5	+5.5	V
		on open-drain I2C-bus pins PIO0_4 and PIO0_5 [5]	–0.5	+5.5	V
		USB_DM, USB_DP pins	–0.5	V_{DD} + 0.5	V
V_{IA}	analog input voltage	[6] [7]	–0.5	4.6	V
$V_{i(xtal)}$	crystal input voltage	pins configured for XTALIN and XTALOUT [2]	–0.5	+2.5	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	[2]	–0.5	4.6	V
I_{DD}	supply current	per supply pin	-	100	mA
I_{SS}	ground current	per ground pin	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5\ V_{DD(IO)}) < V_I < (1.5\ V_{DD(IO)})$; $T_j < 125$ °C	-	100	mA
T_{stg}	storage temperature	[8]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins [9]	-	3	kV

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 8) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_4 and PIO0_5.

[4] Including the voltage on outputs in 3-state mode.

[5] $V_{DD(IO)}$ present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when $V_{DD(IO)}$ is powered down.

[6] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[7] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[8] Dependent on package type.

[9] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 7. Thermal resistance value (C/W): ±15 %

Symbol	Parameter	Conditions	Typ	Unit
LQFP48				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	67	°C/W
		1 m/s	58	°C/W
		2.5 m/s	53	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	100	°C/W
		1 m/s	79	°C/W
		2.5 m/s	71	°C/W
θjc	thermal resistance junction-to-case		15	°C/W
θjb	thermal resistance junction-to-board		19	°C/W

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	$V_{DD} \geq 2.4$ V; 5 V tolerant pins [14] [15]	0	-	5	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage		0.05 V_{DD}	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD}$ − 0.4 V;	4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [16]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$ [16]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.4 V ≤ V_{DD} ≤ 3.6 V	−10	−50	−85	µA
		$V_{DD} < V_I < 5$ V	0	0	0	µA
High-drive output pins configured as digital pin (PIO0_7 and PIO1_31); see Figure 13						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	$V_{DD} \geq 2.4$ V [14] [15]	0	-	5	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage		0.05 V_{DD}	-	-	V

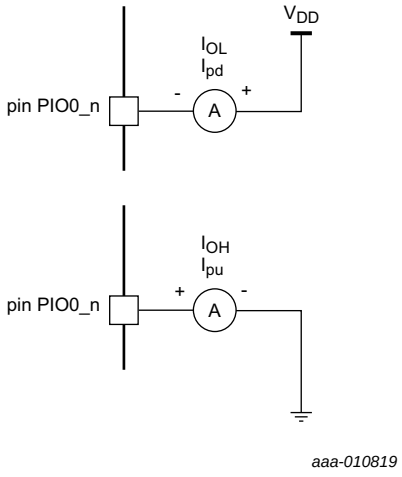
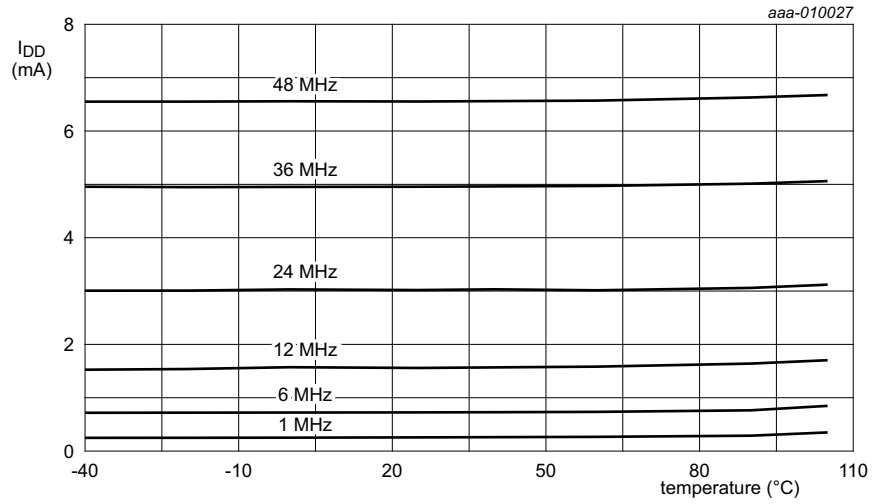


Fig 13. Pin input/output current measurement



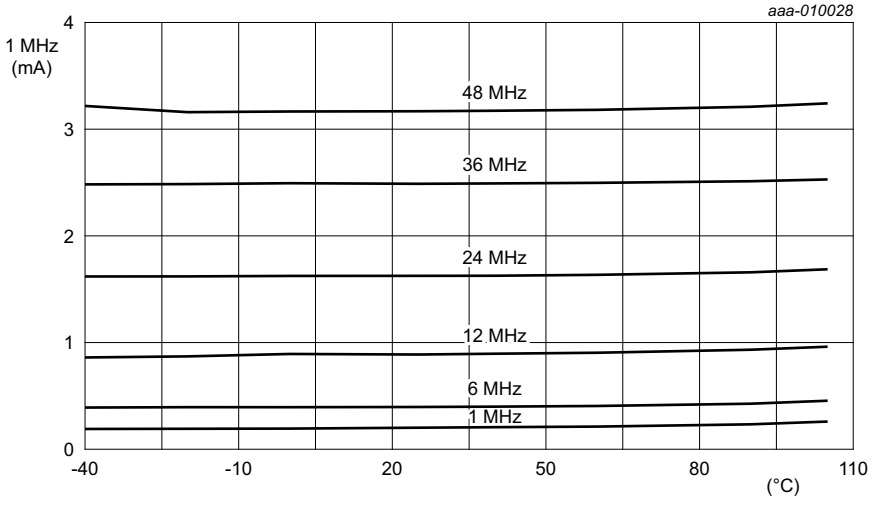
Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 50 MHz: IRC disabled; PLL enabled; sysosc enabled.

Fig 15. Active mode: Typical supply current I_{DD} versus temperature



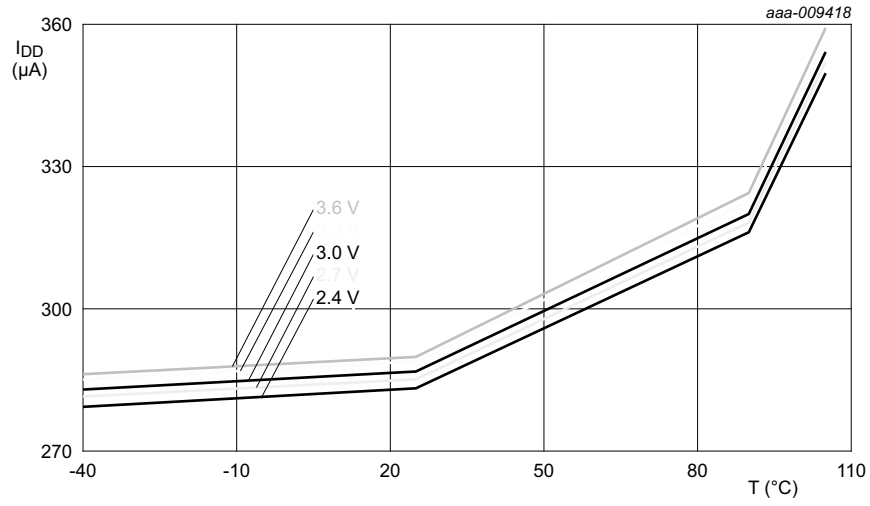
Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F) all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

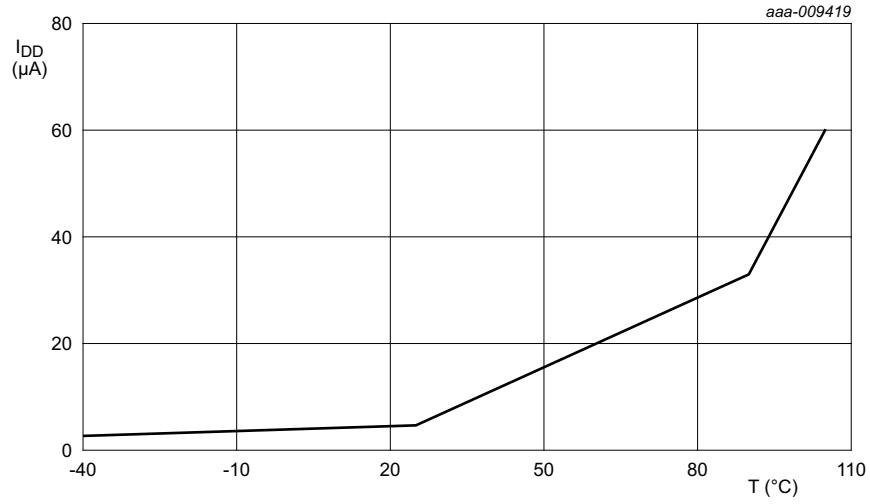
24 MHz to 48 MHz: IRC disabled; PLL enabled; sysosc enabled.

Fig 16. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



Conditions: BOD disabled; all oscillators and analog blocks disabled

Fig 17. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



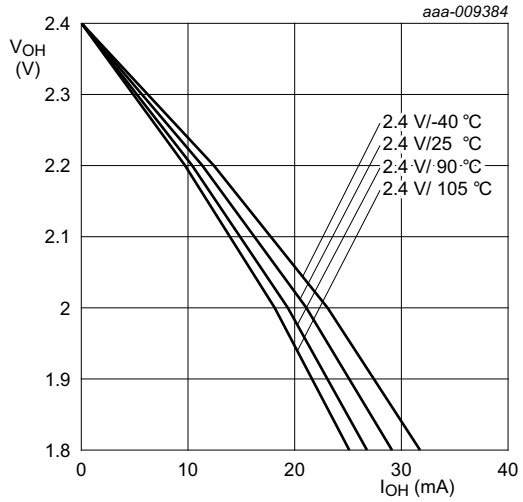
Conditions: BOD disabled; all oscillators and analog blocks disabled; V_{DD} = 2.4 V to 3.6 V.

Fig 18. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

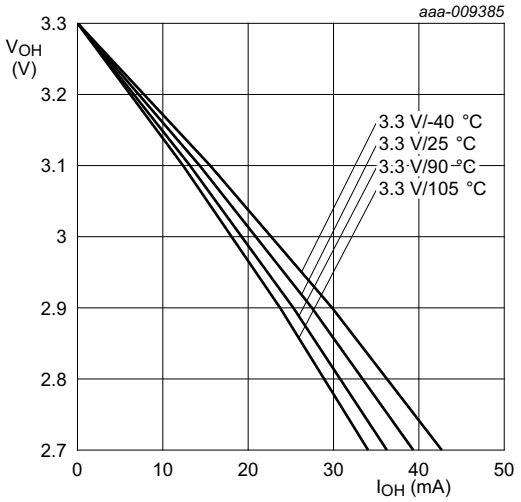
Table 9. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
RTC	-	0.02	0.10	-
WWDT	-	0.05	0.17	Main clock selected as clock source for the WDT.
I2C0	-	0.05	0.22	-
I2C1	-	0.05	0.18	-
SSP0	-	0.15	0.59	-
SSP1	-	0.15	0.58	-
USART0	-	0.31	1.19	-
USART1	-	0.12	0.50	-
USART2	-	0.13	0.49	-
USART3 + USART4	-	0.21	0.81	-
USB	-	0.43	0.72	Register interface disabled in SYSAHBCLKCTRL.
USB PHY	0.54	-	-	
ADC0	-	2.15	2.68	Register interface disabled in SYSAHBCLKCTRL and analog block disabled in PDRUNCFG registers. Power consumption measured while the ADC is sampling a single channel with an ADC clock of 12 MHz or 48 MHz.
Temperature sensor	0.18	-	-	-
DMA	-	0.28	1.1	-
CRC	-	0.04	0.14	-

11.4 Electrical pin characteristics

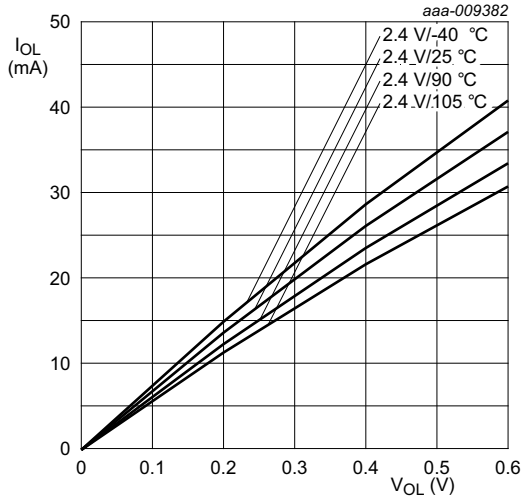


Conditions: V_{DD} = 2.4 V; ON pin PIO0_7 and PIO1_31.

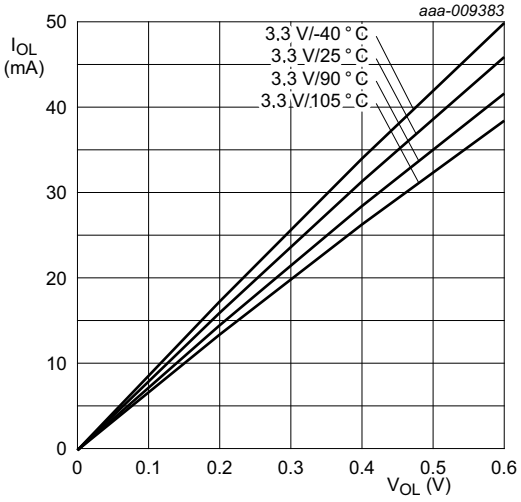


Conditions: V_{DD} = 3.3 V; ON pin PIO0_7 and PIO1_31.

Fig 23. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: V_{DD} = 2.4 V; on pins PIO0_4 and PIO0_5.



Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 24. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

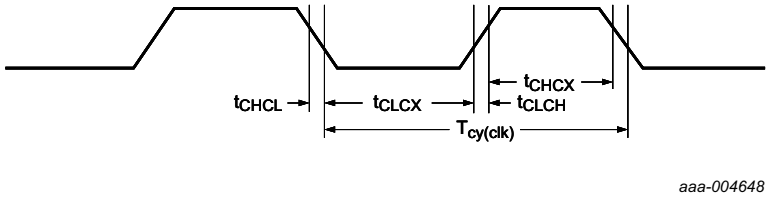


Fig 29. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.3 Internal oscillators

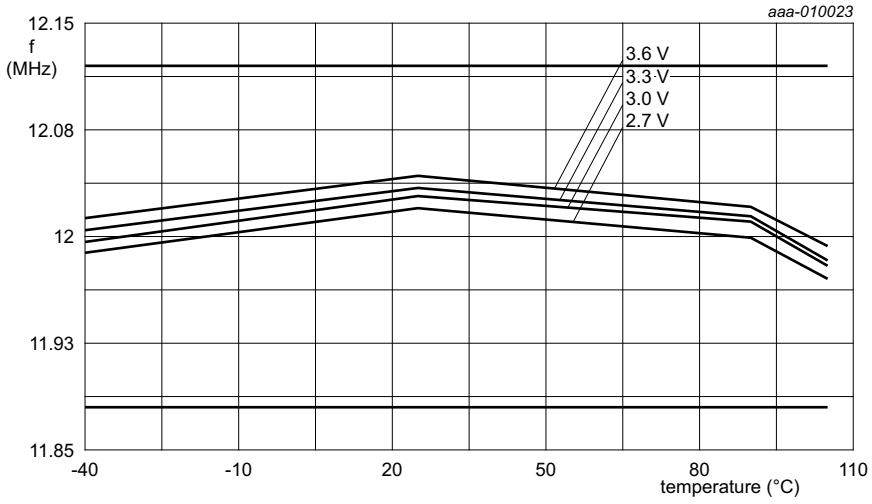
Table 13. Dynamic characteristics: IRC

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	−25 °C ≤ T_{amb} ≤ +85 °C	12 - 1%	12	12 + 1 %	MHz
		−40 °C ≤ T_{amb} < −25 °C	12 - 2%	12	12 + 1 %	MHz
		85 °C < T_{amb} ≤ 105 °C	12 - 1.5 %	12	12 + 1.5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −25 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 30. Typical Internal RC oscillator frequency versus temperature

Table 16. Dynamic characteristic: I²C-bus pins[1] …continued
T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{HD;DAT}$	data hold time [3][4][8]	Standard-mode	0	-	µs
		Fast-mode	0	-	µs
		Fast-mode Plus; on pins PIO0_4 and PIO0_5	0	-	µs
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus; on pins PIO0_4 and PIO0_5	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

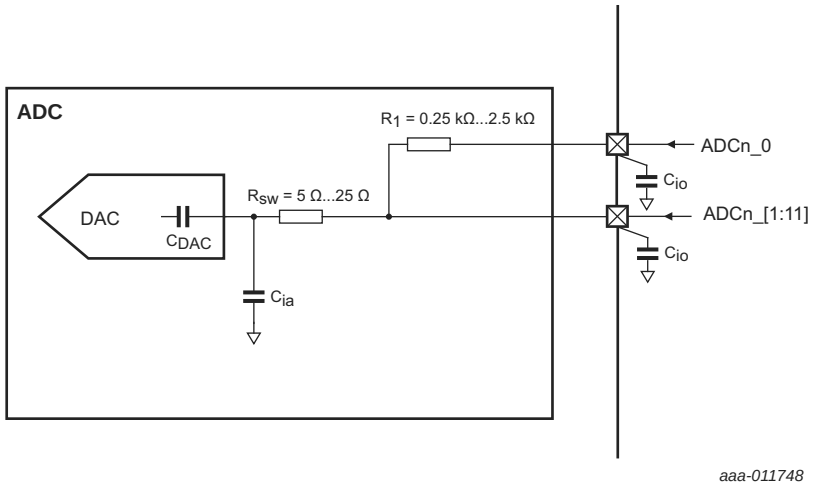


Fig 36. ADC input impedance

Table 23. Temperature sensor static and dynamic characteristics
V_{DDA} = 2.4 V to 3.6 V

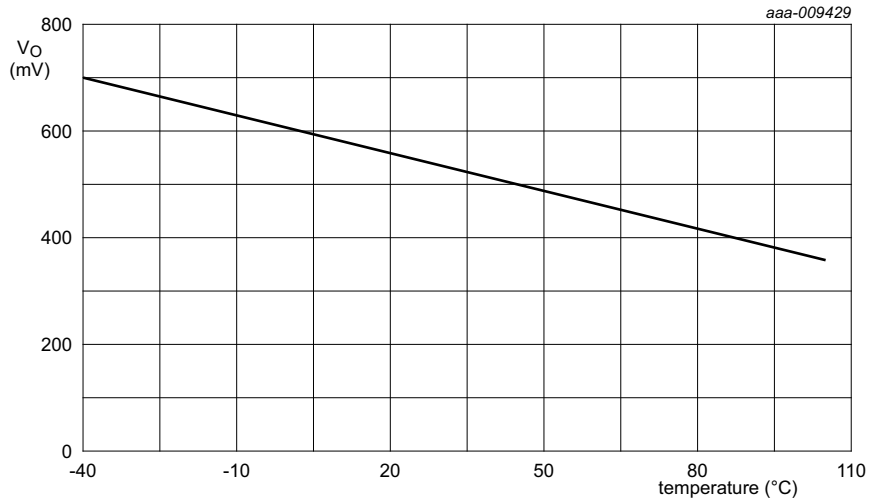
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C [1]	-	±5	-	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C	-	±4	-	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value [2]	-	14	-	µs

[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models).

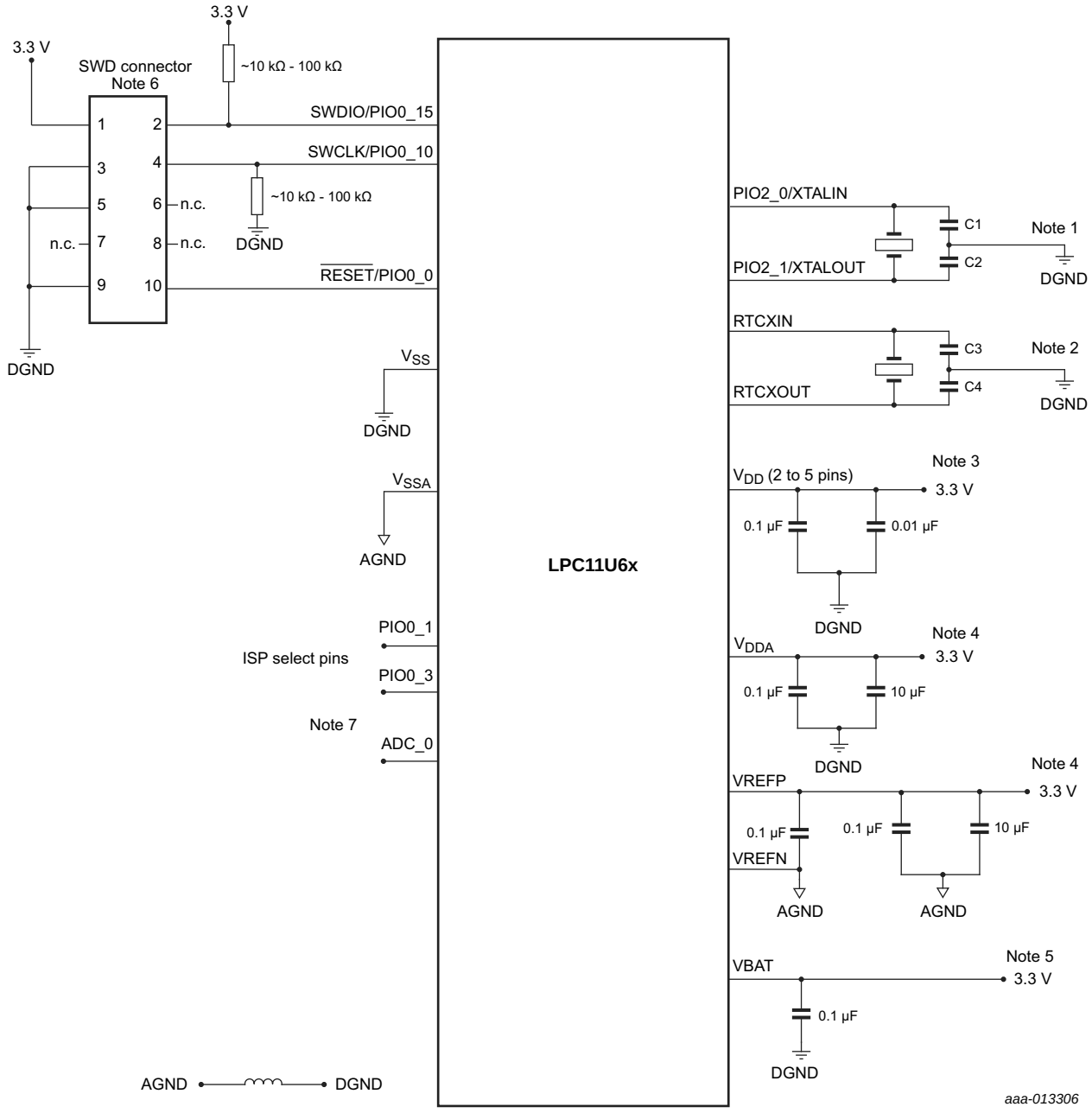
Table 24. Temperature sensor Linear-Least-Square (LLS) fit parameters
V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range	Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C	-	-2.36	-	mV/°C
LLS intercept	T_{amb} = −40 °C to +105°C	-	606	-	mV



V_{DDA} = 3.3 V; measured on a typical silicon sample.

Fig 37. Typical LLS fit of the temperature sensor output voltage



(1) See Section 14.4 “XTAL input and crystal oscillator component selection” for the values of C1 and C2.

(2) See Section 14.6 “RTC oscillator component selection” for the values of C3 and C4.

(3) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(4) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(5) Position the decoupling capacitor of 0.1 µF as close as possible to the VBAT pin. Tie VBAT to V_{DD} if not used.

(6) Uses the ARM 10-pin interface for SWD.

(7) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

Fig 44. Power, clock, and debug connections