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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u68jbd100e

- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep-sleep and Power-down modes on external pin inputs and USART activity.
  - Power-On Reset (POR).
  - Brownout detect.
- Unique device serial number for identification.
- Single power supply (2.4 V to 3.6 V).
- Separate VBAT supply for RTC.
- Operating temperature range −40 °C to 105 °C.
- Available as LQFP48, LQFP64, and LQFP100 packages.

3. Applications

- Three-phase e-meter
- GPS tracker
- Gaming accessories
- Car radio
- Medical monitor
- PC peripherals

7. Pinning information

7.1 Pinning

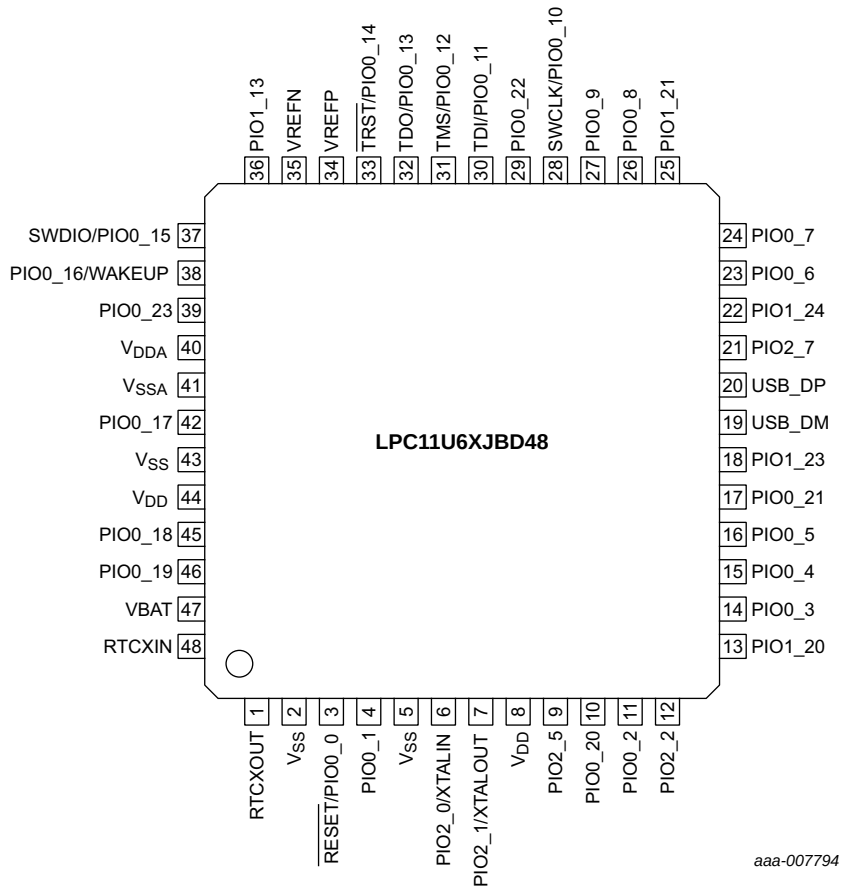


Fig 4. LQFP48 pinning

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO0_20	10	12	17	[6]	I; PU	IO	**PIO0_20 —** General-purpose digital input/output pin.
						I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
						I	**U2_RXD —** Receiver input for USART2.
PIO0_21	17	22	33	[6]	I; PU	IO	**PIO0_21 —** General-purpose digital input/output pin.
						O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
						IO	**SSP1_MOSI —** Master Out Slave In for SSP1.
PIO0_22	29	40	62	[3]	I; PU	IO	**PIO0_22 —** General-purpose digital input/output pin.
						AI	**ADC_11 —** A/D converter, input channel 11.
						I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						IO	**SSP1_MISO —** Master In Slave Out for SSP1.
PIO0_23	39	52	83	[3]	I; PU	IO	**PIO0_23 —** General-purpose digital input/output pin.
						AI	**ADC_1 —** A/D converter, input channel 1.
						-	**R_9 —** Reserved.
						I	**$\overline{\text{U0\_RI}}$ —** Ring Indicator input for USART0.
						IO	**SSP1_SSEL —** Slave select for SSP1.
PIO1_0	-	62	97	[6]	I; PU	IO	**PIO1_0 —** General-purpose digital input/output pin.
						O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
						-	**R_10 —** Reserved.
						O	**U2_TXD —** Transmitter output for USART2.
PIO1_1	-	-	28	[6]	I; PU	IO	**PIO1_1 —** General-purpose digital input/output pin.
						O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
						-	**R_11 —** Reserved.
						O	**$\overline{\text{U0\_DTR}}$ —** Data Terminal Ready output for USART0.
PIO1_2	-	-	55	[6]	I; PU	IO	**PIO1_2 —** General-purpose digital input/output pin.
						O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
						-	**R_12 —** Reserved.
						I	**U1_RXD —** Receiver input for USART1.
PIO1_3	-	-	72	[3]	I; PU	IO	**PIO1_3 —** General-purpose digital input/output pin.
						O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	**R_13 —** Reserved.
						IO	**I2C1_SDA —** I^2C-bus data input/output (not open-drain).
						AI	**ADC_5 —** A/D converter, input channel 5.
PIO1_4	-	-	23	[6]	I; PU	IO	**PIO1_4 —** General-purpose digital input/output pin.
						I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
						-	**R_14 —** Reserved.
						I	**$\overline{\text{U0\_DSR}}$ —** Data Set Ready input for USART0.

8.3 On-chip flash programming memory

The LPC11U6x contain up to 256 KB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip bootloader software.

The flash memory is divided into 24 x 4 KB and 5 x 32 KB sectors. Individual pages of 256 byte each can be erased using the IAP erase page command.

8.4 EEPROM

The LPC11U6x contain 4 KB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip bootloader software.

8.5 SRAM

The LPC11U6x contain a total of up to 36 KB on-chip static RAM memory. The main SRAM block contains either 8 KB, 16 KB, or 32 KB of main SRAM0. Two additional SRAM blocks of 2 KB (SRAM1 and USB SRAM) are located in separate areas of the memory map. See Figure 8.

8.6 On-chip ROM

The on-chip ROM contains the bootloader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM
- USB API
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- APIs to use the following peripherals:
  - I2C
  - USART0 and USART1/2/3/4
  - DMA

8.7 Memory mapping

The LPC11U6x incorporates several distinct memory regions, shown in the following figures. Figure 8 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 KB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 KB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

8.15.1 Features

- Maximum USART0 data bit rate of 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous slave and master mode.
- 16 byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.
- DMA support.

8.16 USART1/2/3/4

Remark: The LPC11U6x contains two distinctive types of UART interfaces: USART0 is software-compatible with the USART interface on the LPC11U1x/LPC11U2x/LPC11U3x parts. USART1 to USART4 use a different register interface to achieve the same UART functionality except for modem and smart card control.

Remark: USART3 and USART4 are available only on part LPC11U68JBD100.

Interrupts generated by the USART1/2/3/4 peripherals can wake up the part from Deep-sleep and power-down modes if the USART is in synchronous mode, the 32 kHz mode is enabled, or the CTS interrupt is enabled. This wake-up mechanism is not available with the USART0 peripheral.

8.16.1 Features

- Maximum bit rates of 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software-address compare feature. (RS-485 possible with software address detection and transceiver direction control.)
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.

Table 4. PWM resources *…continued*

PWM outputs			Peripheral	Pin functions available for PWM			Match registers used
LQFP100	LQFP64	LQFP48		LQFP100	LQFP64	LQFP48	
3	3	3	CT32B1	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	4
4	4	3	SCTIMER0/ PWM	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	up to 5
4	2	-	SCTIMER1/ PWM	SCT1_OUT0, SCT1_OUT1, SCT1_OUT2, SCT1_OUT3	SCT1_OUT2, SCT1_OUT3	-	up to 5

The standard timers and the SCTimers combine to up to eight independent timers. Each SCTimer can be configured either as one 32-bit timer or two independently counting 16-bit timers which use the same input clock. The following combinations are possible:

Table 5. Timer configurations

32-bit timers	Resources	16-bit timers	Resources
4	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer, SCTimer1/PWM as 32-bit timer	2	CT16B0, CT16B1
2	CT32B0, CT32B1	6	CT16B0, CT16B1, SCTimer0/PWM as two 16-bit timers, SCTimer1/PWM as two 16-bit timers
3	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer (or SCTimer1/PWM as 32-bit timer)	4	CT16B0, CT16B1, SCTimer1/PWM as two 16-bit timers (or SCTimer0/PWM as two 16-bit timers)

8.19.1 State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM)

The state configurable timer can create timed output signals such as PWM outputs triggered by programmable events. Combinations of events can be used to define timer states. The SCTimer/PWM can control the timer operations, capture inputs, change states, and toggle outputs triggered only by events entirely without CPU intervention.

If multiple states are not implemented, the SCTimer/PWM simply operates as one 32-bit or two 16-bit timers with match, capture, and PWM functions.

8.19.2 General purpose external event counter/timers (CT32B0/1 and CT16B0/1)

The LPC11U6x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.19.2.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- PWM output function.
- Match outputs and capture inputs serve as hardware triggers for ADC conversions.

8.20 System tick timer (SysTick)

The ARM Cortex-M0+ includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

8.21 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

8.21.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

- Optional warning interrupt can be generated at a programmable time before watchdog time-out.
- Software enables the WWDT, but a hardware reset or a watchdog reset/interrupt is required to disable the WWDT.
- Incorrect feed sequence causes reset or interrupt, if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDOsc). The clock source selection provides a wide range of potential timing choices of watchdog operation under different power conditions.

8.22 Real-Time Clock (RTC)

The RTC resides in a separate always-on voltage domain with battery back-up. The RTC uses an independent oscillator, also located in the always-on voltage domain.

8.22.1 Features

- 32-bit, 1 Hz RTC counter and associated match register for alarm generation.
- Separate 16-bit high-resolution/wake-up timer clocked at 1 kHz for 1 ms resolution with a more that one minute maximum time-out period.
- RTC alarm and high-resolution/wake-up timer time-out each generate independent interrupt requests. Either time-out can wake up the part from any of the low-power modes, including Deep power-down.

8.23 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the counter/timer match outputs and capture inputs and the ARM TXEV.

The ADC includes a hardware threshold compare function with zero-crossing detection.

8.23.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of up to 2 MSamples/s.
- Temperature sensor voltage output selectable as internal voltage source for channel 0.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed V_{DDA} voltage level).
- Burst conversion mode for single or multiple inputs.

8.25.3.1 Internal RC oscillator

The IRC can be used as the clock source for the WDT, the USB PLL in low-speed USB applications, or as the clock that drives the system PLL and then the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC11U6x use the IRC as the clock source. Software can later switch to one of the other available clock sources.

8.25.3.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. Use the system oscillator to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

The system oscillator has a wake-up time of approximately 500 μs.

8.25.3.3 WatchDog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 14).

8.25.3.4 RTC oscillator

The low-power RTC oscillator provides a 1 Hz clock and a 1 kHz clock to the RTC and a 32 kHz clock output that can be used to obtain the main clock (see Figure 10).

8.25.4 System PLL and USB PLL

The LPC11U6x contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

8.25.5 Clock output

The LPC11U6x feature a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

8.25.6 Wake-up process

The LPC11U6x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

8.25.7 Power control

The LPC11U6x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.25.7.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11U6x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

Remark: When using the USB, configure the LPC11U6x in Default mode.

8.25.7.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

The power profiles optimize the chip performance for power consumption or core efficiency by controlling the flash access and core power. As shown in Figure 21 and Figure 22, different power modes result in different CoreMark scores reflecting the trade-off of efficiency and power consumption. In CPU and efficiency modes, the power profiles aim to keep the core efficiency at a maximum for the given system frequency. Depending on optimal flash access parameters that change with frequency, the CoreMark score and also the power consumption change. Since the compiled code for CoreMark testing runs out of flash memory, the CoreMark score depends on the compiler version.

11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed except for the ADC. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

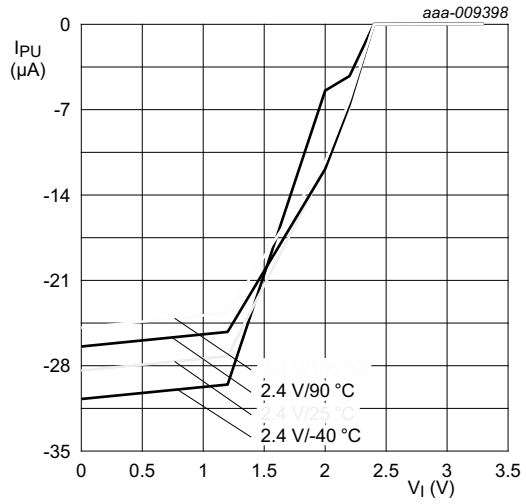
The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 9. Power consumption for individual analog and digital blocks

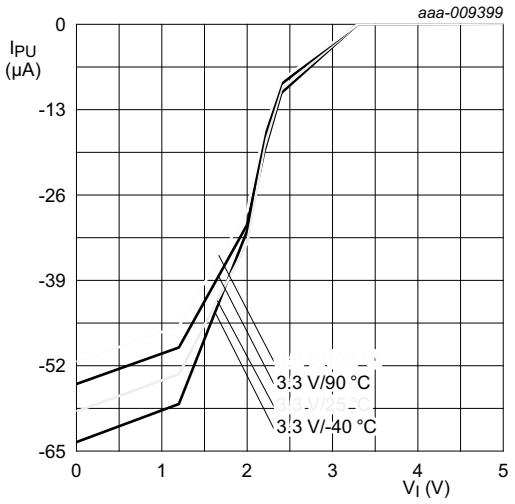
Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.24	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.28	-	-	IRC running; PLL off; independent of main clock frequency.
WatchDog oscillator at 600 kHz/2	0	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.05	-	-	Independent of main clock frequency.
System PLL	0.25	-	-	-
USB PLL	0.37	-	-	-
CLKOUT	-	0.25	0.89	System PLL is source of CLKOUT.
ROM	-	0.09	0.37	-
FLASHREG	-	0.17	0.66	-
FLASHARRAY	-	0.13	0.52	-
SRAM1	-	0.15	0.59	-
USB SRAM	-	0.14	0.56	-
GPIO + pin interrupt/pattern match	-	0.18	0.69	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCON	-	0.08	0.30	-
SCTimer0/PWM + SCTimer1/PWM	-	0.29	1.1	-
CT16B0	-	0.05	0.17	-
CT16B1	-	0.04	0.16	-
CT32B0	-	0.04	0.13	-
CT32B1	-	0.03	0.13	-

Table 9. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
RTC	-	0.02	0.10	-
WWDT	-	0.05	0.17	Main clock selected as clock source for the WDT.
I2C0	-	0.05	0.22	-
I2C1	-	0.05	0.18	-
SSP0	-	0.15	0.59	-
SSP1	-	0.15	0.58	-
USART0	-	0.31	1.19	-
USART1	-	0.12	0.50	-
USART2	-	0.13	0.49	-
USART3 + USART4	-	0.21	0.81	-
USB	-	0.43	0.72	Register interface disabled in SYSAHBCLKCTRL.
USB PHY	0.54	-	-	
ADC0	-	2.15	2.68	Register interface disabled in SYSAHBCLKCTRL and analog block disabled in PDRUNCFG registers. Power consumption measured while the ADC is sampling a single channel with an ADC clock of 12 MHz or 48 MHz.
Temperature sensor	0.18	-	-	-
DMA	-	0.28	1.1	-
CRC	-	0.04	0.14	-

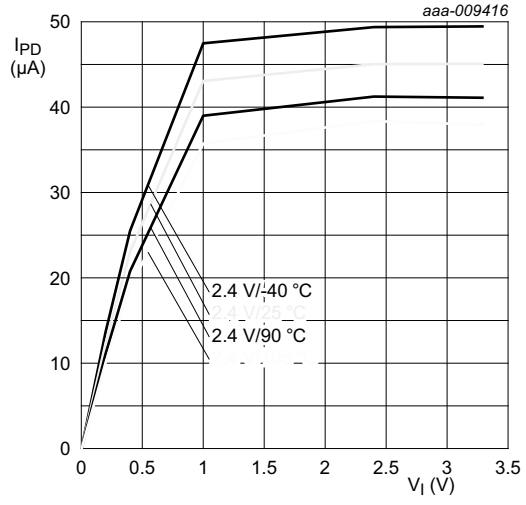


Conditions: V_{DD} = 2.4 V; standard port pins.

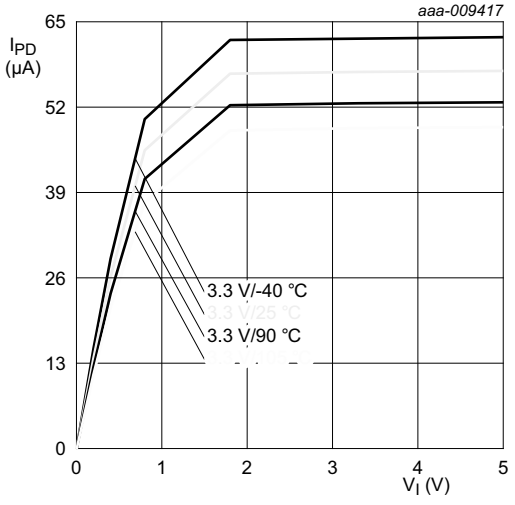


Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 27. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 2.4 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 28. Typical pull-down current I_{PD} versus input voltage V_I

Table 14. Dynamic characteristics: WatchDog oscillator

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; [2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register [2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] See the LPC11U6x *user manual.*

12.4 I/O pins

Table 15. Dynamic characteristics: I/O pins[1]
T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.5 I²C-bus

Table 16. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus; on pins PIO0_4 and PIO0_5	0	1	MHz
t_f	fall time [4][5][6][7]	of both SDA and SCL signals	-	300	ns
		Standard-mode			
		Fast-mode	20 + 0.1 × C_b	300	ns
		Fast-mode Plus; on pins PIO0_4 and PIO0_5	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	µs
		Fast-mode	1.3	-	µs
		Fast-mode Plus; on pins PIO0_4 and PIO0_5	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	µs
		Fast-mode	0.6	-	µs
		Fast-mode Plus; on pins PIO0_4 and PIO0_5	0.26	-	µs

12.7 USART interface

The maximum USART bit rate for all USARTs is 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous slave and master mode.

Table 18. USART dynamic characteristics USART0

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Min	Max	Unit
$T_{cy(clk)}$	clock cycle time [1]	100	-	ns
USART master (in synchronous mode)				
$t_{su(D)}$	data input set-up time	44	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	10	ns
$t_{h(Q)}$	data output hold time	0	-	ns
USART slave (in synchronous mode)				
$t_{su(D)}$	data input set-up time	5	-	ns
$t_{h(D)}$	data input hold time	20	-	ns
$t_{v(Q)}$	data output valid time	-	40	ns
$t_{h(Q)}$	data output hold time	25	-	ns

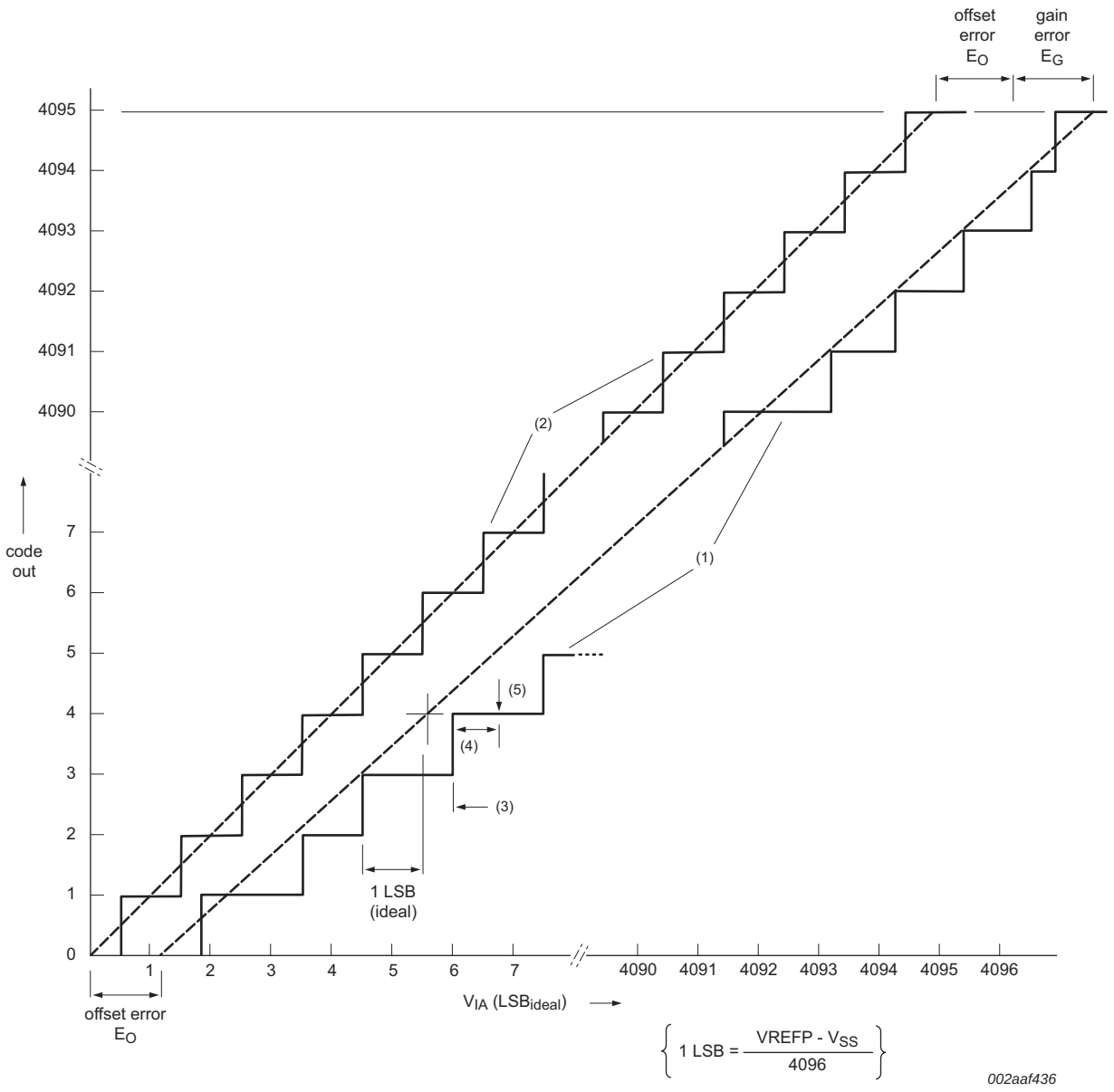
[1] $T_{cy(clk)}$ = (main clock cycle time)/(UARTCLKDIV x 2 x (256 x DLM + DLL)). See the LPC11U6x *User manual UM10732*.

Table 19. USART dynamic characteristics USART1/2/3/4

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Min	Max	Unit
$T_{cy(clk)}$	clock cycle time [1]	100	-	ns
USART master (in synchronous mode)				
$t_{su(D)}$	data input set-up time	44	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	10	ns
$t_{h(Q)}$	data output hold time	0	-	ns
USART slave (in synchronous mode)				
$t_{su(D)}$	data input set-up time	5	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	40	ns
$t_{h(Q)}$	data output hold time	20	-	ns

[1] $T_{cy(clk)}$ = U_PCLK/BRGVAL. See the LPC11U6x *User manual UM10732*.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 35. 12-bit ADC characteristics

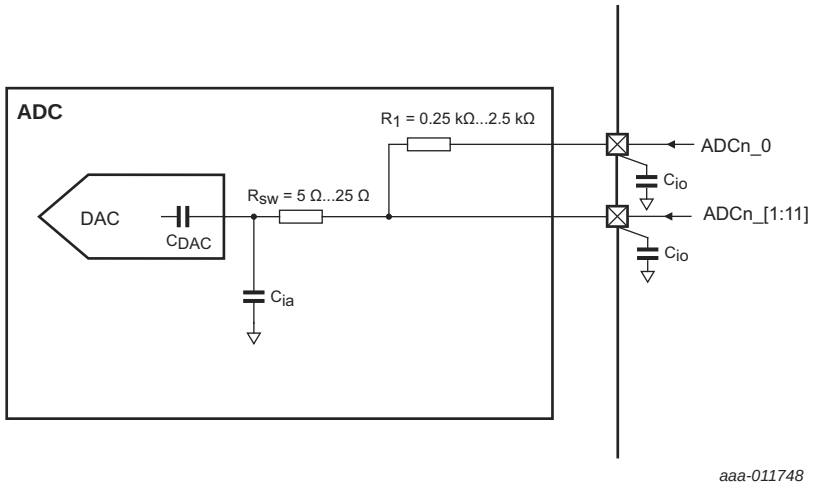


Fig 36. ADC input impedance

Table 23. Temperature sensor static and dynamic characteristics
V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C [1]	-	±5	-	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C	-	±4	-	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value [2]	-	14	-	µs

[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models).

Table 24. Temperature sensor Linear-Least-Square (LLS) fit parameters
V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range	Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C	-	-2.36	-	mV/°C
LLS intercept	T_{amb} = −40 °C to +105°C	-	606	-	mV

External components and models used in oscillation mode are shown in Figure 42 and in Table 26 and Table 27. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} must be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 42 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 26).

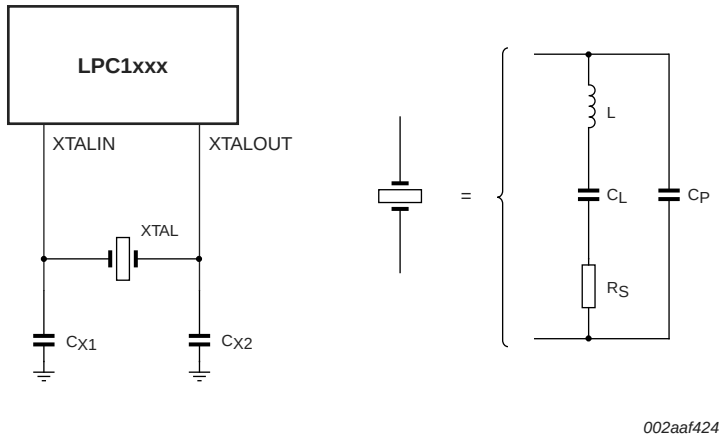


Fig 42. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

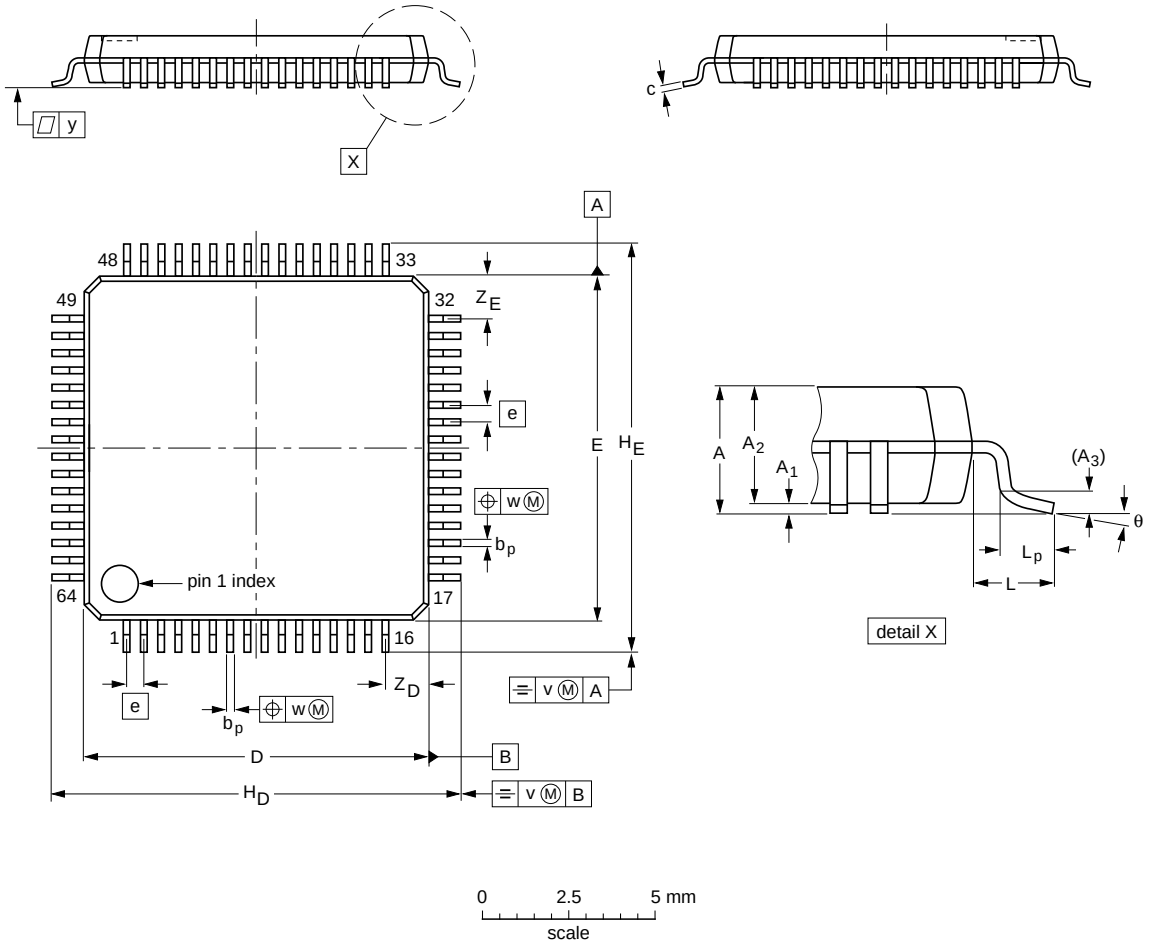
Table 26. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 27. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 46. Package outline LQFP64 (SOT314-2)

18. Revision history

Table 31. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11U6x v.1.3	20160907	Product data sheet	-	LPC11U6x v.1.2
Modifications:	• Section 14.10 “ElectroMagnetic Compatibility (EMC)” added. • Replaced CT16B0_CAP1 with CT16B0_CAP2 for pin PI01_21. See Table 3 “Pin description”. • Replaced CT32B0_CAP1 with CT32B0_CAP2 for pin PIO1_6 and pin PIO1_29. See Table 3 “Pin description”. • Updated Figure 7 “AHB multilayer matrix”: HS GPIO connects with M0+ Core, not with DMA or USB.			
LPC11U6x v.1.2	20140526	Product data sheet	-	LPC11U6x v.1.1
Modifications:	• Part marking updated with revision indicator. • Changed recommendation for VBAT connection if unused: Tie to VDD. See Table 3 “Pin description”. • Section 14.7 “Connecting power, clocks, and debug functions” added. • Section 14.9 “Pin states in different power modes” added. • Remark added about using the regulator in the USB bus-powered set-up. See Section 14.3 “Suggested USB interface solutions”. • Figure 39 “USB interface on a bus-powered device” changed to show USB_VBUS connection to part. • Parts added: LPC11U67JBD100, LPC11U67JBD64, LPC11U66JBD48.			
LPC11U6x v.1.1	20140312	Product data sheet	-	LPC11U6x v.1
Modifications:	• Parameter R_I renamed to Z_I (input impedance) in Table 22. • Description of the internal USB_CONNECT function clarified in Section 14.3 “Suggested USB interface solutions”. The USB_CONNECT function can be set internally by software and does not require external circuitry. • Parameter Cia corrected in Table 22 “12-bit ADC static characteristics”. • Figure 36 “ADC input impedance” added. • Parameter pin capacitance added in Table 8. • Pin description for VBAT updated: If no battery is used, tie VBAT to VDD or to ground. See Table 3. • Pin description for $\overline{\text{RESET}}$/PIO0_0 updated: In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed. See Table 3. • Pin functions TMS, TDI, TDO, and $\overline{\text{TRST}}$ changed to default function in Table 3. • Pin description table updated for clarity (VBAT, I2C-bus pins, WAKEUP pin). • Section 14.1 “ADC usage notes” added. • Use of USB_CONNECT signal explained when VBUS is not connected. See Section 14.3.			
LPC11U6x v.1	20140117	Product data sheet	-	-