Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11u68jbd64e

- Power profiles.
- Flash In-Application Programming (IAP) and In-System Programming (ISP).
- 32-bit integer division routines.

- Digital peripherals:
  - Simple DMA engine with 16 channels and programmable input triggers.
  - High-speed GPIO interface connected to the ARM Cortex-M0+ IO bus with up to 80 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and programmable glitch filter and digital filter.
  - Pin interrupt and pattern match engine using eight selectable GPIO pins.
  - Two GPIO group interrupt generators.
  - CRC engine.
- Configurable PWM/timer subsystem (two 16-bit and two 32-bit standard counter/timers, two State-Configurable Timers (SCTimer/PWM)) that provides:
  - Up to four 32-bit and two 16-bit counter/timers or two 32-bit and six 16-bit counter/timers.
  - Up to 21 match outputs and 16 capture inputs.
  - Up to 19 PWM outputs with 6 independent time bases.
- Windowed WatchDog timer (WWDT).
- Real-time Clock (RTC) in the always-on power domain with separate battery supply pin and 32 kHz oscillator.
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 2 Msamples/s. The ADC supports two independent conversion sequences.
  - Temperature sensor.
- Serial interfaces:
  - Up to five USART interfaces, all with DMA, synchronous mode, and RS-485 mode support. Four USARTs use a shared fractional baud generator.
  - Two SSP controllers with DMA support.
  - Two I^2C-bus interfaces. One I^2C-bus interface with specialized open-drain pins supports I2C Fast-mode plus.
  - USB 2.0 full-speed device controller with on-chip PHY. XTAL-less low-speed mode supported.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - On-chip 32 kHz oscillator for RTC.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz. Oscillator pins are shared with the GPIO pins.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal.
  - A second, dedicated PLL is provided for USB.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO0_6	23	29	44	[6]	I; PU	IO	**PIO0_6 —** General-purpose port 0 input/output 6.
						-	**R —** Reserved.
						IO	**SSP0_SCK —** Serial clock for SSP0.
						-	**R_4 —** Reserved.
PIO0_7	24	30	45	[5]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7 (high-current output driver).
						I	**$\overline{\text{U0\_CTS}}$ —** Clear To Send input for USART.
						-	**R_5 —** Reserved.
						IO	**I2C1_SCL —** I^2C-bus clock input/output. This pin is not open-drain.
PIO0_8	26	37	58	[6]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8.
						IO	**SSP0_MISO —** Master In Slave Out for SSP0.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	**R_6 —** Reserved.
PIO0_9	27	38	59	[6]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9.
						IO	**SSP0_MOSI —** Master Out Slave In for SSP0.
						O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
						-	**R_7 —** Reserved.
SWCLK/PIO0_10	28	39	60	[6]	I; PU	IO	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
						IO	**PIO0_10 —** General-purpose digital input/output pin.
						IO	**SSP0_SCK —** Serial clock for SSP0.
						O	**CT16B0_MAT2 —** 16-bit timer0 MAT2
TDI/PIO0_11	30	42	64	[3]	I; PU	IO	**TDI —** Test Data In for JTAG interface. In boundary scan mode only.
						IO	**PIO0_11 —** General-purpose digital input/output pin.
						AI	**ADC_9 —** A/D converter, input channel 9.
						O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
						O	**$\overline{\text{U1\_RTS}}$ —** Request To Send output for USART1.
						IO	**U1_SCLK —** Serial clock input/output for USART1 in synchronous mode.
TMS/PIO0_12	31	43	66	[3]	I; PU	IO	**TMS —** Test Mode Select for JTAG interface. In boundary scan mode only.
						IO	**PIO0_12 —** General-purpose digital input/output pin.
						AI	**ADC_8 —** A/D converter, input channel 8.
						I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
						I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART3 and USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO1_5	-	-	47	[6]	I; PU	IO	**PIO1_5 —** General-purpose digital input/output pin.
						I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
						-	**R_15 —** Reserved.
						I	**$\overline{\text{U0\_DCD}}$ —** Data Carrier Detect input for USART0.
PIO1_6	-	-	98	[6]	I; PU	IO	**PIO1_6 —** General-purpose digital input/output pin.
						-	**R_16 —** Reserved.
						I	**U2_RXD —** Receiver input for USART2.
						I	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.
PIO1_7	-	6	10	[6]	I; PU	IO	**PIO1_7 —** General-purpose digital input/output pin.
						-	**R_17 —** Reserved.
						I	**$\overline{\text{U2\_CTS}}$ —** Clear To Send input for USART2.
						I	**CT16B1_CAP0 —** Capture input 0 for 32-bit timer 1.
PIO1_8	-	-	61	[6]	I; PU	IO	**PIO1_8 —** General-purpose digital input/output pin.
						-	**R_18 —** Reserved.
						O	**U1_TXD —** Transmitter output for USART1.
						I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO1_9	-	55	86	[3]	I; PU	IO	**PIO1_9 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U0\_CTS}}$ —** Clear To Send input for USART0.
						O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
						I	**ADC_0 —** A/D converter, input channel 0.
PIO1_10	-	13	18	[6]	I; PU	IO	**PIO1_10 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U2\_RTS}}$ —** Request To Send output for USART2.
						IO	**U2_SCLK —** Serial clock input/output for USART2 in synchronous mode.
						O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_11	-	-	65	[6]	I; PU	IO	**PIO1_11 —** General-purpose digital input/output pin.
						IO	**I2C1_SCL —** I^2C1-bus clock input/output (not open-drain).
						O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
						I	**$\overline{\text{U0\_RI}}$ —** Ring Indicator input for USART0.
PIO1_12	-	-	89	[6]	I; PU	IO	**PIO1_12 —** General-purpose digital input/output pin.
						IO	**SSP0_MOSI —** Master Out Slave In for SSP0.
						O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
						-	**R_21 —** Reserved.
PIO1_13	36	49	78	[6]	I; PU	IO	**PIO1_13 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U1\_CTS}}$ —** Clear To Send input for USART1.
						O	**SCT0_OUT3 —** SCTimer0/PWM output 3.
						-	**R_22 —** Reserved.

- Digital filter with programmable filter constant on all pins. The minimum filter constant is 1/50 MHz = 20 ns.

8.9.2 Standard I/O pad configuration

Figure 9 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input digital filter selectable on all pins. In addition, a 10 ns digital glitch filter is selectable on pins with analog function.
- Analog input

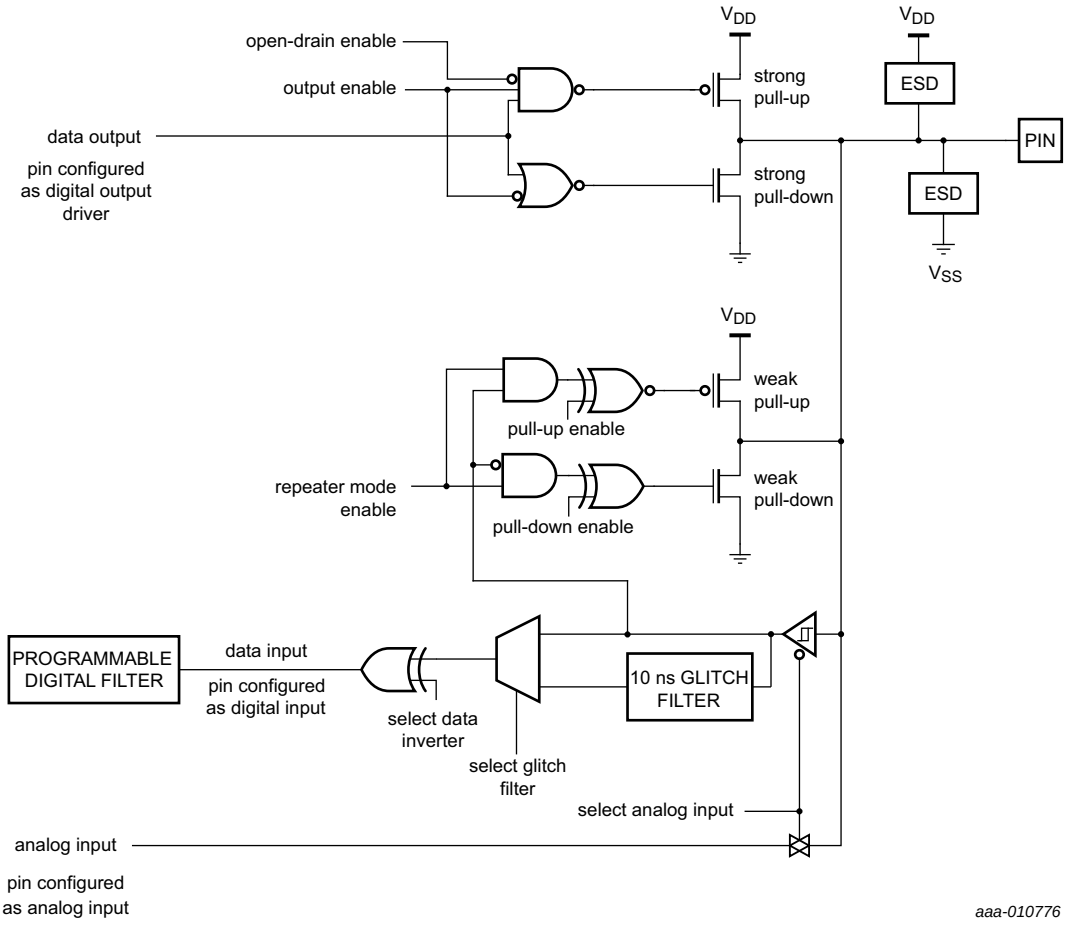


Fig 9. Standard I/O pin configuration

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC11U6x use accelerated GPIO functions:

- GPIO registers are on the ARM Cortex M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 25 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin except pins PIO2_8 and PIO2_23 can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins except pins PIO2_8 and PIO2_23 as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the part from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to 8 pins can be selected from all digital pins except pins PIO2_8 and PIO2_23 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to generate an RXEV notification to the ARM CPU as well.
  - The pattern match engine does not facilitate wake-up.

Table 4. PWM resources *…continued*

PWM outputs			Peripheral	Pin functions available for PWM			Match registers used
LQFP100	LQFP64	LQFP48		LQFP100	LQFP64	LQFP48	
3	3	3	CT32B1	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	4
4	4	3	SCTIMER0/ PWM	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	up to 5
4	2	-	SCTIMER1/ PWM	SCT1_OUT0, SCT1_OUT1, SCT1_OUT2, SCT1_OUT3	SCT1_OUT2, SCT1_OUT3	-	up to 5

The standard timers and the SCTimers combine to up to eight independent timers. Each SCTimer can be configured either as one 32-bit timer or two independently counting 16-bit timers which use the same input clock. The following combinations are possible:

Table 5. Timer configurations

32-bit timers	Resources	16-bit timers	Resources
4	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer, SCTimer1/PWM as 32-bit timer	2	CT16B0, CT16B1
2	CT32B0, CT32B1	6	CT16B0, CT16B1, SCTimer0/PWM as two 16-bit timers, SCTimer1/PWM as two 16-bit timers
3	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer (or SCTimer1/PWM as 32-bit timer)	4	CT16B0, CT16B1, SCTimer1/PWM as two 16-bit timers (or SCTimer0/PWM as two 16-bit timers)

8.19.1 State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM)

The state configurable timer can create timed output signals such as PWM outputs triggered by programmable events. Combinations of events can be used to define timer states. The SCTimer/PWM can control the timer operations, capture inputs, change states, and toggle outputs triggered only by events entirely without CPU intervention.

If multiple states are not implemented, the SCTimer/PWM simply operates as one 32-bit or two 16-bit timers with match, capture, and PWM functions.

8.25 Clocking and power control

8.25.1 Clock generation

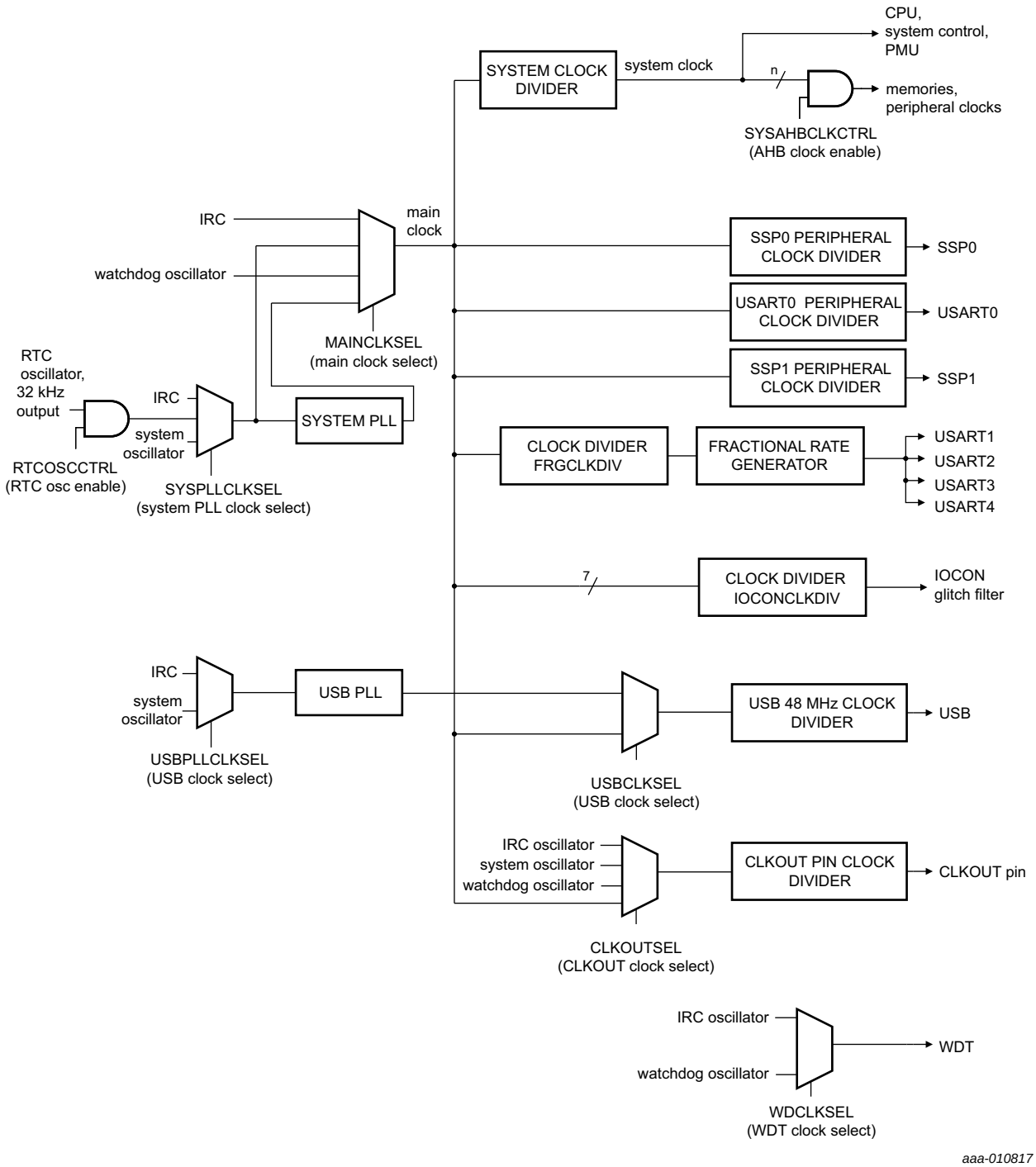


Fig 10. Clock generation

8.25.6 Wake-up process

The LPC11U6x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

8.25.7 Power control

The LPC11U6x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.25.7.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11U6x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

Remark: When using the USB, configure the LPC11U6x in Default mode.

8.25.7.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values. The internal reset status is reflected on the RSTOUT pin.

In Deep power-down mode, an external pull-up resistor is required on the RESET pin.

The RESET pin is operational in active, sleep, deep-sleep, and power-down modes if the RESET function is selected in the IOCON register for pin PIO0_0 (this is the default). A LOW-going pulse as short as 50 ns executes the reset and also wakes up the part if in sleep, deep-sleep or power-down mode. The RESET pin is not functional in Deep power-down mode.

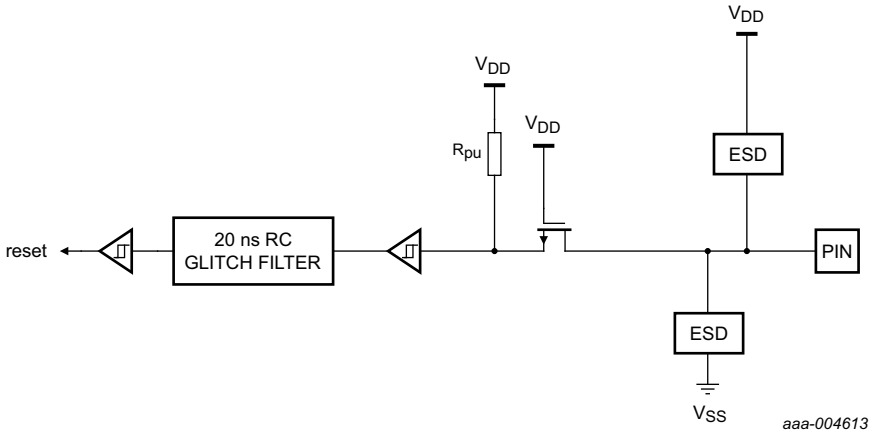


Fig 12. RESET pin configuration

8.26.2 Brownout detection

The LPC11U6x includes two levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Two threshold levels can be selected to cause a forced reset of the chip.

8.26.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details, see the *LPC11Uxx user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC11U6x user manual*.

8.27 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC11U6x is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

Table 8. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 12 mA; 2.4 V ≤ V_{DD} < 2.5 V	V_{DD} − 0.4	-	-	V
		I_{OH} = 20 mA; 2.5 V ≤ V_{DD} < 3.6 V	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.4 V ≤ V_{DD} < 2.5 V	12	-	-	mA
		V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} < 3.6 V	20	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [16]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [16]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V [17]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V [17]	−10	−50	−85	µA
		V_{DD} < V_I < 5 V	0	0	0	µA
I^2C-bus pins (PIO0_4 and PIO0_5); see Figure 13						
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage		0.05 V_{DD}	-	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins	3.5	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins	20	-	-	mA
I_{LI}	input leakage current	V_I = V_{DD} [18]	-	2	4	µA
		V_I = 5 V	-	10	22	µA
USB_DM and USB_DP pins						
V_I	input voltage	[2]	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		1.5	-	-	V
V_{IL}	LOW-level input voltage		-	-	1.3	V
V_{hys}	hysteresis voltage		0.32	-	-	V
Z_{out}	output impedance		28	-	44	Ω
V_{OH}	HIGH-level output voltage	With 15 kΩ resistor to ground	2.9	-	-	V
V_{OL}	LOW-level output voltage	With internal 1.5 kΩ resistor to 3.6 V pull-up enabled	-	-	0.18	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.3 V [19]	4.8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.3 V [19]	5.0	-	-	mA

The power profiles optimize the chip performance for power consumption or core efficiency by controlling the flash access and core power. As shown in Figure 21 and Figure 22, different power modes result in different CoreMark scores reflecting the trade-off of efficiency and power consumption. In CPU and efficiency modes, the power profiles aim to keep the core efficiency at a maximum for the given system frequency. Depending on optimal flash access parameters that change with frequency, the CoreMark score and also the power consumption change. Since the compiled code for CoreMark testing runs out of flash memory, the CoreMark score depends on the compiler version.

11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed except for the ADC. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 9. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.24	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.28	-	-	IRC running; PLL off; independent of main clock frequency.
WatchDog oscillator at 600 kHz/2	0	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.05	-	-	Independent of main clock frequency.
System PLL	0.25	-	-	-
USB PLL	0.37	-	-	-
CLKOUT	-	0.25	0.89	System PLL is source of CLKOUT.
ROM	-	0.09	0.37	-
FLASHREG	-	0.17	0.66	-
FLASHARRAY	-	0.13	0.52	-
SRAM1	-	0.15	0.59	-
USB SRAM	-	0.14	0.56	-
GPIO + pin interrupt/pattern match	-	0.18	0.69	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCON	-	0.08	0.30	-
SCTimer0/PWM + SCTimer1/PWM	-	0.29	1.1	-
CT16B0	-	0.05	0.17	-
CT16B1	-	0.04	0.16	-
CT32B0	-	0.04	0.13	-
CT32B1	-	0.03	0.13	-

Table 22. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 2.4 V to 3.6 V; VREFP = V_{DDA}; V_{SSA} = 0; VREFN = V_{SSA}. ADC calibrated at T = 25 °C.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{IA}	analog input voltage	[2]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance	[3]	-	-	0.32	pF
$f_{clk(ADC)}$	ADC clock frequency	$V_{DDA} \geq 2.7$ V			50	MHz
		$V_{DDA} \geq 2.4$ V			25	MHz
f_s	sampling frequency	$V_{DDA} \geq 2.7$ V	-	-	2	Msamples/s
		$V_{DDA} \geq 2.4$ V	-	-	1	Msamples/s
E_D	differential linearity error	[4]	-	-	±2.5	LSB
$E_{L(adj)}$	integral non-linearity	[5]	-	-	±2.5	LSB
E_O	offset error	[6]	-	-	±4.5	LSB
$V_{err(FS)}$	full-scale error voltage	[7]	-	-	±0.5	%
Z_i	input impedance	f_s = 2 Msamples/s [8][9]	0.1	-	-	MΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The input resistance of ADC channel 0 is higher than for all other channels.

[3] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 2 Msamples/s.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 35.

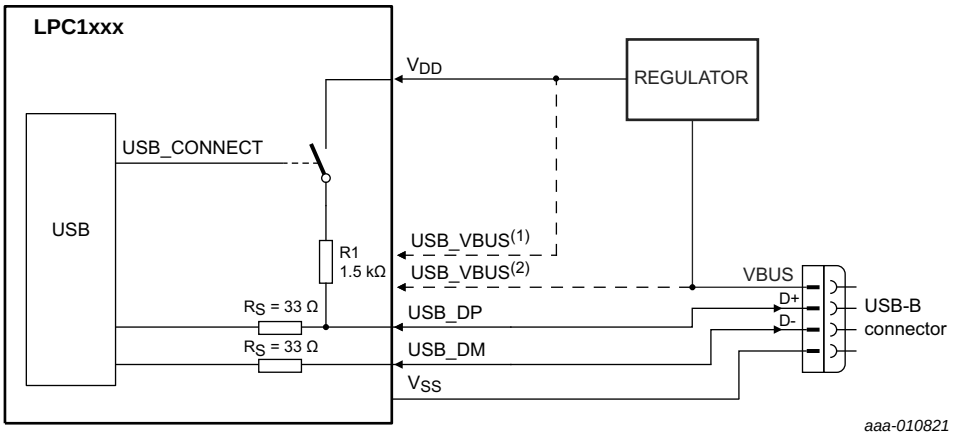
[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 35.

[6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 35.

[7] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 35.

[8] T_{amb} = 25 °C; maximum sampling frequency f_s = 2 Msamples/s and analog input capacitance C_{ia} = 0.32 pF.

[9] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 8 for C_{io}.



Two options exist for connecting VBUS to the USB_VBUS pin:

(1) Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.

(2) Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to supply V_{DD}. Since the PIO0_3/USB_VBUS pin is only 5 V tolerant when V_{DD} is at operating level, this connection can degrade the performance of the part over its lifetime. Simulation shows that lifetime is reduced to 15 years at T_{amb} = 45 °C and 8 years at T_{amb} = 55 °C assuming that USB_VBUS = 5 V is applied continuously while V_{DD} = 0 V.

Fig 39. USB interface on a bus-powered device

Remark: When a self-powered circuit is used without connecting VBUS, configure the PIO0_3/USB_VBUS pin for GPIO (PIO0_3) and provide software that can detect the host presence through some other mechanism before enabling USB_CONNECT and the SoftConnect feature. Enabling the SoftConnect without host presence leads to USB compliance failure.

14.3.1 USB Low-speed operation

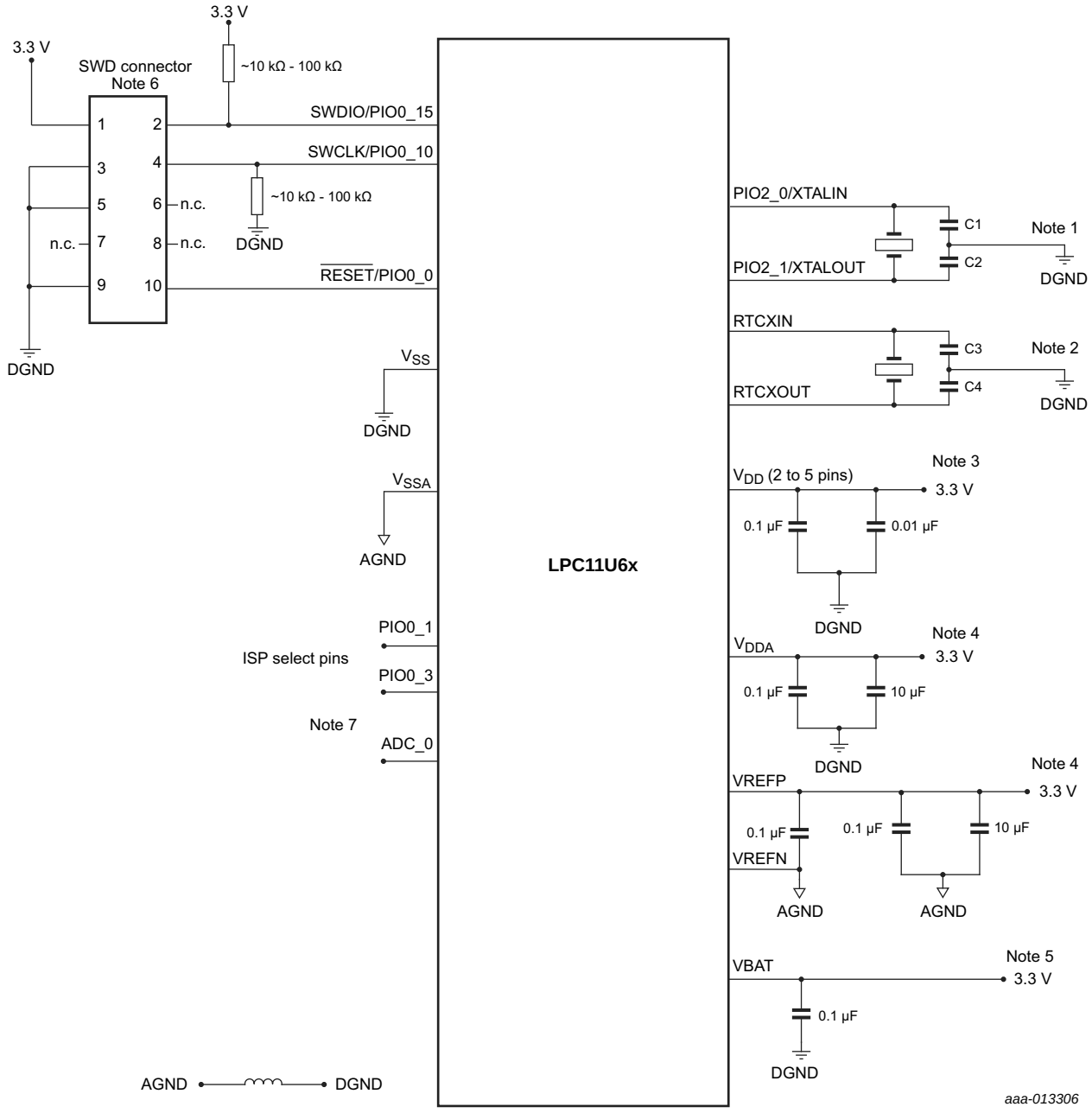
The USB device controller can be used in low-speed mode supporting 1.5 Mbit/s data exchange with a USB host controller.

Remark: To operate in low-speed mode, change the board connections as follows:

1. Connect USB_DP to the D- pin of the connector.
2. Connect USB_DM to the D+ pin of the connector.

Use the IRC as clock source for the USB PLL to generate 48 MHz, then set the USB clock divider USBCLKDIV to 8 for a 6 MHz USB clock (see Figure 10 “Clock generation”).

External 10 Ω resistors are recommended in low-speed mode to reduce over-shoots and accommodate for 5 m cable length required for USB-IF testing.



(1) See Section 14.4 “XTAL input and crystal oscillator component selection” for the values of C1 and C2.

(2) See Section 14.6 “RTC oscillator component selection” for the values of C3 and C4.

(3) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(4) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(5) Position the decoupling capacitor of 0.1 µF as close as possible to the VBAT pin. Tie VBAT to V_{DD} if not used.

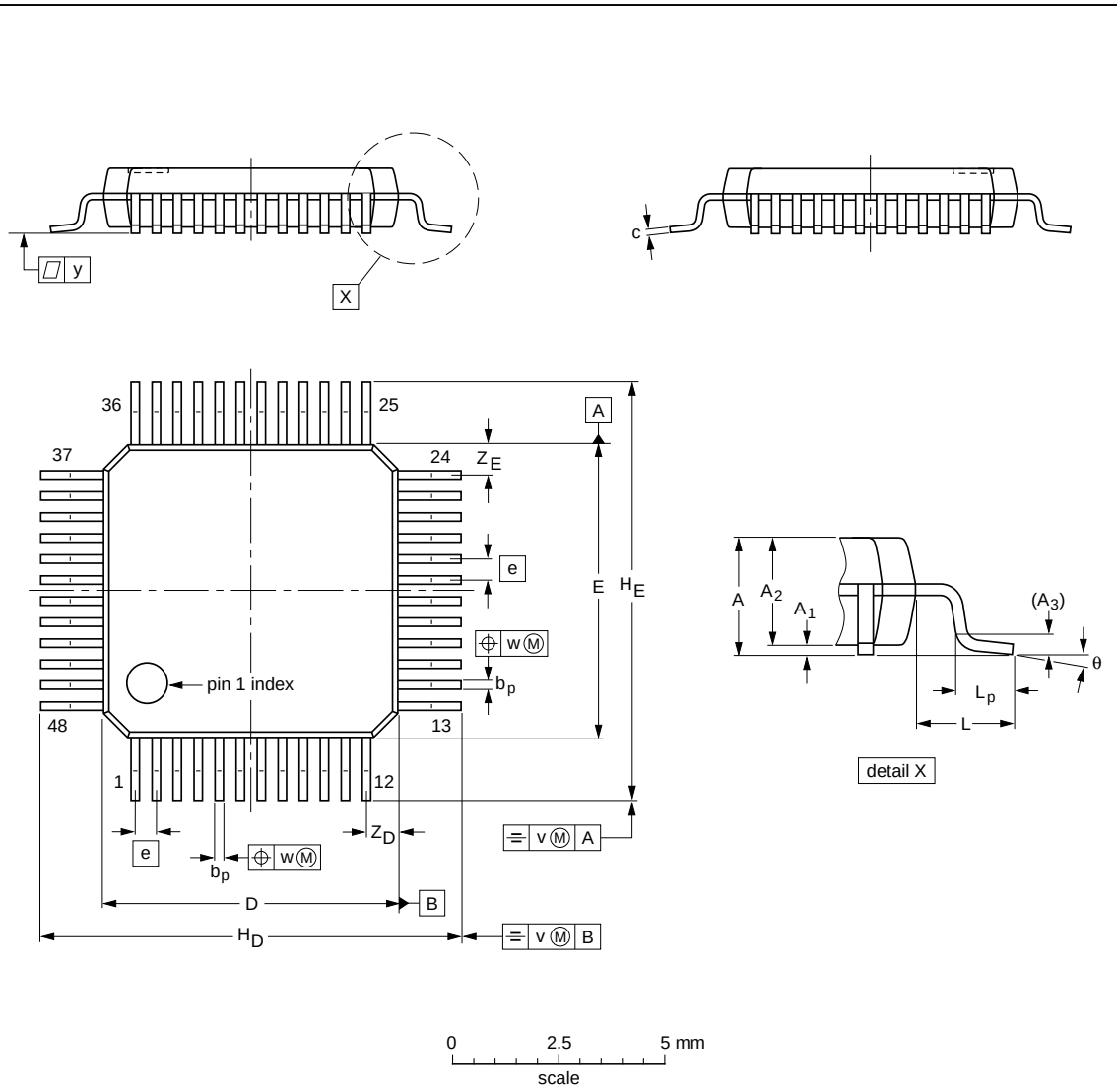
(6) Uses the ARM 10-pin interface for SWD.

(7) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

Fig 44. Power, clock, and debug connections

15. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

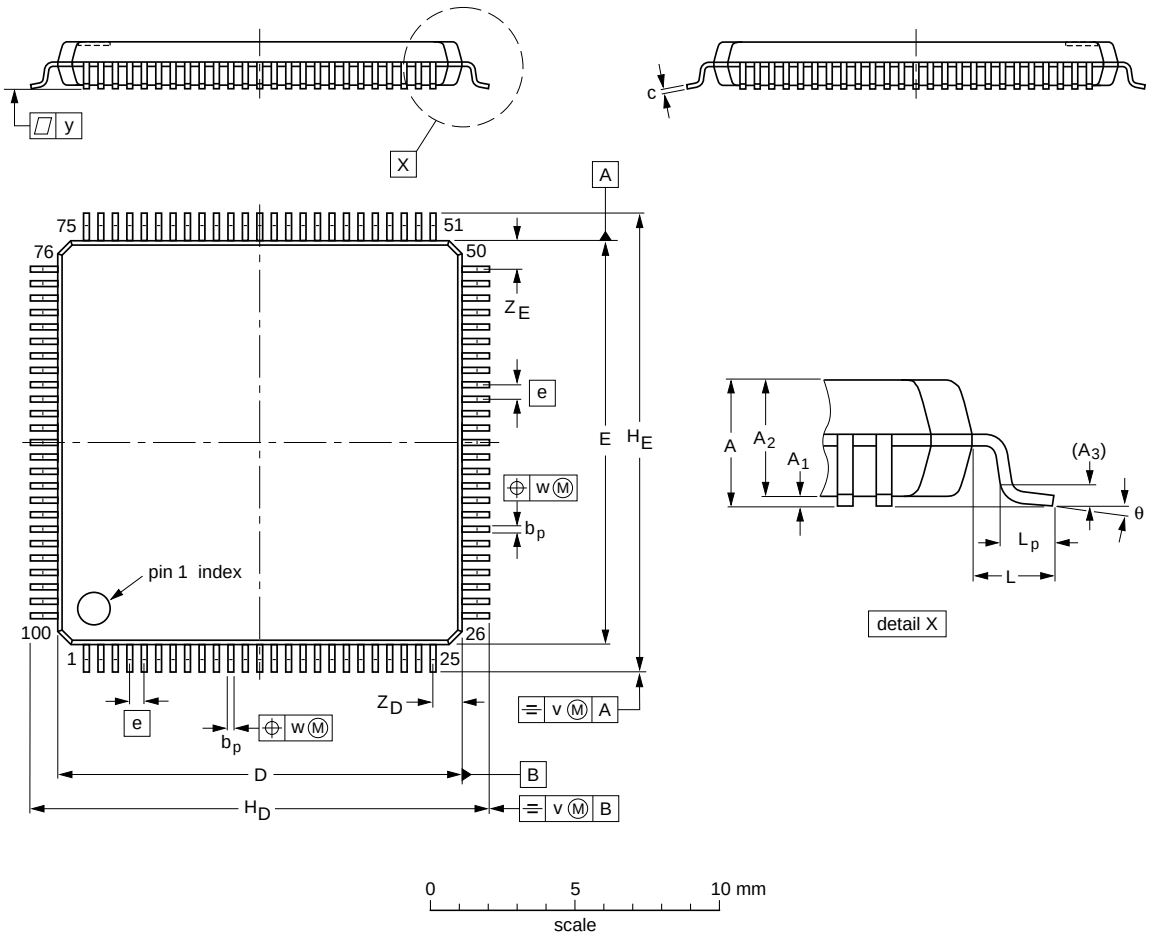
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 45. Package outline LQFP48 (SOT313-2)

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 47. Package outline LQFP100 (SOT407-1)

21. Contents

1 General description 1
2 Features and benefits 1
3 Applications 3
4 Ordering information 4
4.1 Ordering options 4
5 Marking 5
6 Block diagram 6
7 Pinning information 7
7.1 Pinning 7
7.2 Pin description 9
8 Functional description 19
8.1 ARM Cortex-M0+ core 19
8.2 AHB multilayer matrix 19
8.3 On-chip flash programming memory 21
8.4 EEPROM 21
8.5 SRAM 21
8.6 On-chip ROM 21
8.7 Memory mapping 21
8.8 Nested Vectored Interrupt Controller (NVIC) . 22
8.8.1 Features 23
8.8.2 Interrupt sources 23
8.9 IOCON block 23
8.9.1 Features 23
8.9.2 Standard I/O pad configuration 24
8.10 Fast General-Purpose parallel I/O (GPIO) . . . 24
8.10.1 Features 25
8.11 Pin interrupt/pattern match engine 25
8.11.1 Features 25
8.12 GPIO group interrupts 26
8.12.1 Features 26
8.13 DMA controller 26
8.13.1 Features 26
8.14 USB interface 27
8.14.1 Full-speed USB device controller 27
8.14.1.1 Features 27
8.15 USART0 27
8.15.1 Features 28
8.16 USART1/2/3/4 28
8.16.1 Features 28
8.17 SSP serial I/O controller (SSP0/1) 29
8.17.1 Features 29
8.18 I²C-bus serial I/O controller 29
8.18.1 Features 30
8.19 Timer/PWM subsystem 30
8.19.1 State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM) 31
8.19.1.1 Features 32
8.19.2 General purpose external event counter/timers (CT32B0/1 and CT16B0/1) 33
8.19.2.1 Features 33
8.20 System tick timer (SysTick) 33
8.21 Windowed WatchDog Timer (WWDT) 33
8.21.1 Features 33
8.22 Real-Time Clock (RTC) 34
8.22.1 Features 34
8.23 Analog-to-Digital Converter (ADC) 34
8.23.1 Features 34
8.24 Temperature sensor 35
8.25 Clocking and power control 36
8.25.1 Clock generation 36
8.25.2 Power domains 37
8.25.3 Integrated oscillators 37
8.25.3.1 Internal RC oscillator 38
8.25.3.2 System oscillator 38
8.25.3.3 WatchDog oscillator 38
8.25.3.4 RTC oscillator 38
8.25.4 System PLL and USB PLL 38
8.25.5 Clock output 38
8.25.6 Wake-up process 39
8.25.7 Power control 39
8.25.7.1 Power profiles 39
8.25.7.2 Sleep mode 39
8.25.7.3 Deep-sleep mode 40
8.25.7.4 Power-down mode 40
8.25.7.5 Deep power-down mode 40
8.26 System control 40
8.26.1 Reset 40
8.26.2 Brownout detection 41
8.26.3 Code security (Code Read Protection - CRP) 41
8.27 Emulation and debugging 43
9 Limiting values 44
10 Thermal characteristics 45
11 Static characteristics 46
11.1 Power consumption 52
11.2 CoreMark data 56
11.3 Peripheral power consumption 57
11.4 Electrical pin characteristics 59
12 Dynamic characteristics 62
12.1 Flash/EEPROM memory 62
12.2 External clock for the oscillator in slave mode 62
12.3 Internal oscillators 63
12.4 I/O pins 64
12.5 I²C-bus 64

continued >>

12.6 SSP interface 66
12.7 USART interface 68
12.8 SCTimer/PWM output timing 69
13 Characteristics of analog peripherals 70
14 Application information 75
14.1 ADC usage notes 75
14.2 Typical wake-up times 75
14.3 Suggested USB interface solutions 75
14.3.1 USB Low-speed operation 77
14.4 XTAL input and crystal oscillator component selection 78
14.5 XTAL Printed-Circuit Board (PCB) layout guidelines 80
14.6 RTC oscillator component selection 81
14.7 Connecting power, clocks, and debug functions 81
14.8 Termination of unused pins 83
14.9 Pin states in different power modes 84
15 Package outline 85
16 Soldering 88
17 References 91
18 Revision history 92
19 Legal information 93
19.1 Data sheet status 93
19.2 Definitions 93
19.3 Disclaimers 93
19.4 Trademarks 94
20 Contact information 94
21 Contents 95

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 7 September 2016
Document identifier: LPC11U6x