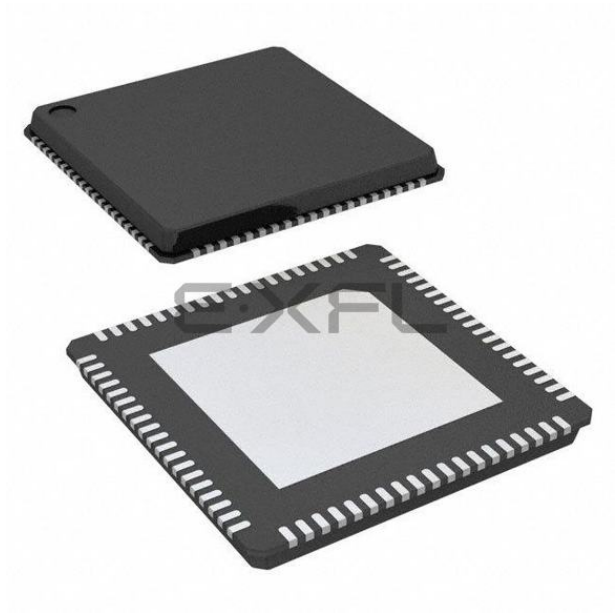

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FT32
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	Ethernet, I²C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	42
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	2.97V ~ 3.63V
Data Converters	A/D 4x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	76-VFQFN Exposed Pad
Supplier Device Package	76-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/bridgetek/ft906q-t

6. Pinning information

6.1 Pinning

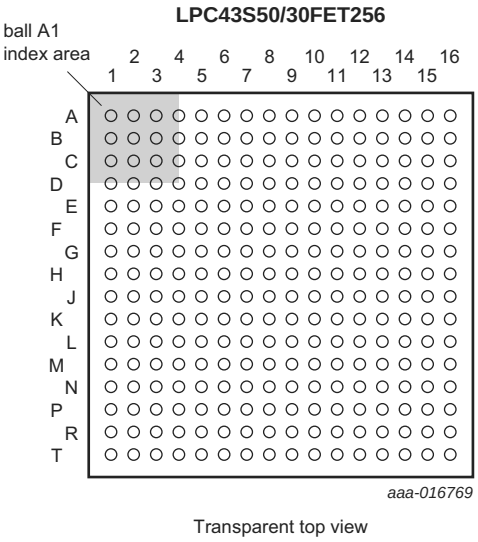


Fig 2. Pin configuration LBGA256 package

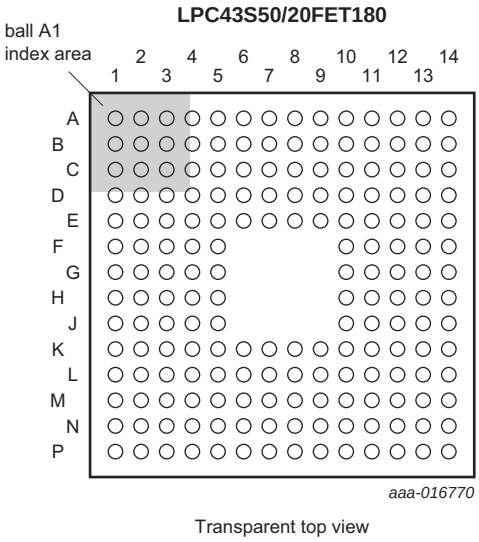


Fig 3. Pin configuration TFBGA180 package

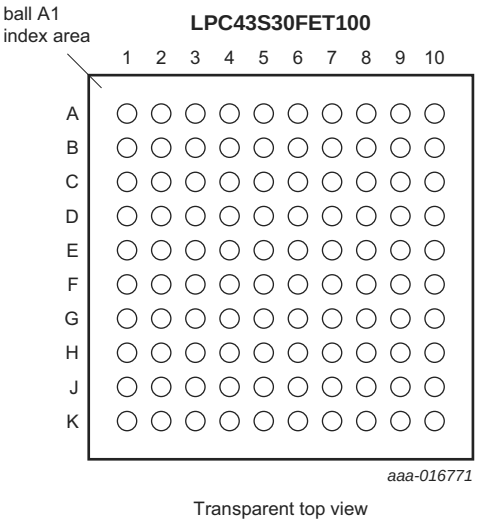


Fig 4. Pin configuration TFBGA100 package

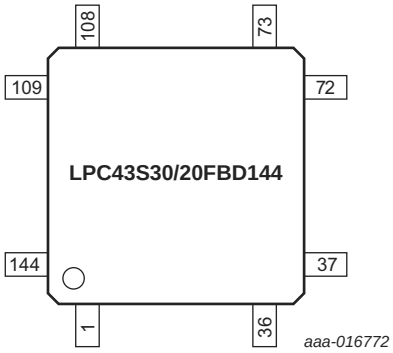


Fig 5. Pin configuration LQFP144 package

6.2 Pin description

On the LPC43S50/S30/S20, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General-Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P5_6	T13	M11	-	63	[2]	N; PU	I/O	**GPIO2[15] —** General purpose digital input/output pin.
							O	**MCOB1 —** Motor control PWM channel 1, output B.
							I/O	**EMC_D10 —** External memory data line 10.
							-	**R —** Function reserved.
							O	**U1_TXD —** Transmitter output for UART 1.
							O	**T1_MAT2 —** Match output 2 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_7	R12	N11	-	65	[2]	N; PU	I/O	**GPIO2[7] —** General purpose digital input/output pin.
							O	**MCOA2 —** Motor control PWM channel 2, output A.
							I/O	**EMC_D11 —** External memory data line 11.
							-	**R —** Function reserved.
							I	**U1_RXD —** Receiver input for UART 1.
							O	**T1_MAT3 —** Match output 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_0	M12	M10	H7	73	[2]	N; PU	-	**R —** Function reserved.
							O	**I2S0_RX_MCLK —** I2S receive master clock.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S0_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_1	R15	P14	G5	74	[2]	N; PU	I/O	**GPIO3[0] —** General purpose digital input/output pin.
							O	**EMC_DYCS1 —** SDRAM chip select 1.
							I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
							I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							-	**R —** Function reserved.
							I	**T2_CAP0 —** Capture input 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PC_11	L5	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULPI data line direction.
							I	**U1_DCD —** Data Carrier Detect input for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[10] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT4 —** SD/MMC data bus line 4.
PC_12	L6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[11] —** General purpose digital input/output pin.
							I/O	**SGPIO11 —** General purpose digital input/output pin.
							I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SD_DAT5 —** SD/MMC data bus line 5.
PC_13	M1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**U1_TXD —** Transmitter output for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[12] —** General purpose digital input/output pin.
							I/O	**SGPIO12 —** General purpose digital input/output pin.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**SD_DAT6 —** SD/MMC data bus line 6.
PC_14	N1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**U1_RXD —** Receiver input for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[13] —** General purpose digital input/output pin.
							I/O	**SGPIO13 —** General purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							I/O	**SD_DAT7 —** SD/MMC data bus line 7.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PD_8	P8	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							I/O	**EMC_D22 —** External memory data line 22.
							-	**R —** Function reserved.
							I/O	**GPIO6[22] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO12 —** General purpose digital input/output pin.
PD_9	T11	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D23 —** External memory data line 23.
							-	**R —** Function reserved.
							I/O	**GPIO6[23] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO13 —** General purpose digital input/output pin.
PD_10	P11	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_1 —** SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							O	**$\overline{\text{EMC\_BLS3}}$ —** LOW active Byte Lane select signal 3.
							-	**R —** Function reserved.
							I/O	**GPIO6[24] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_11	N9	M7	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_CS3}}$ —** LOW active Chip Select 3 signal.
							-	**R —** Function reserved.
							I/O	**GPIO6[25] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PD_12	N11	P9	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_CS2}}$ —** LOW active Chip Select 2 signal.
							-	**R —** Function reserved.
							I/O	**GPIO6[26] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
							-	**R —** Function reserved.
PD_13	T14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_0 —** SCTimer/PWM input 0. Capture input 0 of timer 0, 1, 2, 3.
							O	**$\overline{\text{EMC\_BLS2}}$ —** LOW active Byte Lane select signal 2.
							-	**R —** Function reserved.
							I/O	**GPIO6[27] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							-	**R —** Function reserved.
PD_14	R13	L11	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_DYCS2}}$ —** SDRAM chip select 2.
							-	**R —** Function reserved.
							I/O	**GPIO6[28] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**CTOUT_11 —** SCTimer/PWM output 11. Match output 3 of timer 2.
							-	**R —** Function reserved.
PD_15	T15	P13	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A17 —** External memory address line 17.
							-	**R —** Function reserved.
							I/O	**GPIO6[29] —** General purpose digital input/output pin.
							I	**SD_WP —** SD/MMC card write protect input.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PE_11	D16	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							O	**U1_TXD —** Transmitter output for UART 1.
							I/O	**EMC_D30 —** External memory data line 30.
							I/O	**GPIO7[11] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_12	D15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_11 —** SCTimer/PWM output 11. Match output 3 of timer 2.
							I	**U1_RXD —** Receiver input for UART 1.
							I/O	**EMC_D31 —** External memory data line 31.
							I/O	**GPIO7[12] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_13	G14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
							O	**EMC_DQMOUT3 —** Data mask 3 used with SDRAM and static devices.
							I/O	**GPIO7[13] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_14	C15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_DYCS3 —** SDRAM chip select 3.
							I/O	**GPIO7[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

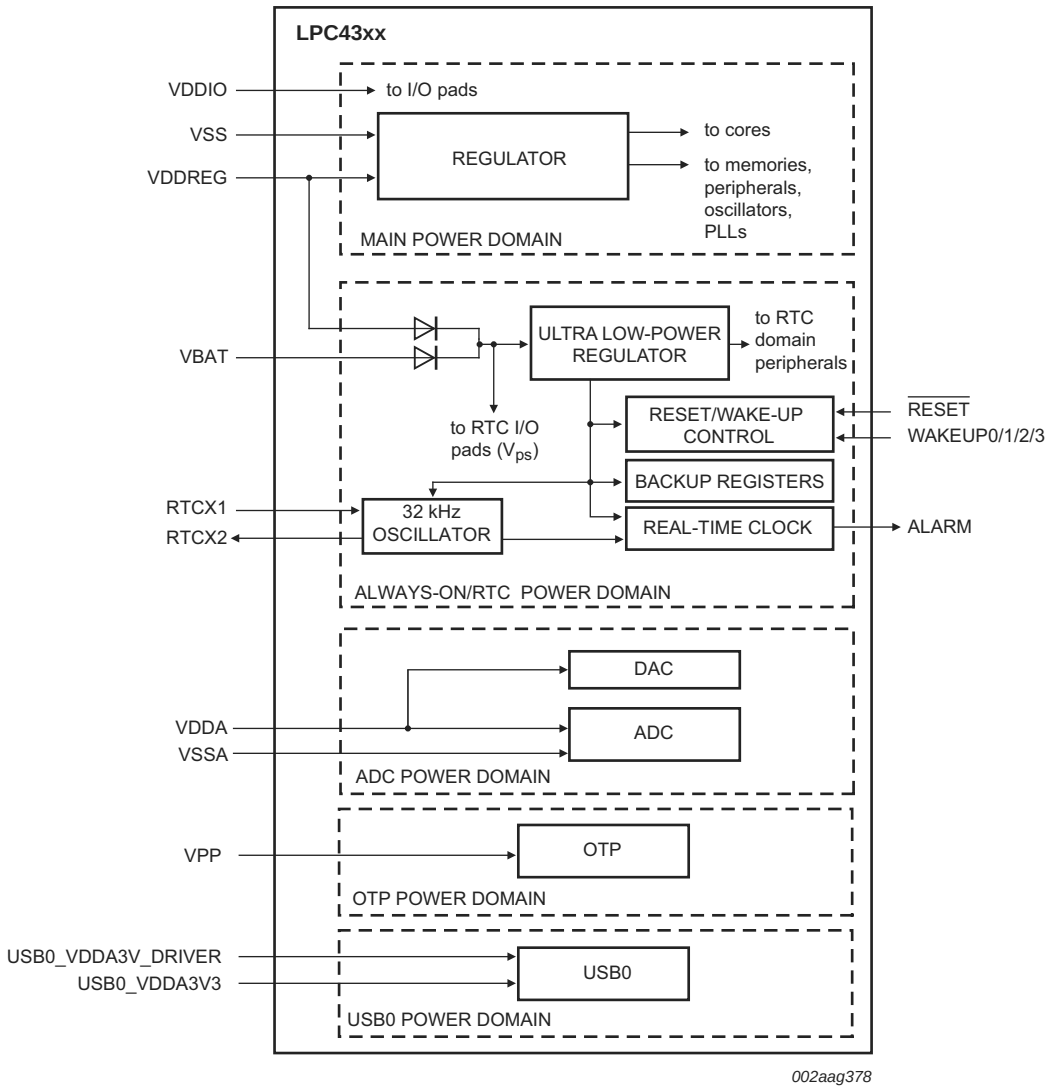


Fig 9. Power domains

7.22.10 Power Management Controller (PMC)

The PMC controls the power to the cores, peripherals, and memories.

The LPC43S50/S30/S20 support the following power modes in order from highest to lowest power consumption:

1. Active mode
2. Sleep mode
3. Power-down modes:
   a. Deep-sleep mode
   b. Power-down mode
   c. Deep power-down mode

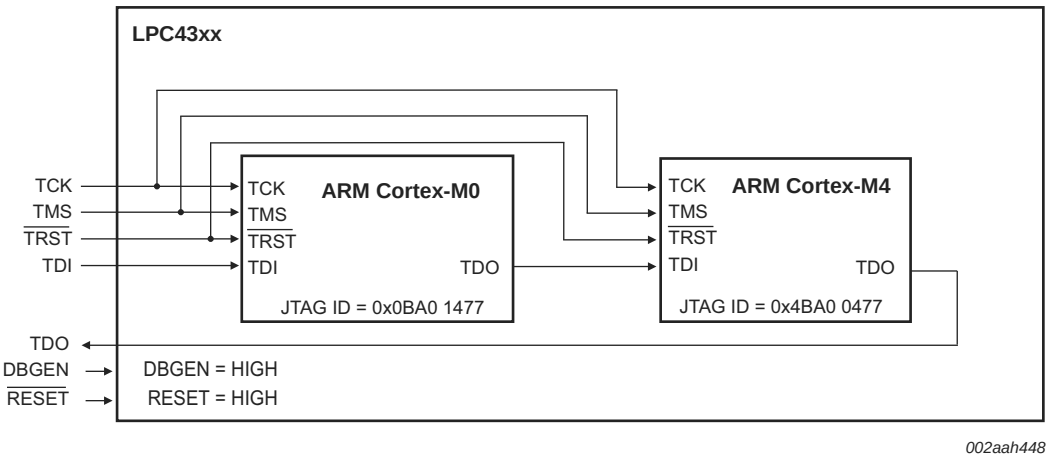


Fig 10. Dual-core debug configuration

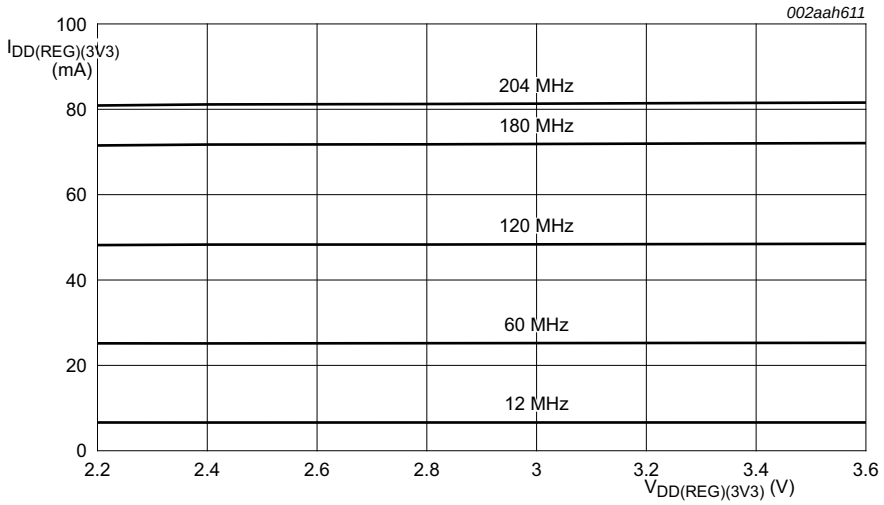
Table 10. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{BAT}	battery supply current	$V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} = 3.6 V	[8]				
		deep-sleep mode		-	2	-	µA
		power-down mode	[8]	-	2	-	µA
		deep power-down mode	[8]	-	2	-	µA
$I_{DD(IO)}$	I/O supply current	deep sleep mode	-	-	1	-	µA
		power-down mode	-	-	1	-	µA
		deep power-down mode	[9]	-	0.05	-	µA
I_{DDA}	Analog supply current	on pin VDDA;	[11]	-	0.4	-	
		deep sleep mode					µA
		power-down mode	[11]	-	0.4	-	µA
		deep power-down mode	[11]	-	0.007	-	µA
$\overline{RESET}$,RTC_ALARM, WAKEUPn pins							
V_{IH}	HIGH-level input voltage		[10]	$0.8 \times (V_{ps} - 0.35)$	-	5.5	V
V_{IL}	LOW-level input voltage		[10]	0	-	$0.3 \times (V_{ps} - 0.1)$	V
V_{hys}	hysteresis voltage		[10]	$0.05 \times (V_{ps} - 0.35)$	-	-	V
V_o	output voltage		[10]	-	V_{ps} - 0.2	-	V
Standard I/O pins - normal drive strength							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V		-	-	20	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function;		0	-	5.5	V
		$V_{DD(IO)} \geq$ 2.2 V					
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			0	-	$0.3 \times V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			$0.1 \times V_{DD(IO)}$	-	-	V

Table 10. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

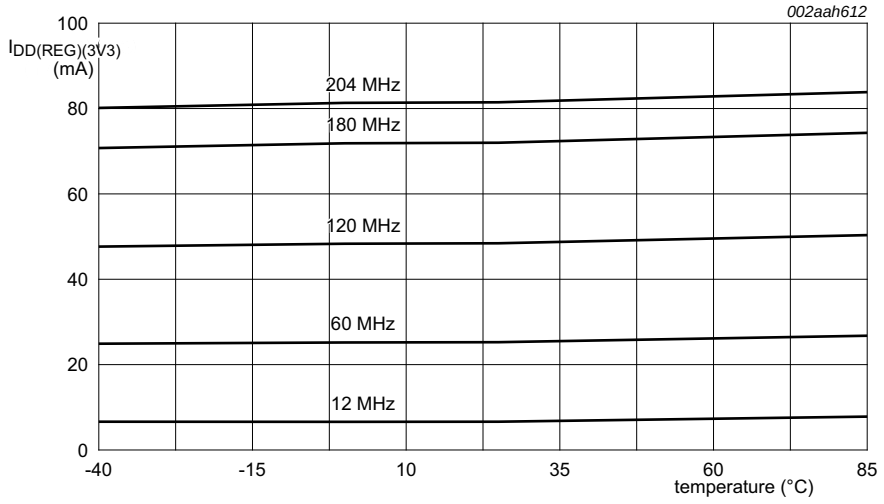
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pu}	pull-up current	V_I = 0 V	[14][15][16]	-	−62	-	μA
		$V_{DD(IO)} < V_I \leq 5$ V		-	10	-	μA
I/O pins - high drive strength: standard drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	32	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	32	mA
I/O pins - high drive strength: medium drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	65	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	63	mA
I/O pins - high drive strength: high drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−14	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		14	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	113	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	110	mA
I/O pins - high drive strength: ultra-high drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−20	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		20	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	165	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	156	mA
I/O pins - high-speed							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA

10.1 Power consumption



Conditions: T_{amb} = 25 °C; active mode entered executing code while(1){} from SRAM; M0-core in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 11. Typical supply current versus regulator supply voltage $V_{DD(REG)(3V3)}$ in active mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V, Active mode entered executing code while(1){} from SRAM; M0-core in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 12. Typical supply current versus temperature in Active mode

10.3 BOD and band gap static characteristics

Table 12. BOD static characteristics[1]

T_{amb} = 25 °C; simulated values for nominal processing.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0					
		assertion		-	2.75	-	V
		de-assertion		-	2.92	-	V
		interrupt level 1					
		assertion		-	2.85	-	V
		de-assertion		-	3.00	-	V
		interrupt level 2					
		assertion		-	2.95	-	V
		de-assertion		-	3.12	-	V
		interrupt level 3					
		assertion		-	3.05	-	V
		de-assertion		-	3.19	-	V
		reset level 0					
		assertion		-	1.70	-	V
		de-assertion		-	1.85	-	V
		reset level 1					
		assertion		-	1.80	-	V
		de-assertion		-	1.95	-	V
		reset level 2					
		assertion		-	1.90	-	V
		de-assertion		-	2.05	-	V
		reset level 3					
		assertion		-	2.00	-	V
		de-assertion		-	2.15	-	V

[1] Interrupt and reset levels are selected by writing to the BODLV1/2 bits in the control register CREGE0, see the *LPC43xx user manual*.

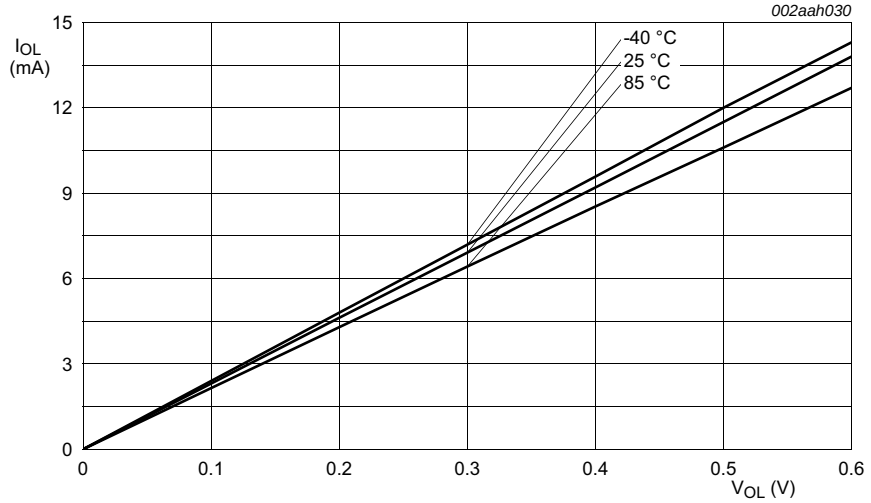
Table 13. Band gap characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +105 °C; unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
$V_{ref(bg)}$	band gap reference voltage	[1]	0.621	0.6425	0.664	mV

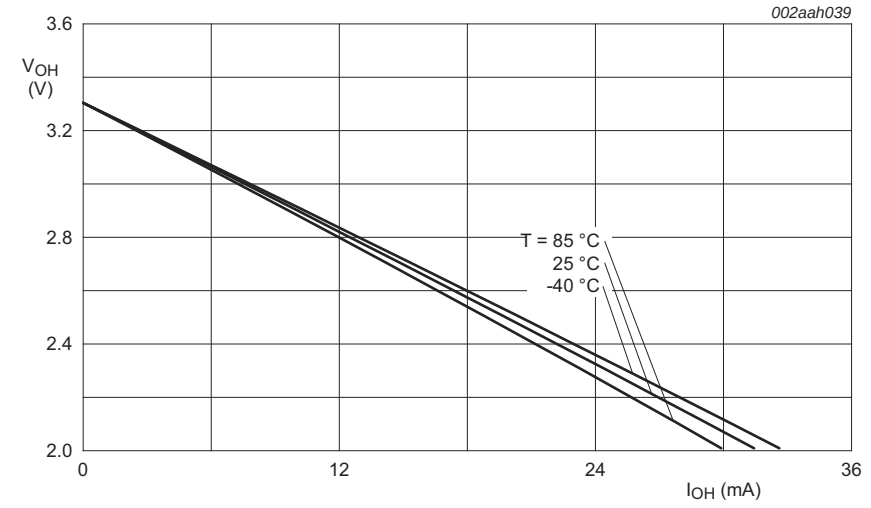
[1] Based on characterization, not tested in production.

10.4 Electrical pin characteristics



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 20. Normal-drive pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 21. Normal-drive pins; typical HIGH level output voltage V_{OL} versus HGH level output current I_{OH}

11.11 SSP interface

Table 24. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SSP master							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	$1/(25.5 \times 10^6)$	-	-	s
		when only transmitting		$1/(51 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		13.6	-	-	ns
t_{DH}	data hold time	in SPI mode		−3.8	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	6.0	ns
$t_{h(Q)}$	data output hold time	in SPI mode		−1.1	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)} + 3.2$	-	$T_{cy(clk)} + 6.1$	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)} + 3.2$	-	$0.5 \times T_{cy(clk)} + 6.1$	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)} + 3.2$	-	$T_{cy(clk)} + 6.1$	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)} + 3.2$	-	$0.5 \times T_{cy(clk)} + 6.1$	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)} + 3.2$	-	$0.5 \times T_{cy(clk)} + 6.1$	ns
		microwire frame format		$T_{cy(clk)} + 3.2$	-	$T_{cy(clk)} + 6.1$	ns
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$	-	-	ns
		microwire frame format		$0.5 \times T_{cy(clk)}$	-	-	ns

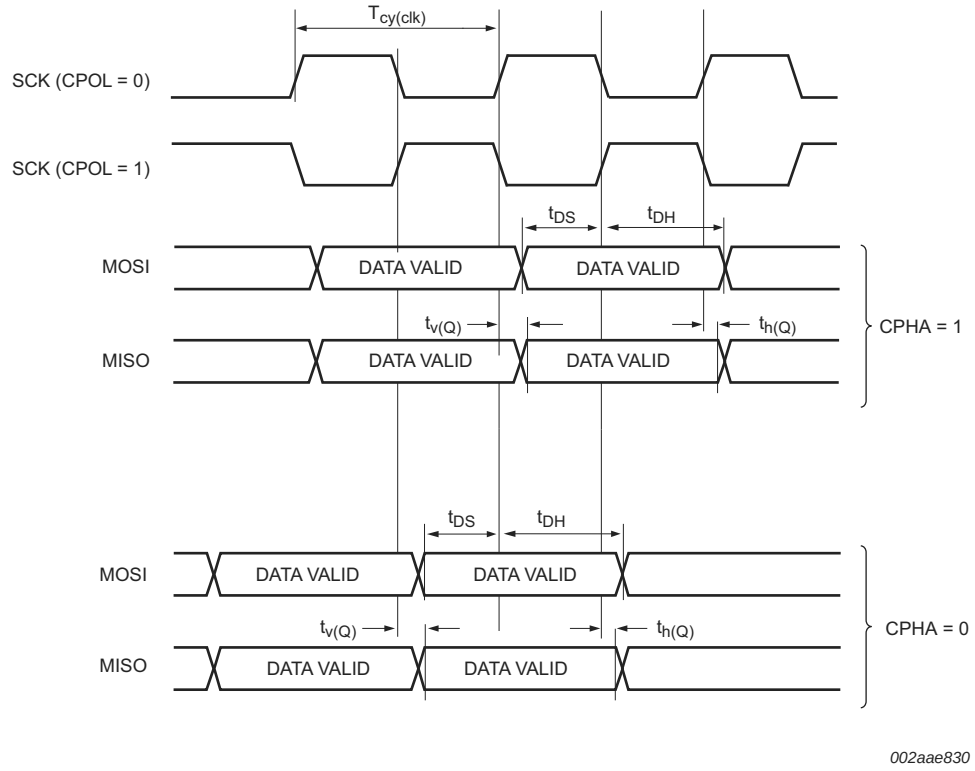
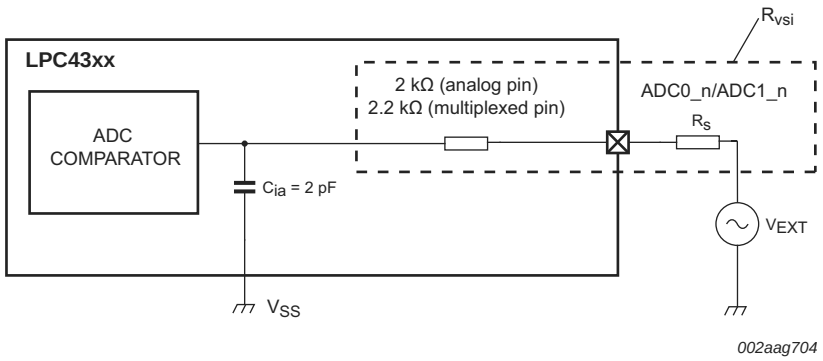


Fig 32. SSP slave mode timing (SPI mode)

11.14 SGPIO timing

The following considerations apply to SGPIO timing:

- SGPIO input signals are synchronized by the internal clock SGPIO_CLOCK. To guarantee that no samples are missed, all input signals should have a duration of at least one SGPIO_CLOCK cycle plus the set-up and hold times.
- When an external clock input is used to generate output data, synchronization causes a latency of at least one SGPIO_CLOCK cycle. The maximum output data rate is one output every two SGPIO_CLOCK cycles.
- Synchronization also causes a latency of one SGPIO_CLOCK cycle when sampling several inputs. This may cause inputs with very similar timings to be sampled with a difference of one SGPIO_CLOCK cycle.



$Rs < 1/((7 \times f_{clk(ADC)} \times C_{ia}) - 2\ k\Omega)$

Fig 42. ADC interface to pins

Table 37. DAC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	code = 0 to 975 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±1.0	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.5	-	LSB
E_O	offset error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
E_G	gain error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.3	-	%
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	%
C_L	load capacitance			-	-	200	pF
R_L	load resistance			1	-	-	kΩ
t_s	settling time		[2]		0.4		μσ

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC43xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.

Table 41. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode *…continued*

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
12 MHz	< 160 Ω	18 pF, 18 pF
	< 160 Ω	39 pF, 39 pF
16 MHz	< 120 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF
20 MHz	<100 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF

Table 42. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{x2}
15 MHz	< 80 Ω	18 pF, 18 pF
20 MHz	< 80 Ω	39 pF, 39 pF
	< 100 Ω	47 pF, 47 pF

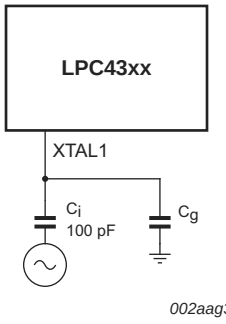


Fig 43. Slave mode operation of the on-chip oscillator

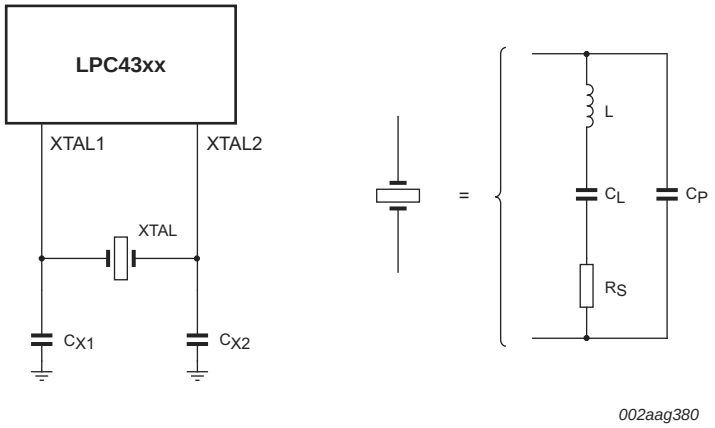
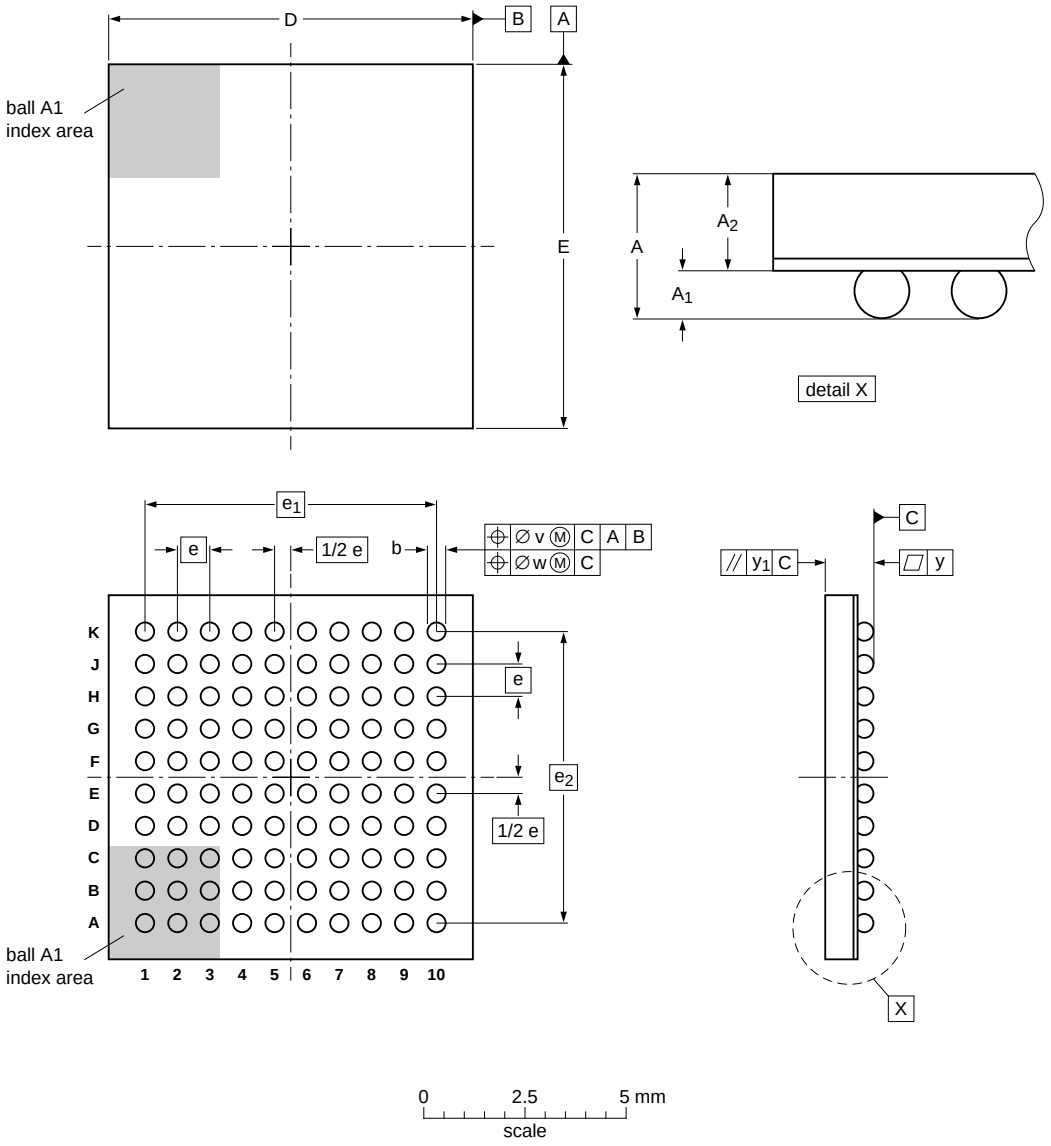


Fig 44. Oscillator modes with external crystal model used for C_{X1}/C_{X2} evaluation

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 53. Package outline of the TFBGA100 package

18. Revision history

Table 44. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC43S50_S30_S20 v.1.2	20160316	Product data sheet	-	LPC43S50_S30_S20 v.1.1
Modifications:	• Updated Table 28 “Dynamic characteristics: Dynamic external memory interface”: Read cycle parameters $t_{h(D)}$ min value is 2.2 ns and max value is “-”.			
LPC43S50_S30_S20 v.1.1	20151117	Product data sheet	2015110031	LPC43S50_S30_S20 v.1.0
Modifications:	• Minor edits. • Updated Section 1 “General description”. • Added motor control PWM instead of PWM to Table 2 “Ordering options”. • Table note 2 corrected in Table 10 “Static characteristics”. • Added a remark to Table 30 “Dynamic characteristics: USB0 and USB1 pins (full-speed)”. • Changed the value in the following text to 0.686 V from ~0.686 V in Section 13.7 “Suggested USB interface solutions”: "For the following operating conditions, $VBUS_{max}$ = 5.25 V; VDDIO = 3.6 V, the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V." • Added GPCLKIN section and table. See Section 11.6 “GPCLKIN” and Table 19 “Dynamic characteristic: GPCLKIN”. • Updated SSP slave and SSP master values in Table 24 “Dynamic characteristics: SSP pins in SPI mode”. Updated footnote 2 to: $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$. – removed $t_{v(Q)}$, data output valid time in SPI mode, minimum value of 3 ´ (1/PCLK) from SSP slave mode. – added units to t_d, delay time, for SSP slave and master mode.			
LPC43S50_S30_S20 v.1.0	20150210	Product data sheet	-	-

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