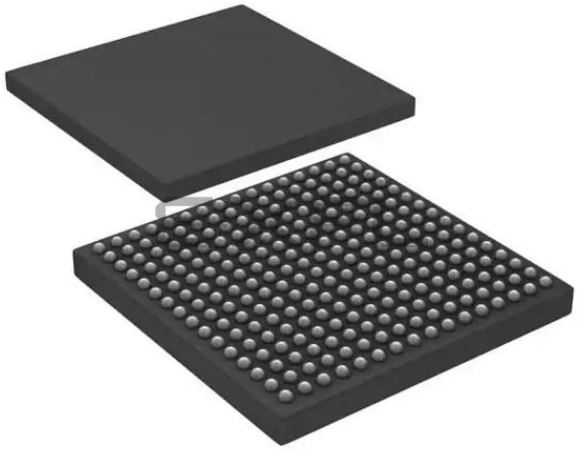

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	164
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	264K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-LBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc43s30fet256e

6. Pinning information

6.1 Pinning

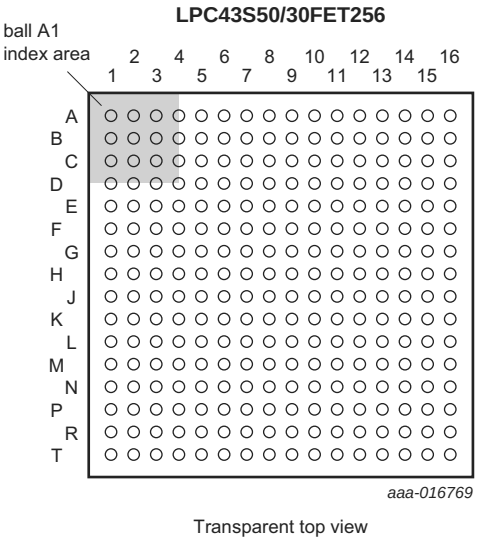


Fig 2. Pin configuration LBGA256 package

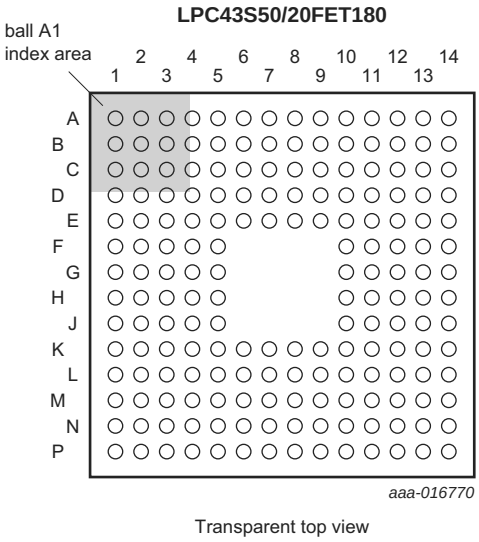


Fig 3. Pin configuration TFBGA180 package

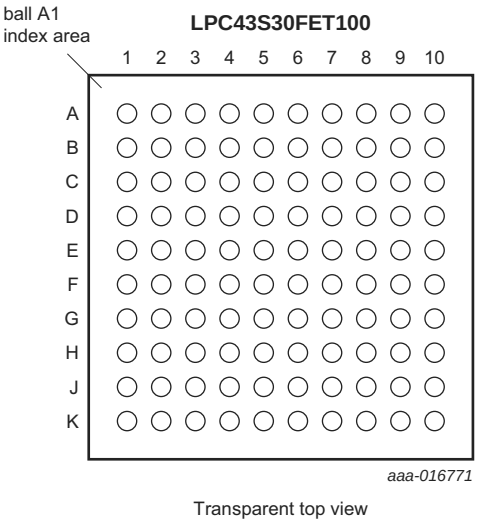


Fig 4. Pin configuration TFBGA100 package

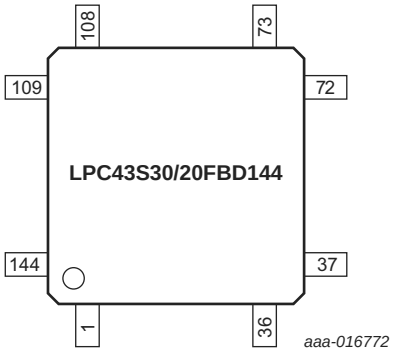


Fig 5. Pin configuration LQFP144 package

6.2 Pin description

On the LPC43S50/S30/S20, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General-Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P3_4	A15	C14	B8	119	[2]	N; PU	I/O	**GPIO1[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SPIFI_SIO3 —** I/O lane 3 for SPIFI.
							O	**U1_TXD —** Transmitter output for UART 1.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S1_RX_SDA —** I2S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**LCD_VD13 —** LCD data.
P3_5	C12	C11	B7	121	[2]	N; PU	I/O	**GPIO1[15] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SPIFI_SIO2 —** I/O lane 2 for SPIFI.
							I	**U1_RXD —** Receiver input for UART 1.
							I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I/O	**I2S1_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							O	**LCD_VD12 —** LCD data.
P3_6	B13	B12	C7	122	[2]	N; PU	I/O	**GPIO0[6] —** General purpose digital input/output pin.
							I/O	**SPI_MISO —** Master In Slave Out for SPI.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I/O	**SPIFI_MISO —** Input 1 in SPIFI quad mode; SPIFI output IO1.
							-	**R —** Function reserved.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P3_7	C11	C10	D7	123	[2]	N; PU	-	**R —** Function reserved.
							I/O	**SPI_MOSI —** Master Out Slave In for SPI.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							I/O	**SPIFI_MOSI —** Input I0 in SPIFI quad mode; SPIFI output IO0.
							I/O	**GPIO5[10] —** General purpose digital input/output pin.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P5_2	R4	M3	-	46	[2]	N; PU	I/O	**GPIO2[11] —** General purpose digital input/output pin.
							I	**MCI1 —** Motor control PWM channel 1, input.
							I/O	**EMC_D14 —** External memory data line 14.
							-	**R —** Function reserved.
							O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							I	**T1_CAP2 —** Capture input 2 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_3	T8	P6	-	54	[2]	N; PU	I/O	**GPIO2[12] —** General purpose digital input/output pin.
							I	**MCI0 —** Motor control PWM channel 0, input.
							I/O	**EMC_D15 —** External memory data line 15.
							-	**R —** Function reserved.
							I	**U1_RI —** Ring Indicator input for UART 1.
							I	**T1_CAP3 —** Capture input 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_4	P9	N7	-	57	[2]	N; PU	I/O	**GPIO2[13] —** General purpose digital input/output pin.
							O	**MCOB0 —** Motor control PWM channel 0, output B.
							I/O	**EMC_D8 —** External memory data line 8.
							-	**R —** Function reserved.
							I	**U1_CTS —** Clear to Send input for UART 1.
							O	**T1_MAT0 —** Match output 0 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_5	P10	N8	-	58	[2]	N; PU	I/O	**GPIO2[14] —** General purpose digital input/output pin.
							O	**MCOA1 —** Motor control PWM channel 1, output A.
							I/O	**EMC_D9 —** External memory data line 9.
							-	**R —** Function reserved.
							I	**U1_DCD —** Data Carrier Detect input for UART 1.
							O	**T1_MAT1 —** Match output 1 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P9_2	N8	M6	-	-	[2]	N; PU	I/O	**GPIO4[14] —** General purpose digital input/output pin.
							O	**MCOB2 —** Motor control PWM channel 2, output B.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I	**ENET_RXD3 —** Ethernet receive data 3 (MII interface).
							I/O	**SGPIO2 —** General purpose digital input/output pin.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
P9_3	M6	P5	-	-	[2]	N; PU	I/O	**GPIO4[15] —** General purpose digital input/output pin.
							O	**MCOA0 —** Motor control PWM channel 0, output A.
							O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**ENET_RXD2 —** Ethernet receive data 2 (MII interface).
							I/O	**SGPIO9 —** General purpose digital input/output pin.
							O	**U3_TXD —** Transmitter output for USART3.
P9_4	N10	M8	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**MCOB0 —** Motor control PWM channel 0, output B.
							O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
							-	**R —** Function reserved.
							I/O	**GPIO5[17] —** General purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							I/O	**SGPIO4 —** General purpose digital input/output pin.
							I	**U3_RXD —** Receiver input for USART3.
P9_5	M9	L7	-	69	[2]	N; PU	-	**R —** Function reserved.
							O	**MCOA1 —** Motor control PWM channel 1, output A.
							O	**USB1_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active high). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB\_PPWR}}$ used on other NXP LPC parts.
							-	**R —** Function reserved.
							I/O	**GPIO5[18] —** General purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**SGPIO3 —** General purpose digital input/output pin.
							O	**U0_TXD —** Transmitter output for USART0.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PC_11	L5	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULPI data line direction.
							I	**U1_DCD —** Data Carrier Detect input for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[10] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT4 —** SD/MMC data bus line 4.
PC_12	L6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[11] —** General purpose digital input/output pin.
							I/O	**SGPIO11 —** General purpose digital input/output pin.
							I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SD_DAT5 —** SD/MMC data bus line 5.
PC_13	M1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**U1_TXD —** Transmitter output for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[12] —** General purpose digital input/output pin.
							I/O	**SGPIO12 —** General purpose digital input/output pin.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**SD_DAT6 —** SD/MMC data bus line 6.
PC_14	N1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**U1_RXD —** Receiver input for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[13] —** General purpose digital input/output pin.
							I/O	**SGPIO13 —** General purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							I/O	**SD_DAT7 —** SD/MMC data bus line 7.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PD_0	N2	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3.
							O	**EMC_DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
							-	**R —** Function reserved.
							I/O	**GPIO6[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO4 —** General purpose digital input/output pin.
PD_1	P1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_CKEOUT2 —** SDRAM clock enable 2.
							-	**R —** Function reserved.
							I/O	**GPIO6[15] —** General purpose digital input/output pin.
							O	**SD_POW —** SD/MMC power monitor output.
							-	**R —** Function reserved.
							I/O	**SGPIO5 —** General purpose digital input/output pin.
PD_2	R1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							I/O	**EMC_D16 —** External memory data line 16.
							-	**R —** Function reserved.
							I/O	**GPIO6[16] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO6 —** General purpose digital input/output pin.
PD_3	P4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_6 —** SCTimer/PWM output 7. Match output 2 of timer 1.
							I/O	**EMC_D17 —** External memory data line 17.
							-	**R —** Function reserved.
							I/O	**GPIO6[17] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO7 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
WAKEUP1	A10	C8	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration > 45 ns wakes up the part. This pin does not have an internal pull-up.
WAKEUP2	C9	E5	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration > 45 ns wakes up the part. This pin does not have an internal pull-up.
WAKEUP3	D8	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration > 45 ns wakes up the part. This pin does not have an internal pull-up.
ADC pins								
ADC0_0/ ADC1_0/DAC	E3	B6	A2	6	[8]	I; IA	I	ADC input channel 0. Shared between 10-bit ADC0/1 and DAC.
ADC0_1/ ADC1_1	C3	C4	A1	2	[8]	I; IA	I	ADC input channel 1. Shared between 10-bit ADC0/1.
ADC0_2/ ADC1_2	A4	B3	B3	143	[8]	I; IA	I	ADC input channel 2. Shared between 10-bit ADC0/1.
ADC0_3/ ADC1_3	B5	B4	A3	139	[8]	I; IA	I	ADC input channel 3. Shared between 10-bit ADC0/1.
ADC0_4/ ADC1_4	C6	A5	-	138	[8]	I; IA	I	ADC input channel 4. Shared between 10-bit ADC0/1.
ADC0_5/ ADC1_5	B3	C3	-	144	[8]	I; IA	I	ADC input channel 5. Shared between 10-bit ADC0/1.
ADC0_6/ ADC1_6	A5	A4	-	142	[8]	I; IA	I	ADC input channel 6. Shared between 10-bit ADC0/1.
ADC0_7/ ADC1_7	C5	B5	-	136	[8]	I; IA	I	ADC input channel 7. Shared between 10-bit ADC0/1.
RTC								
RTC_ALARM	A11	A10	C3	129	[11]	O	O	RTC controlled output. This pin has an internal pull-up. The reset state of this pin is LOW after POR. For all other types of reset, the reset state depends on the state of the RTC alarm interrupt.
RTCX1	A8	A8	A5	125	[8]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	B7	B5	126	[8]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
Crystal oscillator pins								
XTAL1	D1	C1	B1	12	[8]	-	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	E1	D1	C1	13	[8]	-	O	Output from the oscillator amplifier.
Power and ground pins								
USB0_VDDA 3V3_DRIVER	F3	E3	D1	16		-	-	Separate analog 3.3 V power supply for driver.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
VSSIO	C4, D13, G6, G7, G8, H8, H9, J8, J9, K9, K10, M13, P7, P13	-	C8, D4, D5, G8, J3, J6	4, 40, 76, 109	[13] [14]	-	-	Ground.
VSSA	B2	A3	C2	135		-	-	Analog ground.
Not connected								
-	B9	B8	-	-		-	-	n.c.

[1] N = neutral, input buffer disabled; no extra VDDIO current consumption if the input is driven midway between supplies; set the EZI bit in the SFS register to enable the input buffer; I = input; OL = output driving LOW; OH = output driving HIGH; AI/O = analog input/output; IA = inactive; PU = pull-up enabled (weak pull-up resistor pulls up pin to VDDIO; F = floating. Reset state reflects the pin state at reset without boot code operation.

[2] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength.

[3] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels, and hysteresis; high drive strength.

[4] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides high-speed digital I/O functions with TTL levels and hysteresis.

[5] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input or output (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V). When configured as an ADC input or DAC output, the pin is not 5 V tolerant and the digital section of the pad must be disabled by setting the pin to an input function and disabling the pull-up resistor through the pin's SFSP register.

[6] 5 V tolerant transparent analog pad.

[7] For maximum load C_L = 6.5 µF and maximum pull-down resistance R_{pd} = 80 kΩ, the VBUS signal takes about 2 s to fall from VBUS = 5 V to VBUS = 0.2 V when it is no longer driven.

[8] Transparent analog pad. Not 5 V tolerant.

[9] Pad provides USB functions 5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only).

[10] Open-drain 5 V tolerant digital I/O pad, compatible with I2C-bus Fast Mode Plus specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I2C-bus is floating and does not disturb the I2C lines.

[11] 5 V tolerant pad with 20 ns glitch filter; provides digital I/O functions with open-drain output and hysteresis.

[12] On the TFBGA100 package, VPP is internally connected to VDDIO.

[13] On the LQFP144 package, VSSIO and VSS are connected to a common ground plane.

[14] On the TFBGA100 package, VSS is internally connected to VSSIO.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-CODE bus, and the D-code bus. The I-CODE and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC43S50/S30/S20 use a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

An ARM Cortex-M0 co-processor is included in the LPC43S50/S30/S20, capable of off-loading the main ARM Cortex-M4 application processor. Most peripheral interrupts are connected to both processors. The processors communicate with each other via an interprocessor communication protocol.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core. The processor includes an NVIC with up to 53 interrupts.

7.3 ARM Cortex-M0 coprocessor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low-power consumption. The ARM Cortex-M0 co-processor uses a 3-stage pipeline von-Neumann architecture and a small but powerful instruction set providing high-end processing hardware. The co-processor incorporates an NVIC with 32 interrupts.

7.4 Interprocessor communication

The ARM Cortex-M4 and ARM Cortex-M0 interprocessor communication is based on using shared SRAM as mailbox and one processor raising an interrupt on the other processor's NVIC, for example after it has delivered a new message in the mailbox. The receiving processor can reply by raising an interrupt on the sending processor's NVIC to acknowledge the message.

- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- Two AHB bus masters for transferring data. These interfaces transfer data when a DMA request goes active. Master 1 can access memories and peripherals, master 0 can access memories only.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.17.3 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the ARM Cortex-M4 processor with little performance penalty compared to parallel flash devices with higher pin count.

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasing and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.17.3.1 Features

- Interfaces to serial flash memory in the main memory map.

Active mode and sleep mode apply to the state of the core. In a dual-core system, either core can be in active or sleep mode independently of the other core.

If the core is in Active mode, it is fully operational and can access peripherals and memories as configured by software. If the core is in Sleep mode, it receives no clocks, but peripherals and memories remain running.

Either core can enter sleep mode from active mode independently of the other core and while the other core remains in active mode or is in sleep mode.

Power-down modes apply to the entire system. In the Power-down modes, both cores and all peripherals except for peripherals in the always-on power domain are shut down. Memories can remain powered for retaining memory contents as defined by the individual power-down mode.

Either core in active mode can put the part into one of the three power down modes if the core is enabled to do so. If both cores are enabled for putting the system into power-down, then the system enters power-down only once both cores have received a WFI or WFE instruction.

Wake-up from sleep mode is caused by an interrupt or event in the core's NVIC. The interrupt is captured in the NVIC and an event is captured in the Event router. Both cores can wake up from sleep mode independently of each other.

Wake-up from the Power-down modes, Deep-sleep, Power-down, and Deep power-down, is caused by an event on the WAKEUP pins or an event from the RTC or alarm timer.

When waking up from Deep power-down mode, the part resets and attempts to boot.

7.23 Serial Wire Debug/JTAG

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

Remark: Serial Wire Debug is supported for the ARM Cortex-M4 only,

The ARM Cortex-M0 coprocessor supports JTAG debug. A standard ARM Cortex-compliant debugger can debug the ARM Cortex-M4 and the ARM Cortex-M0 cores separately or both cores simultaneously.

Remark: In order to debug the ARM Cortex-M0, release the M0 reset by software in the RGU block.

Table 10. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{BAT}	battery supply current	$V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} = 3.6 V	[8]				
		deep-sleep mode		-	2	-	µA
		power-down mode	[8]	-	2	-	µA
		deep power-down mode	[8]	-	2	-	µA
$I_{DD(IO)}$	I/O supply current	deep sleep mode	-	-	1	-	µA
		power-down mode	-	-	1	-	µA
		deep power-down mode	[9]	-	0.05	-	µA
I_{DDA}	Analog supply current	on pin VDDA;	[11]	-	0.4	-	
		deep sleep mode					µA
		power-down mode	[11]	-	0.4	-	µA
		deep power-down mode	[11]	-	0.007	-	µA
$\overline{RESET}$,RTC_ALARM, WAKEUPn pins							
V_{IH}	HIGH-level input voltage		[10]	$0.8 \times (V_{ps} - 0.35)$	-	5.5	V
V_{IL}	LOW-level input voltage		[10]	0	-	$0.3 \times (V_{ps} - 0.1)$	V
V_{hys}	hysteresis voltage		[10]	$0.05 \times (V_{ps} - 0.35)$	-	-	V
V_o	output voltage		[10]	-	V_{ps} - 0.2	-	V
Standard I/O pins - normal drive strength							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V		-	-	20	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function;		0	-	5.5	V
		$V_{DD(IO)} \geq$ 2.2 V					
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			0	-	$0.3 \times V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			$0.1 \times V_{DD(IO)}$	-	-	V

Table 24. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$0.5T_{cy(clk)}$ + 0.2	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$ + 0.2	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		0.5 × $T_{cy(clk)}$ + 0.2	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$ + 0.2	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$ + 0.2	-	-	ns
		microwire frame format		0.5 × $T_{cy(clk)}$	-	-	ns
t_d	delay time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 0; CPHA = 1		-	n/a	-	ns
		SPI mode; CPOL = 1; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 1; CPHA = 1		-	n/a	-	ns
		synchronous serial frame mode		-	$T_{cy(clk)}$	-	ns
		microwire frame format		-	n/a	-	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

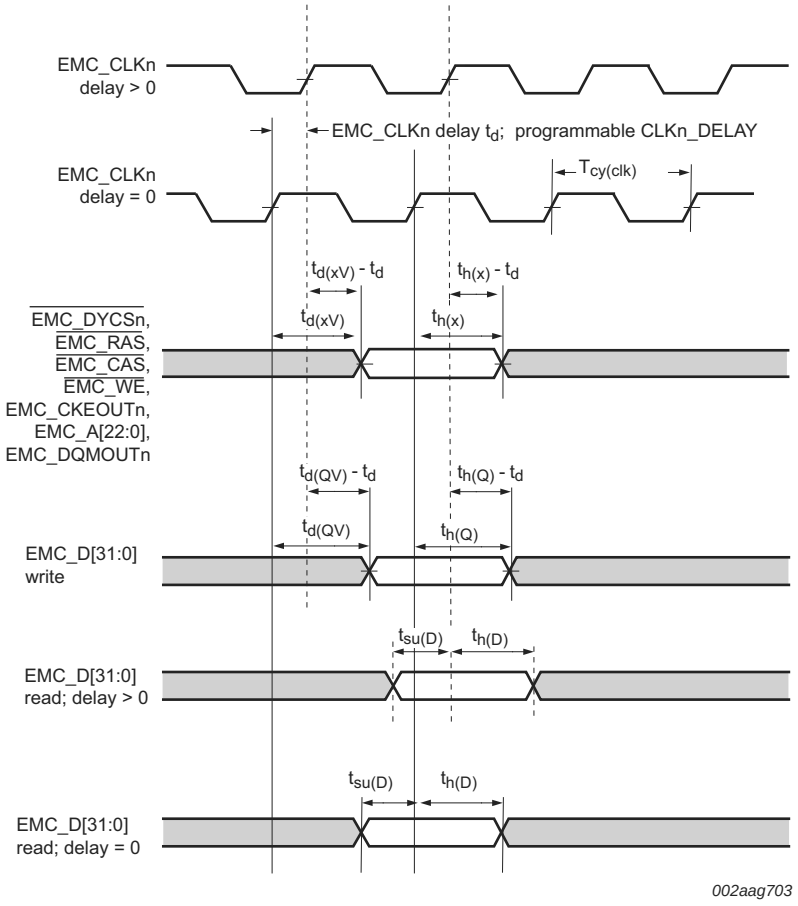
[2] $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$.

11.15 External memory interface

Table 27. Dynamic characteristics: Static asynchronous external memory interface

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design. Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted resulting in multiple memory accesses.

Symbol	Parameter[1]	Conditions		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time			−3.1	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		[2]	−0.6 + $T_{cy(clk)}$ × WAITOEN	-	1.3 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1		−0.7	-	1.8	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		[2]	−0.6 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time			-	-	−16 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	ns
$t_{h(D)}$	data input hold time			−16	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1		−0.4	-	1.9	ns
t_{CSHOEH}	CS HIGH to $\overline{OE}$ HIGH time			−0.4	-	1.4	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid	PB = 1		−2.0	-	2.6	ns
t_{CSHEOR}	$\overline{CS}$ HIGH to end of read time		[3]	−2.0	-	0	ns
t_{CSLSOR}	$\overline{CS}$ LOW to start of read time		[4]	0	-	1.8	ns
Write cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time			−3.1	-	1.6	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time			−3.1	-	1.5	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	PB = 1		−1.5	-	0.2	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1		−0.7	-	1.8	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	PB = 1	[2]	−0.6 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	PB = 1	[2]	−0.9 + $T_{cy(clk)}$	-	2.3 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	PB = 1	[2] [5]	−0.4 + $T_{cy(clk)}$	-	−0.3 + $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	PB = 0		−0.7	-	1.8	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 0	[2]	−0.9 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns



For the programmable EMC_CLK[3:0] clock delays CLKn_DELAY, see Table 29.

Remark: For SDRAM operation, set CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY in the EMCDELAYCLK register.

Fig 36. SDRAM timing

11.16 USB interface

Table 30. Dynamic characteristics: USB0 and USB1 pins (full-speed)
C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(IO)}$; 3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4	-	20	ns
t_f	fall time	10 % to 90 %		4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90	-	111.11	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 37		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 37		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 37	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 37	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Remark: If only USB0 (HS USB) is used, the pins VDDREG and VDDIO can be at different voltages within the operating range but should have the same ramp up time. If USB1(FS USB) is used, the pins VDDREG and VDDIO should be a minimum of 3.0 V and be tied together.

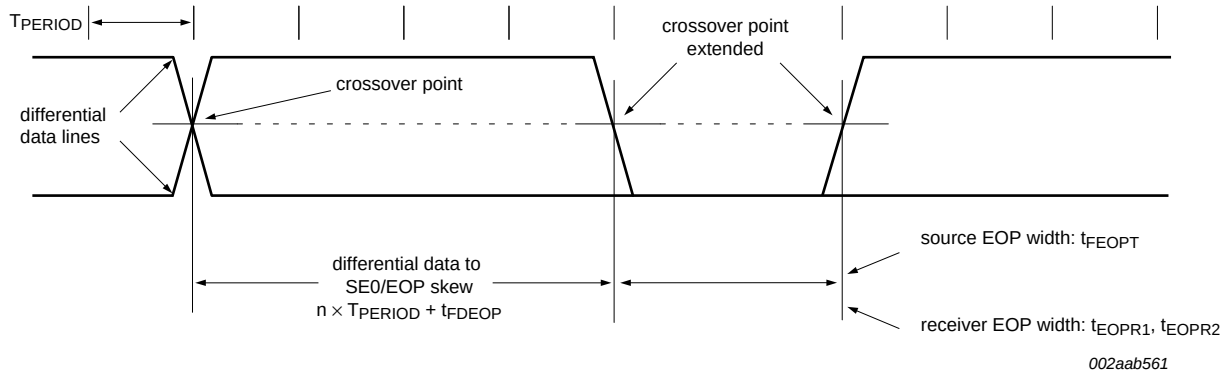


Fig 37. Differential data-to-EOP transition skew and EOP width

Table 41. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode *…continued*

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
12 MHz	< 160 Ω	18 pF, 18 pF
	< 160 Ω	39 pF, 39 pF
16 MHz	< 120 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF
20 MHz	<100 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF

Table 42. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{x2}
15 MHz	< 80 Ω	18 pF, 18 pF
20 MHz	< 80 Ω	39 pF, 39 pF
	< 100 Ω	47 pF, 47 pF

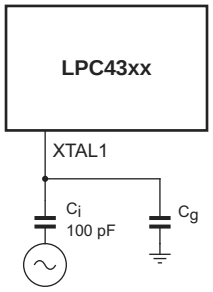


Fig 43. Slave mode operation of the on-chip oscillator

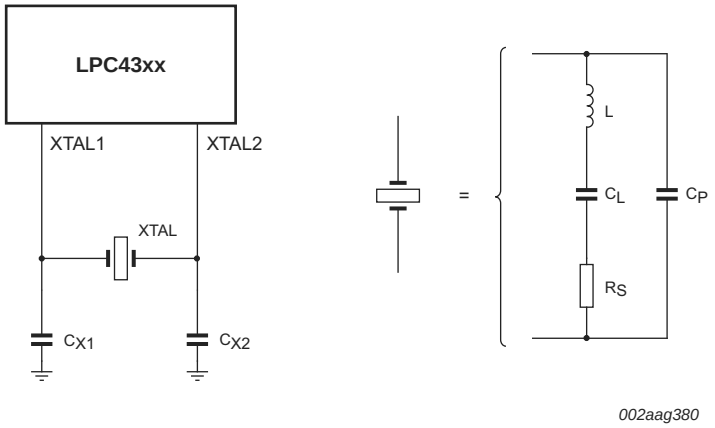
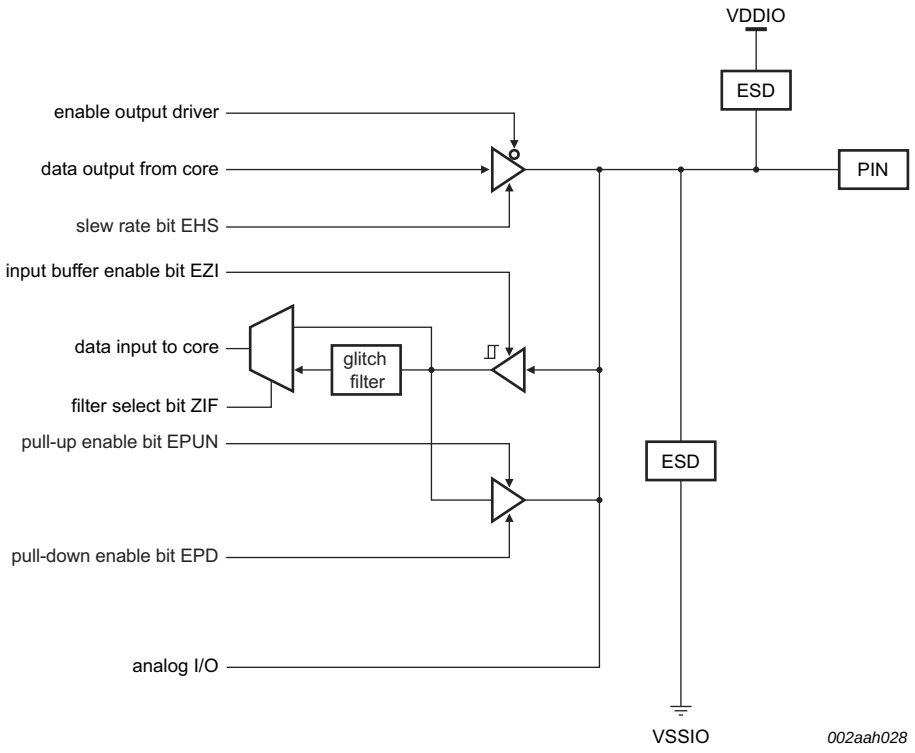


Fig 44. Oscillator modes with external crystal model used for C_{X1}/C_{X2} evaluation



The glitch filter rejects pulses of typical 12 ns width.

Fig 46. Standard I/O pin configuration with analog input

13.6 Reset pin configuration

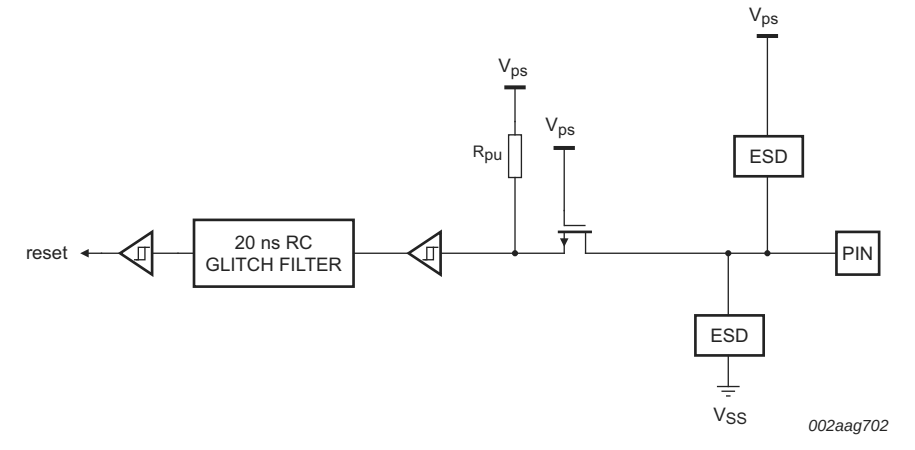
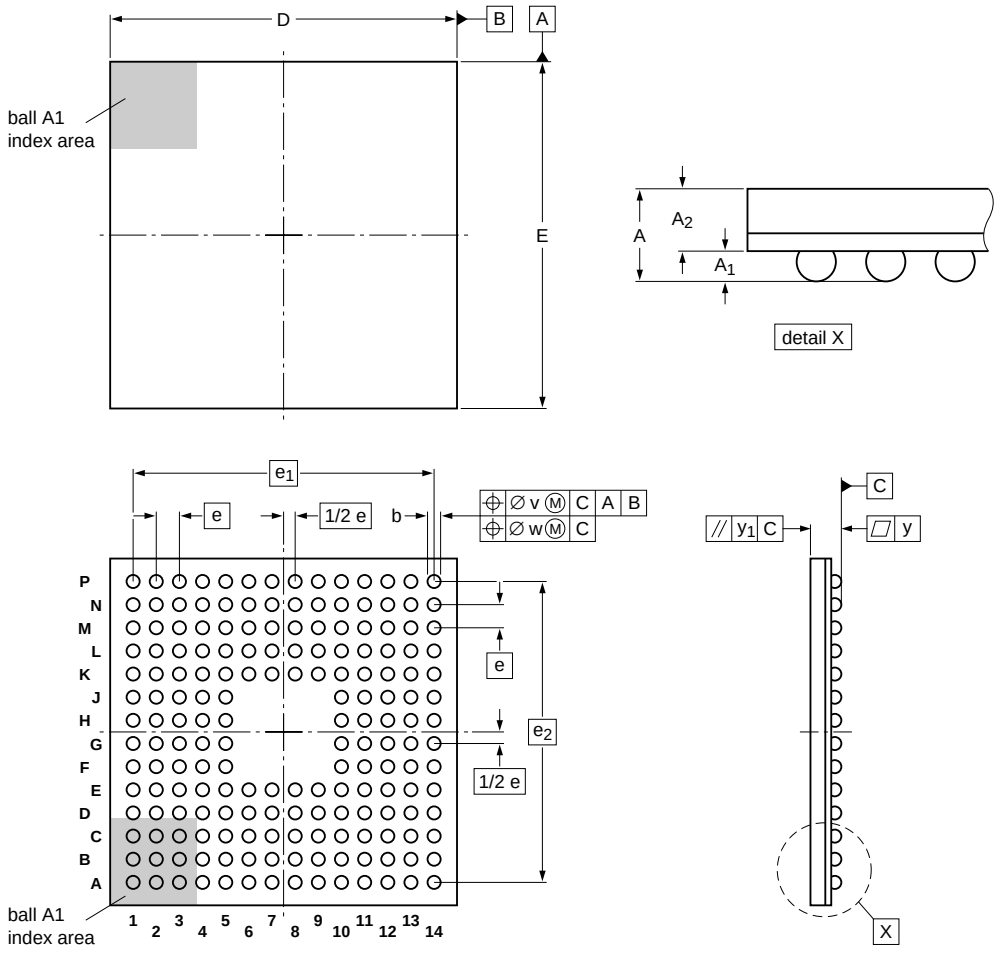


Fig 47. Reset pin configuration

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



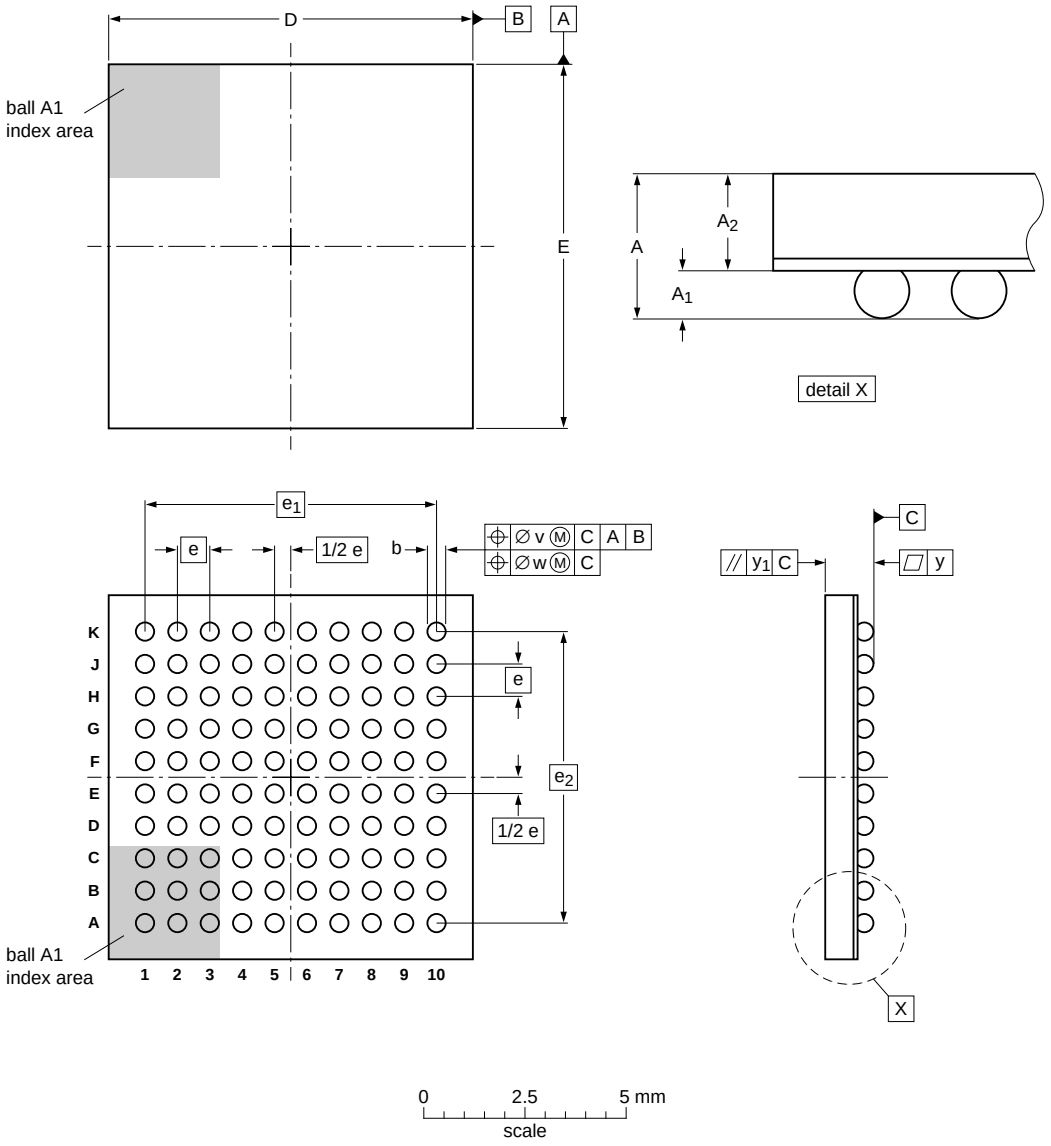
DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 52. Package outline of the TFBGA180 package

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 53. Package outline of the TFBGA100 package