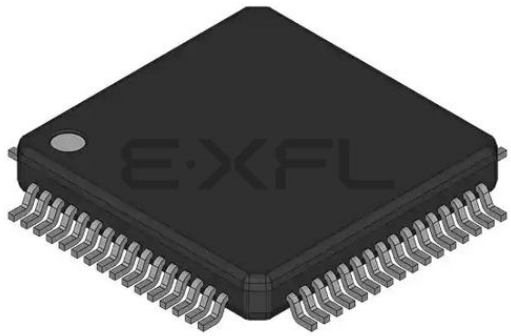

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	53
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc908gr32acfue

List of Chapters

- Master reset pin and power-on reset (POR)
- On-chip FLASH memory:
  - MC68HC908GR60A — 60 Kbytes
  - MC68HC908GR48A — 48 Kbytes
  - MC68HC908GR32A — 32 Kbytes
- Random-access memory (RAM):
  - MC68HC908GR60A — 2048 bytes
  - MC68HC908GR48A — 1536 bytes
  - MC68HC908GR32A — 1536 bytes
- Serial peripheral interface (SPI) module
- Enhanced serial communications interface (ESCI) module
- One 16-bit, 2-channel timer interface module (TIM1) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- One 16-bit, 6-channel timer interface module (TIM2) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- Timebase module with clock prescaler circuitry for eight user selectable periodic real-time interrupts with optional active clock source during stop mode for periodic wakeup from stop using an external crystal
- 24-channel, 10-bit successive approximation analog-to-digital converter (ADC)
- 8-bit keyboard wakeup port with software selectable rising or falling edge detect, as well as high or low level detection
- Up to 53 general-purpose input/output (I/O) pins, including:
  - 40 shared-function I/O pins, depending on package choice
  - Up to 13 dedicated I/O pins, depending on package choice
- Selectable pullups on inputs only on ports A, C, and D. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce customer system cost
- High current 10-mA sink/source capability on all port pins
- Higher current 20-mA sink/source capability on PTC0–PTC4 and PTF0–PTF3
- User selectable clockout feature with divide by 1, 2, and 4 of the bus or crystal frequency
- User selection of having the oscillator enabled or disabled during stop mode
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Available packages:
  - 32-pin low-profile quad flat pack (LQFP)
  - 48-pin low-profile quad flat pack (LQFP)
  - 64-pin quad flat pack (QFP)
- Specific features in 32-pin LQFP are:
  - Port A is only 4 bits: PTA0–PTA3; shared with ADC and KBI modules
  - Port B is only 6 bits: PTB0–PTB5; shared with ADC module
  - Port C is only 2 bits: PTC0–PTC1
  - Port D is only 7 bits: PTD0–PTD6; shared with SPI, TIM1 and TIM2 modules
  - Port E is only 2 bits: PTE0–PTE1; shared with ESCI module

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0459	TIM2 Channel 3 Status and Control Register (T2SC3) See page 255.	Read:	CH3F	CH3IE	0	MS3A	ELS3B	ELS3A	TOV3	CH3MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$045A	TIM2 Channel 3 Register High (T2CH3H) See page 258.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$045B	TIM2 Channel 3 Register Low (T2CH3L) See page 258.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$045C	TIM2 Channel 4 Status and Control Register (T2SC4) See page 255.	Read:	CH4F	CH4IE	MS4B	MS4A	ELS4B	ELS4A	TOV4	CH4MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$045D	TIM2 Channel 4 Register High (T2CH4H) See page 258.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$045E	TIM2 Channel 4 Register Low (T2CH4L) See page 258.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$045F	TIM2 Channel 5 Status and Control Register (T2SC5) See page 255.	Read:	CH5F	CH5IE	0	MS5A	ELS5B	ELS5A	TOV 5	CH5MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0460	TIM2 Channel 5 Register High (T2CH5H) See page 258.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$0461	TIM2 Channel 5 Register Low (T2CH5L) See page 258.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$FE00	Break Status Register (BSR) See page 199.	Read:	R	R	R	R	R	R	SBSW	R
		Write:							NOTE 1	
		Reset:	0	0	0	0	0	0	0	0

1. Writing a 0 clears SBSW.

$FE01	SIM Reset Status Register (SRSR) See page 199.	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
		Write:								
		POR:	1	0	0	0	0	0	0	0
$FE02	Reserved	Read:	R	R	R	R	R	R	R	R
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 7 of 9)

When bits within FL2BPR are programmed (0), they lock a block of memory address ranges as shown in 2.7.2.2 FLASH-2 Block Protect Register. If FL2BPR is programmed with any value other than $FF, the protected block of FLASH memory can not be erased or programmed.

NOTE

The vector locations and the FLASH block protect registers are located in the same page. FL1BPR and FL2BPR are not protected with special hardware or software. Therefore, if this page is not protected by FL1BPR and the vector locations are erased by either a page or a mass erase operation, both FL1BPR and FL2BPR will also get erased.

2.7.4 FLASH-2 Mass Erase Operation

Use this step-by-step procedure to erase the entire FLASH-2 memory:

1. Set both the ERASE bit and the MASS bit in the FLASH-2 control register (FL2CR).
2. Read the FLASH-2 block protect register (FL2BPR).

NOTE

Mass erase is disabled whenever any block is protected (FL2BPR does not equal $FF).

3. Write to any FLASH-2 address within the FLASH-2 array with any data.
4. Wait for a time, t_{NVS} (minimum 10 μs).
5. Set the HVEN bit.
6. Wait for a time, t_{MERASE} (minimum 4 ms).
7. Clear the ERASE and MASS bits.
8. Wait for a time, t_{NVHL} (minimum 100 μs).
9. Clear the HVEN bit.
10. Wait for a time, t_{RCV}, (typically 1 μs) after which the memory can be accessed in normal read mode.

NOTE

A. *Programming and erasing of FLASH locations can not be performed by code being executed from the same FLASH array.*

B. *While these operations must be performed in the order shown, other unrelated operations may occur between the steps. However, care must be taken to ensure that these operations do not access any address within the FLASH array memory space such as the COP control register (COPCTL) at $FFFF.*

C. *It is highly recommended that interrupts be disabled during program/erase operations.*

Table 7-1. Instruction Set Summary (Sheet 6 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	–	–	1	–	–	–	INH	83		9
TAP	Transfer A to CCR	CCR ← (A)	↕	↕	↕	↕	↕	↕	INH	84		2
TAX	Transfer A to X	X ← (A)	–	–	–	–	–	–	INH	97		1
TPA	Transfer CCR to A	A ← (CCR)	–	–	–	–	–	–	INH	85		1
TST *opr* TSTA TSTX TST *opr*,X TST ,X TST *opr*,SP	Test for Negative or Zero	(A) – $00 or (X) – $00 or (M) – $00	0	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3D 4D 5D 6D 7D 9E6D	dd ff ff	3 1 1 3 2 4
TSX	Transfer SP to H:X	H:X ← (SP) + 1	–	–	–	–	–	–	INH	95		2
TXA	Transfer X to A	A ← (X)	–	–	–	–	–	–	INH	9F		1
TXS	Transfer H:X to SP	(SP) ← (H:X) – 1	–	–	–	–	–	–	INH	94		2
WAIT	Enable Interrupts; Wait for Interrupt	I bit ← 0; Inhibit CPU clocking until interrupted	–	–	0	–	–	–	INH	8F		1

A	Accumulator
C	Carry/borrow bit
CCR	Condition code register
dd	Direct address of operand
dd rr	Direct address of operand and relative offset of branch instruction
DD	Direct to direct addressing mode
DIR	Direct addressing mode
DIX+	Direct to indexed with post increment addressing mode
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing
EXT	Extended addressing mode
ff	Offset byte in indexed, 8-bit offset addressing
H	Half-carry bit
H	Index register high byte
hh ll	High and low bytes of operand address in extended addressing
I	Interrupt mask
ii	Immediate operand byte
IMD	Immediate source to direct destination addressing mode
IMM	Immediate addressing mode
INH	Inherent addressing mode
IX	Indexed, no offset addressing mode
IX+	Indexed, no offset, post increment addressing mode
IX+D	Indexed with post increment to direct addressing mode
IX1	Indexed, 8-bit offset addressing mode
IX1+	Indexed, 8-bit offset, post increment addressing mode
IX2	Indexed, 16-bit offset addressing mode
M	Memory location
N	Negative bit
n	Any bit
opr	Operand (one or two bytes)
PC	Program counter
PCH	Program counter high byte
PCL	Program counter low byte
REL	Relative addressing mode
rel	Relative program counter offset byte
rr	Relative program counter offset byte
SP1	Stack pointer, 8-bit offset addressing mode
SP2	Stack pointer 16-bit offset addressing mode
SP	Stack pointer
U	Undefined
V	Overflow bit
X	Index register low byte
Z	Zero bit
&	Logical AND
|	Logical OR
⊕	Logical EXCLUSIVE OR
( )	Contents of
–( )	Negation (two's complement)
#	Immediate value
«	Sign extend
←	Loaded with
?	If
:	Concatenated with
↕	Set or cleared
—	Not affected

7.8 Opcode Map

See Table 7-2.

8.6 IRQ Status and Control Register

The IRQ status and control register (INTSCR) controls and monitors operation of the IRQ module. The INTSCR:

- Shows the state of the IRQ flag
- Clears the IRQ latch
- Masks IRQ interrupt request
- Controls triggering sensitivity of the $\overline{\text{IRQ}}$ interrupt pin

Address: $001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IRQF	0	IMASK	MODE
Write:						ACK		
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 8-3. IRQ Status and Control Register (INTSCR)

IRQF — IRQ Flag Bit

This read-only status bit is high when the IRQ interrupt is pending.

1 = $\overline{\text{IRQ}}$ interrupt pending
0 = $\overline{\text{IRQ}}$ interrupt not pending

ACK — IRQ Interrupt Request Acknowledge Bit

Writing a 1 to this write-only bit clears the IRQ latch. ACK always reads as 0. Reset clears ACK.

IMASK — IRQ Interrupt Mask Bit

Writing a 1 to this read/write bit disables IRQ interrupt requests. Reset clears IMASK.

1 = IRQ interrupt requests disabled
0 = IRQ interrupt requests enabled

MODE — IRQ Edge/Level Select Bit

This read/write bit controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin. Reset clears MODE.

1 = $\overline{\text{IRQ}}$ interrupt requests on falling edges and low levels
0 = $\overline{\text{IRQ}}$ interrupt requests on falling edges only

10.7 External Interrupt Module (IRQ)

10.7.1 Wait Mode

The external interrupt (IRQ) module remains active in wait mode. Clearing the IMASK bit in the IRQ status and control register enables $\overline{\text{IRQ}}$ CPU interrupt requests to bring the MCU out of wait mode.

10.7.2 Stop Mode

The IRQ module remains active in stop mode. Clearing the IMASK bit in the IRQ status and control register enables $\overline{\text{IRQ}}$ CPU interrupt requests to bring the MCU out of stop mode.

10.8 Keyboard Interrupt Module (KBI)

10.8.1 Wait Mode

The keyboard interrupt (KBI) module remains active in wait mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

10.8.2 Stop Mode

The keyboard module remains active in stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

10.9 Low-Voltage Inhibit Module (LVI)

10.9.1 Wait Mode

If enabled, the low-voltage inhibit (LVI) module remains active in wait mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of wait mode.

10.9.2 Stop Mode

If enabled, the LVI module remains active in stop mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of stop mode.

10.10 Enhanced Serial Communications Interface Module (ESCI)

10.10.1 Wait Mode

The enhanced serial communications interface (ESCI), or SCI module for short, module remains active in wait mode. Any enabled CPU interrupt request from the SCI module can bring the MCU out of wait mode.

If SCI module functions are not required during wait mode, reduce power consumption by disabling the module before executing the WAIT instruction.

10.10.2 Stop Mode

The SCI module is inactive in stop mode. The STOP instruction does not affect SCI register states. SCI module operation resumes after the MCU exits stop mode.

Because the internal clock is inactive during stop mode, entering stop mode during an SCI transmission or reception results in invalid data.

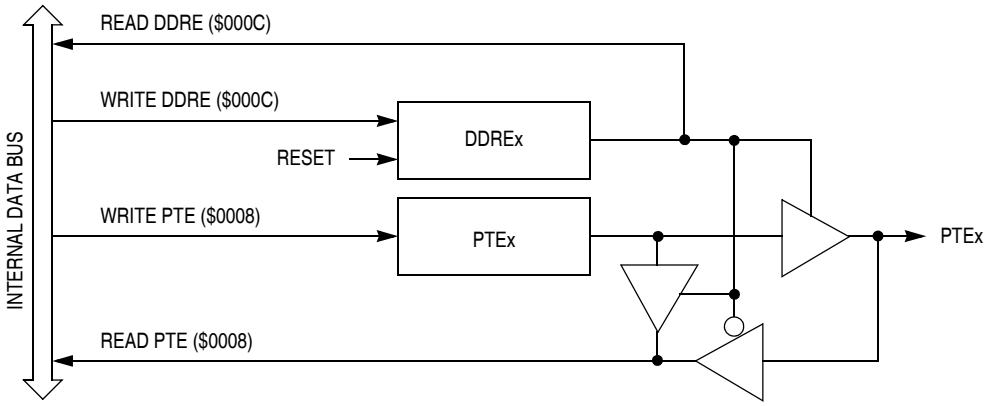

Figure 12-19. Port E I/O Circuit

Table 12-6. Port E Pin Functions

DDRE Bit	PTE Bit	I/O Pin Mode	Accesses to DDRE	Accesses to PTE	
			Read/Write	Read	Write
0	X(1)	Input, Hi-Z(2)	DDRE5–DDRE0	Pin	PTE5–PTE0(3)
1	X	Output	DDRE5–DDRE0	PTE5–PTE0	PTE5–PTE0

1. X = Don't care
2. Hi-Z = High impedance
3. Writing affects data register, but does not affect input.

12.8 Port F

Port F is an 8-bit special-function port that shares four of its pins with the timer interface (TIM2) module.

12.8.1 Port F Data Register

The port F data register (PTF) contains a data latch for each of the eight port F pins.

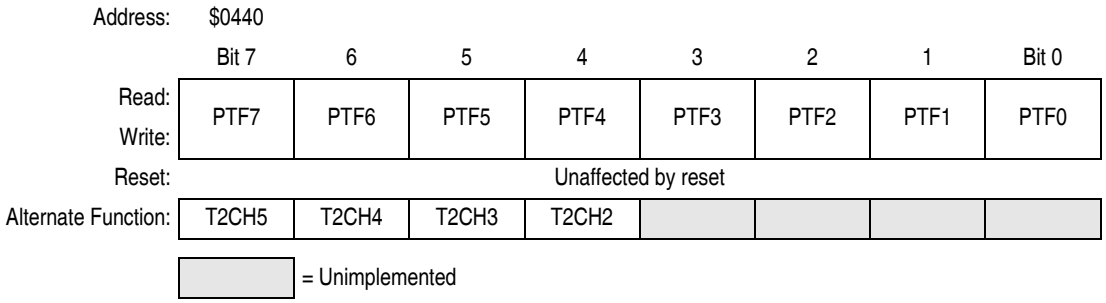

Figure 12-20. Port F Data Register (PTF)

PTF7–PTF0 — Port F Data Bits

These read/write bits are software-programmable. Data direction of each port F pin is under the control of the corresponding bit in data direction register F. Reset has no effect on port F data.

12.9.2 Data Direction Register G

Data direction register G (DDRG) determines whether each port G pin is an input or an output. Writing a 1 to a DDRG bit enables the output buffer for the corresponding port G pin; a 0 disables the output buffer.

Address: $0445

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRG7	DDRG6	DDRG5	DDRG4	DDRG3	DDRG2	DDRG1	DDRG0
Reset:	0	0	0	0	0	0	0	0

Figure 12-24. Data Direction Register G (DDRG)

DDRG7–DDRG0 — Data Direction Register G Bits

These read/write bits control port G data direction. Reset clears DDRG7–DDRG0], configuring all port G pins as inputs.

1 = Corresponding port G pin configured as output
0 = Corresponding port G pin configured as input

NOTE

Avoid glitches on port G pins by writing to the port G data register before changing data direction register G bits from 0 to 1.

Figure 12-25 shows the port G I/O logic.

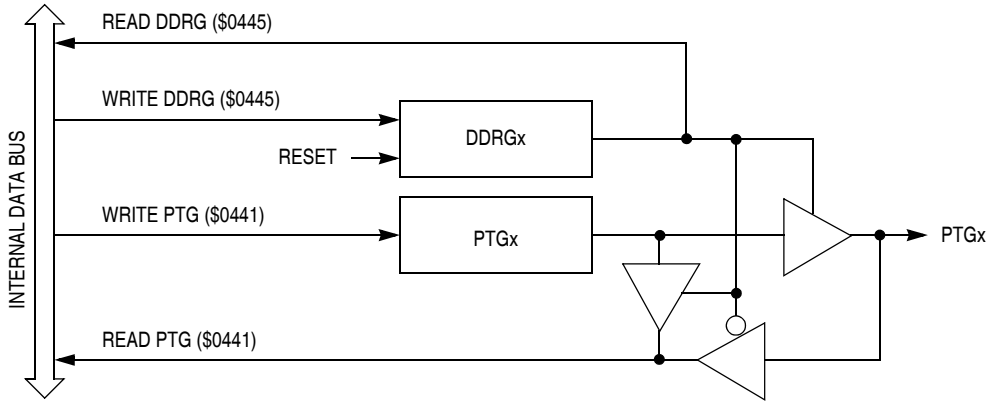

Figure 12-25. Port G I/O Circuit

When bit DDRGx is a 1, reading address $0441 reads the PTGx data latch. When bit DDRGx is a 0, reading address $0441 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 12-8 summarizes the operation of the port G pins.

Table 12-8. Port G Pin Functions

DDRG Bit	PTG Bit	I/O Pin Mode	Accesses to DDRG	Accesses to PTG	
			Read/Write	Read	Write
0	X[1]	Input, Hi-Z[2]	DDRG7–DDRG0	Pin	PTG7–PTG0[3]
1	X	Output	DDRG7–DDRG0	PTG7–PTG0	PTG7–PTG0

1. X = Don't care
2. Hi-Z = High impedance
3. Writing affects data register, but does not affect input.

Chapter 13
Enhanced Serial Communications Interface (ESCI) Module

13.1 Introduction

The enhanced serial communications interface (ESCI) module allows asynchronous communications with peripheral devices and other microcontroller units (MCU).

13.2 Features

Features include:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Programmable baud rates
- Programmable 8-bit or 9-bit character length
- Separately enabled transmitter and receiver
- Separate receiver and transmitter central processor unit (CPU) interrupt requests
- Programmable transmitter output polarity
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight interrupt flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

Interrupt Status Register 4

Address: $FE07

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	IF24	IF23
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 14-15. Interrupt Status Register 4 (INT4)

Bits 7–2 — Always read 0

IF24–IF23 — Interrupt Flags 24–23

These flags indicate the presence of an interrupt request from the source shown in Table 14-3.

1 = Interrupt request present

0 = No interrupt request present

14.5.2 Reset

All reset sources always have equal and highest priority and cannot be arbitrated.

14.5.3 Break Interrupts

The break module can stop normal program flow at a software-programmable break point by asserting its break interrupt output (see Chapter 17 Timer Interface Module (TIM1) and Chapter 18 Timer Interface Module (TIM2)). The SIM puts the CPU into the break state by forcing it to the SWI vector location. Refer to the break interrupt subsection of each module to see how each module is affected by the break state.

14.5.4 Status Flag Protection in Break Mode

The SIM controls whether status flags contained in other modules can be cleared during break mode. The user can select whether flags are protected from being cleared by properly initializing the break clear flag enable bit (BCFE) in the SIM break flag control register (BFCR).

Protecting flags in break mode ensures that set flags will not be cleared while in break mode. This protection allows registers to be freely read and written during break mode without losing status flag information.

Setting the BCFE bit enables the clearing mechanisms. Once cleared in break mode, a flag remains cleared even when break mode is exited. Status flags with a 2-step clearing mechanism — for example, a read of one register followed by the read or write of another — are protected, even when the first step is accomplished prior to entering break mode. Upon leaving break mode, execution of the second step will clear the flag as normal.

14.6 Low-Power Modes

Executing the WAIT or STOP instruction puts the MCU in a low power-consumption mode for standby situations. The SIM holds the CPU in a non-clocked state. The operation of each of these modes is described in the following subsections. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupts to occur.

POR — Power-On Reset Bit

1 = Last reset caused by POR circuit
0 = Read of SRSR

PIN — External Reset Bit

1 = Last reset caused by external reset pin ($\overline{RST}$)
0 = POR or read of SRSR

COP — Computer Operating Properly Reset Bit

1 = Last reset caused by COP counter
0 = POR or read of SRSR

ILOP — Illegal Opcode Reset Bit

1 = Last reset caused by an illegal opcode
0 = POR or read of SRSR

ILAD — Illegal Address Reset Bit (opcode fetches only)

1 = Last reset caused by an opcode fetch from an illegal address
0 = POR or read of SRSR

MODRST — Monitor Mode Entry Module Reset Bit

1 = Last reset caused by monitor mode entry when vector locations $FFFE and $FFFF are $FF after POR while $\overline{IRQ} = V_{DD}$
0 = POR or read of SRSR

LVI — Low-Voltage Inhibit Reset Bit

1 = Last reset caused by the LVI circuit
0 = POR or read of SRSR

14.7.3 Break Flag Control Register

The break flag control register contains a bit that enables software to clear status bits while the MCU is in a break state.

Address: $FE03

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	BCFE	R	R	R	R	R	R	R
Reset:	0							

R = Reserved

Figure 14-23. Break Flag Control Register (BFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break
0 = Status bits not clearable during break

Address: $0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

= Unimplemented

Figure 17-5. TIM1 Status and Control Register (T1SC)

TOF — TIM1 Overflow Flag Bit

This read/write flag is set when the TIM1 counter reaches the modulo value programmed in the TIM1 counter modulo registers. Clear TOF by reading the TIM1 status and control register when TOF is set and then writing a 0 to TOF. If another TIM1 overflow occurs before the clearing sequence is complete, then writing 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a 1 to TOF has no effect.

1 = TIM1 counter has reached modulo value
0 = TIM1 counter has not reached modulo value

TOIE — TIM1 Overflow Interrupt Enable Bit

This read/write bit enables TIM1 overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM1 overflow interrupts enabled
0 = TIM1 overflow interrupts disabled

TSTOP — TIM1 Stop Bit

This read/write bit stops the TIM1 counter. Counting resumes when TSTOP is cleared. Reset sets the TSTOP bit, stopping the TIM1 counter until software clears the TSTOP bit.

1 = TIM1 counter stopped
0 = TIM1 counter active

NOTE

Do not set the TSTOP bit before entering wait mode if the TIM1 is required to exit wait mode. Also, when the TSTOP bit is set and the timer is configured for input capture operation, input captures are inhibited until the TSTOP bit is cleared.

TRST — TIM1 Reset Bit

Setting this write-only bit resets the TIM1 counter and the TIM1 prescaler. Setting TRST has no effect on any other registers. Counting resumes from $0000. TRST is cleared automatically after the TIM1 counter is reset and always reads as 0. Reset clears the TRST bit.

1 = Prescaler and TIM1 counter cleared
0 = No effect

NOTE

Setting the TSTOP and TRST bits simultaneously stops the TIM1 counter at a value of $0000.

Address: $0025 T1SC0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

Address: $0028 T1SC1

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 17-8. TIM1 Channel Status and Control Registers (T1SC0:T1SC1)

CHxF — Channel x Flag Bit

When channel x is an input capture channel, this read/write bit is set when an active edge occurs on the channel x pin. When channel x is an output compare channel, CHxF is set when the value in the TIM1 counter registers matches the value in the TIM1 channel x registers.

Clear CHxF by reading the TIM1 channel x status and control register with CHxF set and then writing a 0 to CHxF. If another interrupt request occurs before the clearing sequence is complete, then writing 0 to CHxF has no effect. Therefore, an interrupt request cannot be lost due to inadvertent clearing of CHxF.

Reset clears the CHxF bit. Writing a 1 to CHxF has no effect.

1 = Input capture or output compare on channel x
0 = No input capture or output compare on channel x

CHxIE — Channel x Interrupt Enable Bit

This read/write bit enables TIM1 CPU interrupt service requests on channel x. Reset clears the CHxIE bit.

1 = Channel x CPU interrupt requests enabled
0 = Channel x CPU interrupt requests disabled

MSxB — Mode Select Bit B

This read/write bit selects buffered output compare/PWM operation. MSxB exists only in the TIM1 channel 0 status and control register.

Setting MS0B disables the channel 1 status and control register and reverts T1CH1 to general-purpose I/O.

Reset clears the MSxB bit.

1 = Buffered output compare/PWM operation enabled
0 = Buffered output compare/PWM operation disabled

MSxA — Mode Select Bit A

When ELSxB:A ≠ 00, this read/write bit selects either input capture operation or unbuffered output compare/PWM operation. See Table 17-2.

1 = Unbuffered output compare/PWM operation
0 = Input capture operation

Chapter 18
Timer Interface Module (TIM2)

18.1 Introduction

This section describes the timer interface module (TIM2). The TIM2 is a 6-channel timer that provides a timing reference with input capture, output compare, and pulse-width-modulation functions. Figure 18-2 is a block diagram of the TIM2.

18.2 Features

Features of the TIM2 include:

- Six input capture/output compare channels:
  - Rising-edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
- Buffered and unbuffered pulse width modulation (PWM) signal generation
- Programmable TIM2 clock input
  - 7-frequency internal bus clock prescaler selection
  - External TIM2 clock input (4-MHz maximum frequency)
- Free-running or modulo up-count operation
- Toggle any channel pin on overflow
- TIM2 counter stop and reset bits

18.3 Functional Description

Figure 18-2 shows the TIM2 structure. The central component of the TIM2 is the 16-bit TIM2 counter that can operate as a free-running counter or a modulo up-counter. The TIM2 counter provides the timing reference for the input capture and output compare functions. The TIM2 counter modulo registers, T2MODH:T2MODL, control the modulo value of the TIM2 counter. Software can read the TIM2 counter value at any time without affecting the counting sequence.

The six TIM2 channels are programmable independently as input capture or output compare channels.

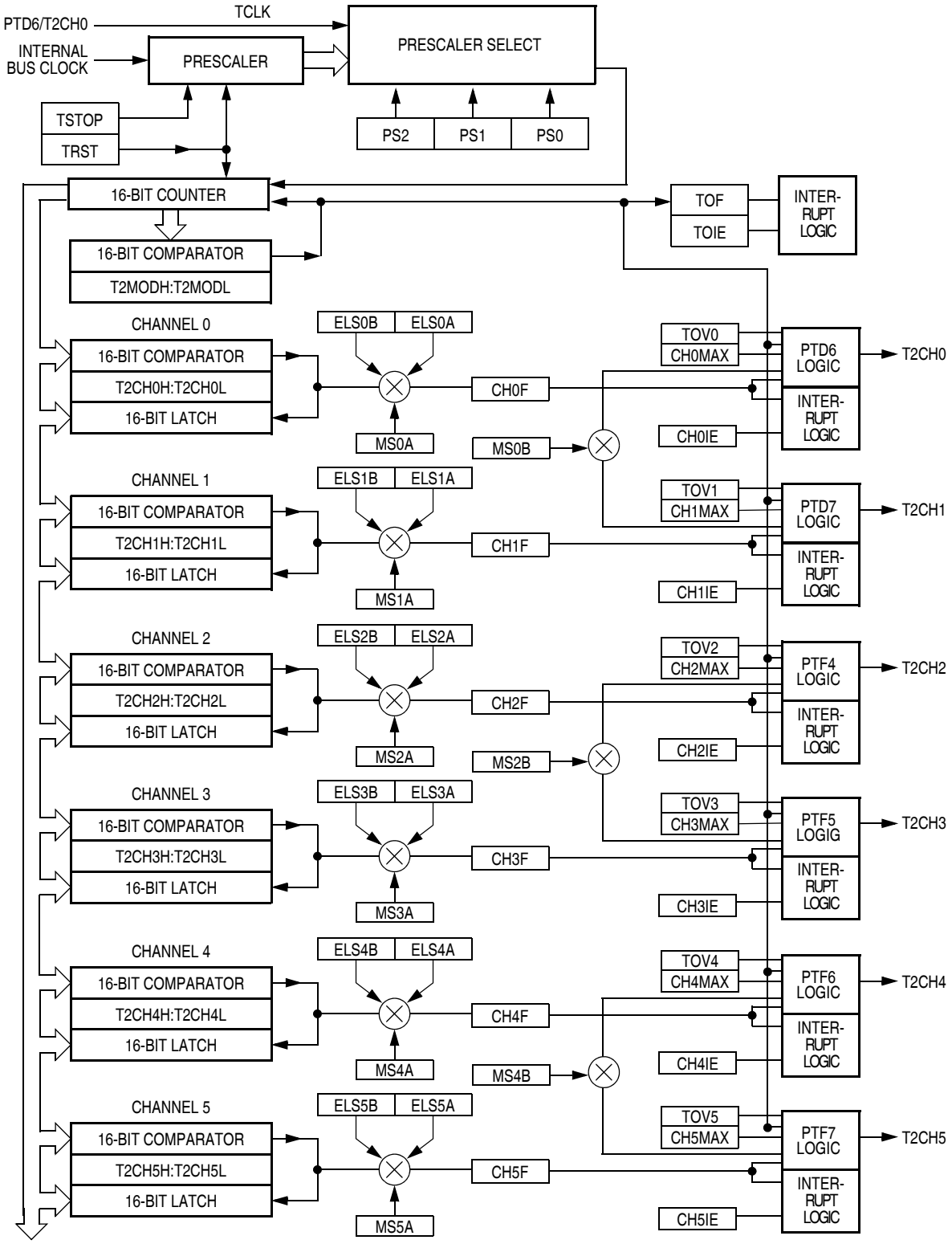

Figure 18-2. TIM2 Block Diagram

CHxF — Channel x Flag Bit

When channel x is an input capture channel, this read/write bit is set when an active edge occurs on the channel x pin. When channel x is an output compare channel, CHxF is set when the value in the TIM2 counter registers matches the value in the TIM2 channel x registers.

When CHxIE = 1, clear CHxF by reading TIM2 channel x status and control register with CHxF set, and then writing a 0 to CHxF. If another interrupt request occurs before the clearing sequence is complete, then writing 0 to CHxF has no effect. Therefore, an interrupt request cannot be lost due to inadvertent clearing of CHxF.

Reset clears the CHxF bit. Writing a 1 to CHxF has no effect.

1 = Input capture or output compare on channel x
0 = No input capture or output compare on channel x

CHxIE — Channel x Interrupt Enable Bit

This read/write bit enables TIM2 CPU interrupts on channel x.
Reset clears the CHxIE bit.

1 = Channel x CPU interrupt requests enabled
0 = Channel x CPU interrupt requests disabled

MSxB — Mode Select Bit B

This read/write bit selects buffered output compare/PWM operation. MSxB exists only in the TIM2 channel 0, TIM2 channel 2, and TIM2 channel 4 status and control registers.

Setting MS0B disables the channel 1 status and control register and reverts T2CH1 pin to general-purpose I/O.

Setting MS2B disables the channel 3 status and control register and reverts T2CH3 pin to general-purpose I/O.

Setting MS4B disables the channel 5 status and control register and reverts T2CH5 pin to general-purpose I/O.

Reset clears the MSxB bit.

1 = Buffered output compare/PWM operation enabled
0 = Buffered output compare/PWM operation disabled

MSxA — Mode Select Bit A

When ELSxB:ELSxA ≠ 00, this read/write bit selects either input capture operation or unbuffered output compare/PWM operation. (See Table 18-2.)

1 = Unbuffered output compare/PWM operation
0 = Input capture operation

When ELSxB:ELSxA = 00, this read/write bit selects the initial output level of the T2CHx pin once PWM, input capture, or output compare operation is enabled. (See Table 18-2.) Reset clears the MSxA bit.

1 = Initial output level low
0 = Initial output level high

NOTE

Before changing a channel function by writing to the MSxB or MSxA bit, set the TSTOP and TRST bits in the TIM2 status and control register (T2SC).

19.3.1.4 Data Format

Communication with the monitor ROM is in standard non-return-to-zero (NRZ) mark/space data format. Transmit and receive baud rates must be identical.

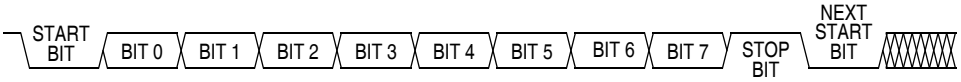

Figure 19-12. Monitor Data Format

19.3.1.5 Break Signal

A start bit (0) followed by nine 0 bits is a break signal. When the monitor receives a break signal, it drives the PTA0 pin high for the duration of approximately two bits and then echoes back the break signal.

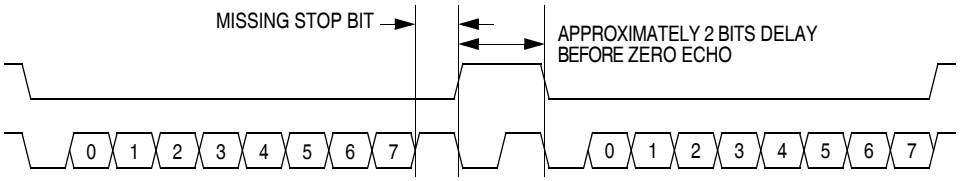

Figure 19-13. Break Transaction

19.3.1.6 Baud Rate

The communication baud rate is controlled by the crystal frequency or external clock and the state of the PTB4 pin (when $\overline{IRQ}$ is set to V_{TST}) upon entry into monitor mode. If monitor mode was entered with V_{DD} on $\overline{IRQ}$ and the reset vector blank, then the baud rate is independent of PTB4.

Table 19-1 also lists external frequencies required to achieve a standard baud rate of 7200 bps. The effective baud rate is the bus frequency divided by 278. If using a crystal as the clock source, be aware of the upper frequency limit that the internal clock module can handle. See 20.7 5.0-Volt Control Timing or 20.8 3.3-Volt Control Timing for this limit.

19.3.1.7 Commands

The monitor ROM firmware uses these commands:

- READ (read memory)
- WRITE (write memory)
- IREAD (indexed read)
- IWRITE (indexed write)
- READSP (read stack pointer)
- RUN (run user program)

The monitor ROM firmware echoes each received byte back to the PTA0 pin for error checking. An 11-bit delay at the end of each command allows the host to send a break character to cancel the command. A delay of two bit times occurs before each echo and before READ, IREAD, or READSP data is returned. The data returned by a read command appears after the echo of the last byte of the command.

NOTE

Wait one bit time after each echo before sending the next byte.

19.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

NOTE

Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors.

During monitor mode entry, the MCU waits after the power-on reset for the host to send the eight security bytes on pin PTA0. If the received bytes match those at locations $FFF6–$FFFD, the host bypasses the security feature and can read all FLASH locations and execute code from FLASH. Security remains bypassed until a power-on reset occurs. If the reset was not a power-on reset, security remains bypassed and security code entry is not required. See Figure 19-17.

Upon power-on reset, if the received bytes of the security code do not match the data at locations $FFF6–$FFFD, the host fails to bypass the security feature. The MCU remains in monitor mode, but reading a FLASH location returns an invalid value and trying to execute code from FLASH causes an illegal address reset. After receiving the eight security bytes from the host, the MCU transmits a break character, signifying that it is ready to receive a command.

NOTE

The MCU does not transmit a break character until after the host sends the eight security bytes.

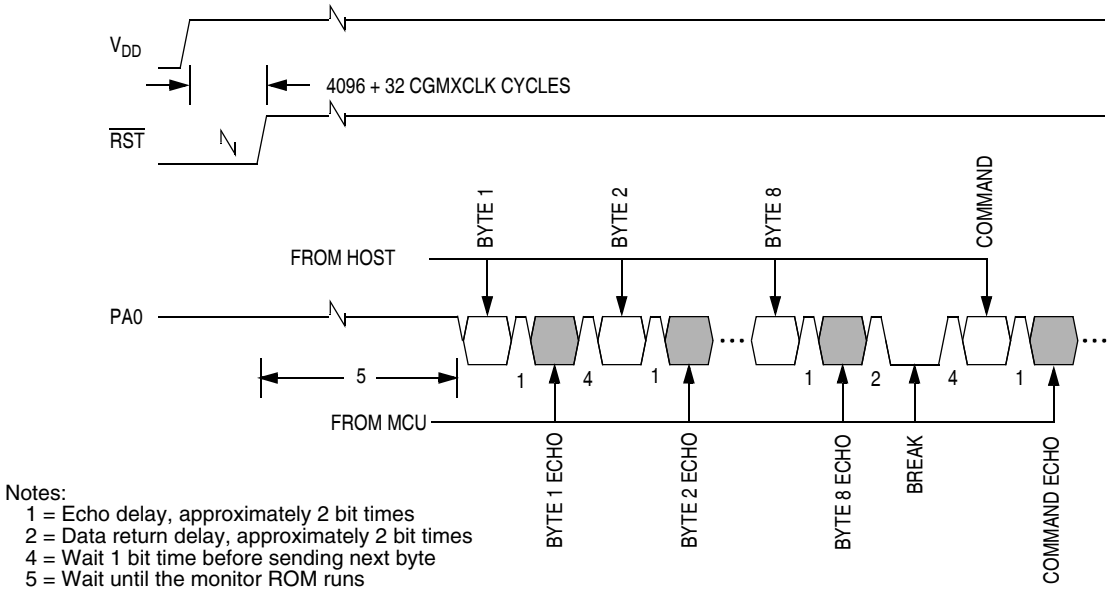

Figure 19-17. Monitor Mode Entry Timing

To determine whether the security code entered is correct, check to see if bit 6 of RAM address $40 is set. If it is, then the correct security code has been entered and FLASH can be accessed.

If the security sequence fails, the device should be reset by a power-on reset and brought up in monitor mode to attempt another entry. After failing the security sequence, the FLASH module can also be mass erased by executing an erase routine that was downloaded into internal RAM. The mass erase operation clears the security code locations so that all eight security bytes become $FF (blank).

20.3 Functional Operating Range

Characteristic	Symbol	Value	Unit
Operating temperature range	T_A	–40 to +125	°C
Operating voltage range	V_{DD}	5.0 ±10% 3.3 ±10%	V

20.4 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance 32-pin LQFP 48-pin LQFP 64-pin QFP	θ_{JA}	 95 95 54	°C/W
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation(1)	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O} = K/(T_J + 273\ °C)$	W
Constant(2)	K	$P_D \times (T_A + 273\ °C) + P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	T_J	$T_A + (P_D \times \theta_{JA})$	°C

1. Power dissipation is a function of temperature.
2. K is a constant unique to the device. K can be determined for a known T_A and measured P_D. With this value of K, P_D and T_J can be determined for any value of T_A.