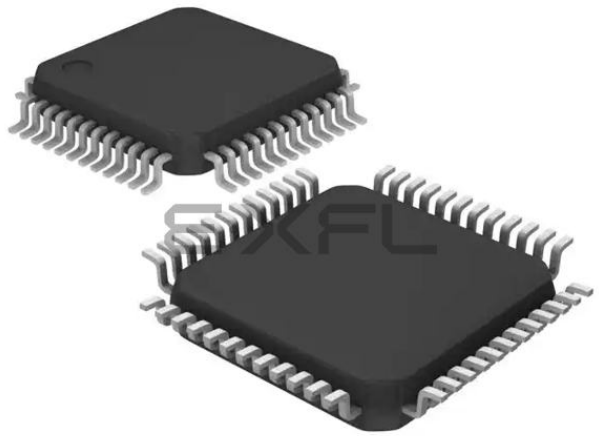

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Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908gr32amfae

Chapter 17
Timer Interface Module (TIM1)

17.1 Introduction . . . 225
17.2 Features . . . 225
17.3 Functional Description . . . 225
17.3.1 TIM1 Counter Prescaler . . . 228
17.3.2 Input Capture . . . 228
17.3.3 Output Compare . . . 229
17.3.3.1 Unbuffered Output Compare . . . 229
17.3.3.2 Buffered Output Compare . . . 229
17.3.4 Pulse Width Modulation (PWM) . . . 230
17.3.4.1 Unbuffered PWM Signal Generation . . . 230
17.3.4.2 Buffered PWM Signal Generation . . . 231
17.3.4.3 PWM Initialization . . . 231
17.4 Interrupts . . . 232
17.5 Wait Mode . . . 232
17.6 TIM1 During Break Interrupts . . . 233
17.7 Input/Output Signals . . . 233
17.8 Input/Output Registers . . . 233
17.8.1 TIM1 Status and Control Register . . . 233
17.8.2 TIM1 Counter Registers . . . 235
17.8.3 TIM1 Counter Modulo Registers . . . 236
17.8.4 TIM1 Channel Status and Control Registers . . . 236
17.8.5 TIM1 Channel Registers . . . 239

Chapter 18
Timer Interface Module (TIM2)

18.1 Introduction . . . 241
18.2 Features . . . 241
18.3 Functional Description . . . 241
18.3.1 TIM2 Counter Prescaler . . . 245
18.3.2 Input Capture . . . 246
18.3.3 Output Compare . . . 246
18.3.3.1 Unbuffered Output Compare . . . 246
18.3.3.2 Buffered Output Compare . . . 247
18.3.4 Pulse Width Modulation (PWM) . . . 248
18.3.4.1 Unbuffered PWM Signal Generation . . . 248
18.3.4.2 Buffered PWM Signal Generation . . . 249
18.3.4.3 PWM Initialization . . . 250
18.4 Interrupts . . . 251
18.5 Low-Power Modes . . . 251
18.5.1 Wait Mode . . . 251
18.5.2 Stop Mode . . . 251
18.6 TIM2 During Break Interrupts . . . 251

V_{REFL} is the low reference supply for the ADC, and by default the V_{SSAD}/V_{REFL} pin should be connected to the same voltage potential as V_{SS}. See Chapter 3 Analog-to-Digital Converter (ADC).

1.5.8 Port A Input/Output (I/O) Pins (PTA7/KBD7/AD15–PTA0/KBD0/AD8)

PTA7–PTA0 are general-purpose, bidirectional I/O port pins. Any or all of the port A pins can be programmed to serve as keyboard interrupt pins or used as analog-to-digital inputs. PTA7–PTA4 are only available on the 48-pin LQFP and 64-pin QFP packages. See Chapter 12 Input/Output (I/O) Ports, Chapter 9 Keyboard Interrupt Module (KBI), and Chapter 3 Analog-to-Digital Converter (ADC).

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.9 Port B I/O Pins (PTB7/AD7–PTB0/AD0)

PTB7–PTB0 are general-purpose, bidirectional I/O port pins that can also be used for analog-to-digital converter (ADC) inputs. PTB7–PTB6 are only available on the 48-pin LQFP and 64-pin QFP packages. See Chapter 12 Input/Output (I/O) Ports and Chapter 3 Analog-to-Digital Converter (ADC).

1.5.10 Port C I/O Pins (PTC6–PTC0)

PTC6 and PTC5 are general-purpose, bidirectional I/O port pins.

PTC4–PTC0 are general-purpose, bidirectional I/O port pins that contain higher current sink/source capability. PTC6–PTC2 are only available on the 48-pin LQFP and 64-pin QFP packages. See Chapter 12 Input/Output (I/O) Ports.

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.11 Port D I/O Pins (PTD7/T2CH1–PTD0/$\overline{SS}$)

PTD7–PTD0 are special-function, bidirectional I/O port pins. PTD3–PTD0 can be programmed to be serial peripheral interface (SPI) pins, while PTD7–PTD4 can be individually programmed to be timer interface module (TIM1 and TIM2) pins. PTD0 can be used to output a clock, MCLK. PTD7 is only available on the 48-pin LQFP and 64-pin QFP packages. See Chapter 17 Timer Interface Module (TIM1), Chapter 18 Timer Interface Module (TIM2), Chapter 15 Serial Peripheral Interface (SPI) Module, Chapter 12 Input/Output (I/O) Ports, and Chapter 5 Configuration Register (CONFIG).

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.12 Port E I/O Pins (PTE5–PTE2, PTE1/RxD, and PTE0/TxD)

PTE5–PTE0 are general-purpose, bidirectional I/O port pins. PTE1 and PTE0 can also be programmed to be enhanced serial communications interface (ESCI) pins. PTE5–PTE2 are only available on the 48-pin LQFP and 64-pin QFP packages. See Chapter 13 Enhanced Serial Communications Interface (ESCI) Module and Chapter 12 Input/Output (I/O) Ports.

1.5.13 Port F I/O Pins (PTF7/T2CH5–PTF0)

PTF7–PTF4 are special-function, bidirectional I/O port pins that can be individually programmed to be timer interface module (TIM2) pins.

2.6.2.2 FLASH-1 Block Protect Register

The FLASH-1 block protect register (FL1BPR) is implemented as a byte within the FLASH-1 memory; therefore, it can only be written during a FLASH programming sequence. The value in this register determines the starting location of the protected range within the FLASH-1 memory.

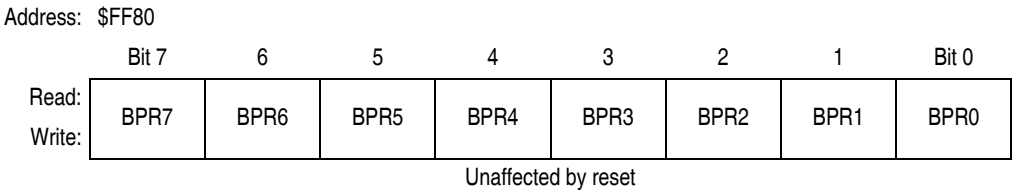


Figure 2-4. FLASH-1 Block Protect Register (FL1BPR)

FL1BPR[7:0] — Block Protect Register Bits 7 to 0

These eight bits represent bits [14:7] of a 16-bit memory address. Bit 15 is a 1 and bits [6:0] are 0s.

The resultant 16-bit address is used for specifying the start address of the FLASH-1 memory for block protection. FLASH-1 is protected from this start address to the end of FLASH-1 memory at $FFFF. With this mechanism, the protect start address can be $XX00 and $XX80 (128 byte page boundaries) within the FLASH-1 array.

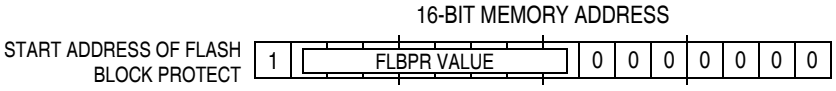


Figure 2-5. FLASH-1 Block Protect Start Address

Table 2-2. FLASH-1 Protected Ranges

FL1BPR[7:0]	Protected Range
$FF	No protection
$FE	$FF00–$FFFF
$FD ↓ $0B	$FE80–$FFFF ↓ $8580–$FFFF
$0A	$8500–$FFFF
$09	$8480–$FFFF
$08 ↓ $04	$8400–$FFFF ↓ $8200–$FFFF
$03	$8180–$FFFF
$02	$8100–$FFFF
$01	$8080–$FFFF
$00	$8000–$FFFF

2.7 FLASH-2 Memory (FLASH-2)

This subsection describes the operation of the embedded FLASH-2 memory. This memory can be read, programmed, and erased from a single external supply. The program and erase operations are enabled through the use of an internal charge pump.

2.7.1 Functional Description

The FLASH-2 memory is a non-continuous array consisting of a total of 29,822 bytes. An erased bit reads as a 1 and a programmed bit reads as a 0.

Memory in the FLASH-2 array is organized into rows within pages. There are two rows of memory per page with 64 bytes per row. The minimum erase block size is a single page,128 bytes. Programming is performed on a per-row basis, 64 bytes at a time. Program and erase operations are facilitated through control bits in the FLASH-2 control register (FL2CR). Details for these operations appear later in this subsection.

The FLASH-2 memory map consists of:

- $0462–$04FF: user memory (158 bytes)
- $0980–$1B7F: user memory (4608 bytes)
- $1E20–$7FFF: user memory (25056 bytes)
- $FF81: FLASH-2 block protect register (FL2BPR)

NOTE

FL2BPR physically resides within FLASH-1 memory addressing space

- $FE08: FLASH-2 control register (FL2CR)

Programming tools are available from Freescale Semiconductor. Contact your local representative for more information.

NOTE

A security feature prevents viewing of the FLASH contents.[1]

2.7.2 FLASH-2 Control and Block Protect Registers

The FLASH-2 array has two registers that control its operation, the FLASH-2 control register (FL2CR) and the FLASH-2 block protect register (FL2BPR).

2.7.2.1 FLASH-2 Control Register

The FLASH-2 control register (FL2CR) controls FLASH-2 program and erase operations.

Address: $FE08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 2-7. FLASH-2 Control Register (FL2CR)

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

In cases where desired bus frequency has some tolerance, choose f_{RCLK} to a value determined either by other module requirements (such as modules which are clocked by CGMXCLK), cost requirements, or ideally, as high as the specified range allows. See Chapter 20 Electrical Specifications. After choosing N, the actual bus frequency can be determined using equation in 2 above.

4. Select a VCO frequency multiplier, N.

$$N = \text{round}\left(\frac{f_{VCLKDES}}{f_{RCLK}}\right)$$

5. Calculate and verify the adequacy of the VCO and bus frequencies f_{VCLK} and f_{BUS}.

$$f_{VCLK} = (N) \times f_{RCLK}$$
$$f_{BUS} = (f_{VCLK})/4$$

6. Select the VCO's power-of-two range multiplier E, according to Table 4-2.

Table 4-2. Power-of-Two Range Selectors

Frequency Range	E
$0 < f_{VCLK} \leq 8$ MHz	0
8 MHz$< f_{VCLK} \leq 16$ MHz	1
16 MHz$< f_{VCLK} \leq 32$ MHz	$2^{(1)}$

1. Do not program E to a value of 3.

7. Select a VCO linear range multiplier, L, where f_{NOM} = 71.4 kHz

$$L = \text{Round}\left(\frac{f_{VCLK}}{2^E \times f_{NOM}}\right)$$

8. Calculate and verify the adequacy of the VCO programmed center-of-range frequency, f_{VRS}. The center-of-range frequency is the midpoint between the minimum and maximum frequencies attainable by the PLL.

$$f_{VRS} = (L \times 2^E)\, f_{NOM}$$

9. For proper operation,

$$|f_{VRS} - f_{VCLK}| \leq \frac{f_{NOM} \times 2^E}{2}$$

10. Verify the choice of N, E, and L by comparing f_{VCLK} to f_{VRS} and $f_{VCLKDES}$. For proper operation, f_{VCLK} must be within the application's tolerance of $f_{VCLKDES}$, and f_{VRS} must be as close as possible to f_{VCLK}.

NOTE

Exceeding the recommended maximum bus frequency or VCO frequency can crash the MCU.

4.5.4 PLL Multiplier Select Register Low

The PLL multiplier select register low (PMSL) contains the programming information for the low byte of the modulo feedback divider.

Address: $0038

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	MUL7	MUL6	MUL5	MUL4	MUL3	MUL2	MUL1	MUL0
Reset:	0	1	0	0	0	0	0	0

Figure 4-7. PLL Multiplier Select Register Low (PMSL)

NOTE

For applications using 1–8 MHz reference frequencies this register must be reprogrammed before enabling the PLL. The reset value of this register will cause applications using 1–8 MHz reference frequencies to become unstable if the PLL is enabled without programming an appropriate value. The programmed value must not allow the VCO clock to exceed 32 MHz. See 4.3.6 Programming the PLL for detailed instructions on choosing the proper value for PMSL.

MUL7–MUL0 — Multiplier Select Bits

These read/write bits control the low byte of the modulo feedback divider that selects the VCO frequency multiplier, N. (See 4.3.3 PLL Circuits and 4.3.6 Programming the PLL.) MUL7–MUL0 cannot be written when the PLLON bit in the PCTL is set. A value of $0000 in the multiplier select registers configures the modulo feedback divider the same as a value of $0001. Reset initializes the register to $40 for a default multiply value of 64.

NOTE

The multiplier select bits have built-in protection such that they cannot be written when the PLL is on (PLLON = 1).

4.5.5 PLL VCO Range Select Register

The PLL VCO range select register (PMRS) contains the programming information required for the hardware configuration of the VCO.

Address: $003A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	VRS7	VRS6	VRS5	VRS4	VRS3	VRS2	VRS1	VRS0
Reset:	0	1	0	0	0	0	0	0

Figure 4-8. PLL VCO Range Select Register (PMRS)

NOTE

Verify that the value of the PMRS register is appropriate for the given reference and VCO clock frequencies before enabling the PLL. See 4.3.6 Programming the PLL for detailed instructions on selecting the proper value for these control bits.

Table 7-1. Instruction Set Summary (Sheet 2 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
BHS *rel*	Branch if Higher or Same (Same as BCC)	PC ← (PC) + 2 + *rel* ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BIH *rel*	Branch if $\overline{\text{IRQ}}$ Pin High	PC ← (PC) + 2 + *rel* ? $\overline{\text{IRQ}}$ = 1	–	–	–	–	–	–	REL	2F	rr	3
BIL *rel*	Branch if $\overline{\text{IRQ}}$ Pin Low	PC ← (PC) + 2 + *rel* ? $\overline{\text{IRQ}}$ = 0	–	–	–	–	–	–	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X BIT *opr*,SP BIT *opr*,SP	Bit Test	(A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A5 B5 C5 D5 E5 F5 9EE5 9ED5	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
BLE *opr*	Branch if Less Than or Equal To (Signed Operands)	PC ← (PC) + 2 + *rel* ? (Z) ∣ (N ⊕ V) = 1	–	–	–	–	–	–	REL	93	rr	3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? (C) ∣ (Z) = 1	–	–	–	–	–	–	REL	23	rr	3
BLT *opr*	Branch if Less Than (Signed Operands)	PC ← (PC) + 2 + *rel* ? (N ⊕ V) =1	–	–	–	–	–	–	REL	91	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? (I) = 0	–	–	–	–	–	–	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? (N) = 1	–	–	–	–	–	–	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? (I) = 1	–	–	–	–	–	–	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? (Z) = 0	–	–	–	–	–	–	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? (N) = 0	–	–	–	–	–	–	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel*	–	–	–	–	–	–	REL	20	rr	3
BRCLR *n*,*opr*,*rel*	Branch if Bit *n* in M Clear	PC ← (PC) + 3 + *rel* ? (Mn) = 0	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2	–	–	–	–	–	–	REL	21	rr	3
BRSET *n*,*opr*,*rel*	Branch if Bit *n* in M Set	PC ← (PC) + 3 + *rel* ? (Mn) = 1	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n*,*opr*	Set Bit *n* in M	Mn ← 1	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	–	–	–	–	–	–	REL	AD	rr	4
CBEQ *opr*,*rel* CBEQA #*opr*,*rel* CBEQX #*opr*,*rel* CBEQ *opr*,X+,*rel* CBEQ X+,*rel* CBEQ *opr*,SP,*rel*	Compare and Branch if Equal	PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 3 + rel ? (X) – (M) = $00 PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 2 + rel ? (A) – (M) = $00 PC ← (PC) + 4 + rel ? (A) – (M) = $00	–	–	–	–	–	–	DIR IMM IMM IX1+ IX+ SP1	31 41 51 61 71 9E61	dd rr ii rr ii rr ff rr rr ff rr	5 4 4 5 4 6
CLC	Clear Carry Bit	C ← 0	–	–	–	–	–	0	INH	98		1
CLI	Clear Interrupt Mask	I ← 0	–	–	0	–	–	–	INH	9A		2

11.3.3 Voltage Hysteresis Protection

Once the LVI has triggered (by having V_{DD} fall below V_{TRIPF}), the LVI will maintain a reset condition until V_{DD} rises above the rising trip point voltage, V_{TRIPR}. This prevents a condition in which the MCU is continually entering and exiting reset if V_{DD} is approximately equal to V_{TRIPF}. V_{TRIPR} is greater than V_{TRIPF} by the hysteresis voltage, V_{HYS}.

11.3.4 LVI Trip Selection

The LVI5OR3 bit in the configuration register selects whether the LVI is configured for 5-V or 3-V protection.

NOTE

The microcontroller is guaranteed to operate at a minimum supply voltage. The trip point (V_{TRIPF} [5 V] or V_{TRIPF} [3 V]) may be lower than this. See Chapter 20 Electrical Specifications for the actual trip point voltages.

11.4 LVI Status Register

The LVI status register (LVISR) indicates if the V_{DD} voltage was detected below the V_{TRIPF} level.

Address: $FE0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LVIOUT	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-3. LVI Status Register (LVISR)

LVIOUT — LVI Output Bit

This read-only flag becomes set when the V_{DD} voltage falls below the V_{TRIPF} trip voltage (see Table 11-1). Reset clears the LVIOUT bit.

Table 11-1. LVIOUT Bit Indication

V_{DD}	LVIOUT
$V_{DD} > V_{TRIPR}$	0
$V_{DD} < V_{TRIPF}$	1
$V_{TRIPF} < V_{DD} < V_{TRIPR}$	Previous value

11.5 LVI Interrupts

The LVI module does not generate interrupt requests.

Table 12-1. Port Control Register Bits Summary (Continued)

Port	Bit	DDR	Module Control		Module Control		Pin
C	0	DDRC0			—	—	PTC0
	1	DDRC1					PTC1
	2	DDRC2					PTC2
	3	DDRC3					PTC3
	4	DDRC4					PTC4
	5	DDRC5					PTC5
	6	DDRC6					PTC6
D	0	DDRD0	SPI	SPE	—	—	PTD0/$\overline{SS}$/MCLK
	1	DDRD1					PTD1/MISO
	2	DDRD2					PTD2/MOSI
	3	DDRD3					PTD3/SPSCK
	4	DDRD4	TIM1	ELS0B:ELS0A			PTD4/T1CH0
	5	DDRD5		ELS1B:ELS1A			PTD5/T1CH1
	6	DDRD6	TIM2	ELS0B:ELS0A			PTD6/T2CH0
	7	DDRD7		ELS1B:ELS1A			PTD7/T2CH1
E	0	DDRE0	SCI	ENSCI	—	—	PTE0/TxD
	1	DDRE1					PTE1/RxD
	2	DDRE2					PTE2
	3	DDRE3					PTE3
	4	DDRE4					PTE4
	5	DDRE5					PTE5
F	0	DDRF0			—	—	PTF0
	1	DDRF1					PTF1
	2	DDRF2					PTF2
	3	DDRF3					PTF3
	4	DDRF4	TIM2	ELS2B:ELS2A			PTF4/T2CH2
	5	DDRF5		ELS3B:ELS3A			PTF5/T2CH3
	6	DDRF6		ELS4B:ELS4A			PTF6/T2CH4
	7	DDRF7		ELS5B:ELS5A			PTF7/T2CH5
G	0	DDRG0	ADC	ADCH[23:16]	—	—	PTG0/AD16
	1	DDRG1					PTG1/AD17
	2	DDRG2					PTG2/AD18
	3	DDRG3					PTG3/AD19
	4	DDRG4					PTG4/AD20
	5	DDRG5					PTG5/AD21
	6	DDRG6					PTG6/AD22
	7	DDRG7					PTG7/AD23

RE — Receiver Enable Bit

Setting this read/write bit enables the receiver. Clearing the RE bit disables the receiver but does not affect receiver interrupt flag bits. Reset clears the RE bit.

1 = Receiver enabled
0 = Receiver disabled

NOTE

Writing to the RE bit is not allowed when the enable ESCI bit (ENSCI) is clear. ENSCI is in ESCI control register 1.

RWU — Receiver Wakeup Bit

This read/write bit puts the receiver in a standby state during which receiver interrupts are disabled. The WAKE bit in SCC1 determines whether an idle input or an address mark brings the receiver out of the standby state and clears the RWU bit. Reset clears the RWU bit.

1 = Standby state
0 = Normal operation

SBK — Send Break Bit

Setting and then clearing this read/write bit transmits a break character followed by a 1. The 1 after the break character guarantees recognition of a valid start bit. If SBK remains set, the transmitter continuously transmits break characters with no 1s between them. Reset clears the SBK bit.

1 = Transmit break characters
0 = No break characters being transmitted

NOTE

Do not toggle the SBK bit immediately after setting the SCTE bit. Toggling SBK before the preamble begins causes the ESCI to send a break character instead of a preamble.

13.8.3 ESCI Control Register 3

ESCI control register 3 (SCC3):

- Stores the ninth ESCI data bit received and the ninth ESCI data bit to be transmitted.
- Enables these interrupts:
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error

Address: $0015

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R8	T8	R	R	ORIE	NEIE	FEIE	PEIE
Write:								
Reset:	U	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 13-12. ESCI Control Register 3 (SCC3)

R8 — Received Bit 8

When the ESCI is receiving 9-bit characters, R8 is the read-only ninth bit (bit 8) of the received character. R8 is received at the same time that the SCDR receives the other 8 bits.

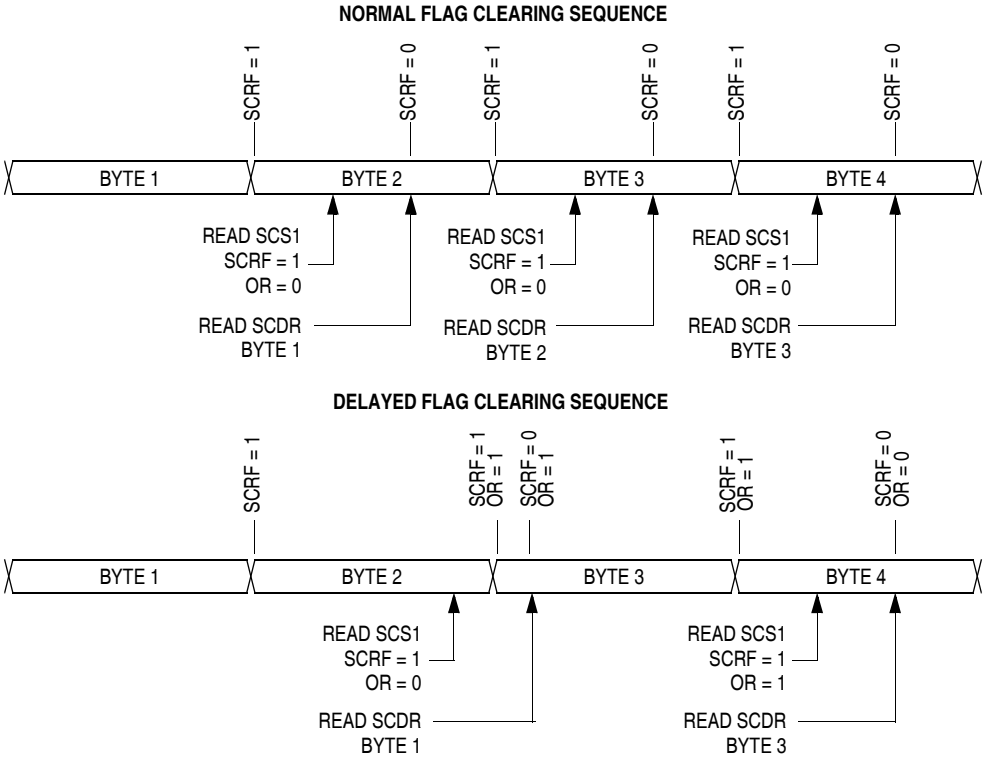


Figure 13-14. Flag Clearing Sequence

In applications that are subject to software latency or in which it is important to know which byte is lost due to an overrun, the flag-clearing routine can check the OR bit in a second read of SCS1 after reading the data register.

NF — Receiver Noise Flag Bit

This clearable, read-only bit is set when the ESCI detects noise on the RxD pin. NF generates an NF CPU interrupt request if the NEIE bit in SCC3 is also set. Clear the NF bit by reading SCS1 and then reading the SCDR. Reset clears the NF bit.

1 = Noise detected
0 = No noise detected

FE — Receiver Framing Error Bit

This clearable, read-only bit is set when a 0 is accepted as the stop bit. FE generates an ESCI error CPU interrupt request if the FEIE bit in SCC3 also is set. Clear the FE bit by reading SCS1 with FE set and then reading the SCDR. Reset clears the FE bit.

1 = Framing error detected
0 = No framing error detected

PE — Receiver Parity Error Bit

This clearable, read-only bit is set when the ESCI detects a parity error in incoming data. PE generates a PE CPU interrupt request if the PEIE bit in SCC3 is also set. Clear the PE bit by reading SCS1 with PE set and then reading the SCDR. Reset clears the PE bit.

1 = Parity error detected
0 = No parity error detected

13.9.1 ESCI Arbiter Control Register

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	AM1	ALOST	AM0	ACLK	AFIN	ARUN	AROVFL	ARD8
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-19. ESCI Arbiter Control Register (SCIACTL)

AM1 and AM0 — Arbiter Mode Select Bits

These read/write bits select the mode of the arbiter module as shown in Table 13-12. Reset clears AM1 and AM0.

Table 13-12. ESCI Arbiter Selectable Modes

AM[1:0]	ESCI Arbiter Mode
0 0	Idle / counter reset
0 1	Bit time measurement
1 0	Bus arbitration
1 1	Reserved / do not use

ALOST — Arbitration Lost Flag

This read-only bit indicates loss of arbitration. Clear ALOST by writing a 0 to AM1. Reset clears ALOST.

ACLK — Arbiter Counter Clock Select Bit

This read/write bit selects the arbiter counter clock source. Reset clears ACLK.

1 = Arbiter counter is clocked with one half of the ESCI input clock generated by the ESCI prescaler
0 = Arbiter counter is clocked with the bus clock divided by four

NOTE

For ACLK = 1, the arbiter input clock is driven from the ESCI prescaler. The prescaler can be clocked by either the bus clock or CGMXCLK depending on the state of the SCIBDSRC bit in CONFIG2.

AFIN— Arbiter Bit Time Measurement Finish Flag

This read-only bit indicates bit time measurement has finished. Clear AFIN by writing any value to SCIACTL. Reset clears AFIN.

1 = Bit time measurement has finished
0 = Bit time measurement not yet finished

ARUN— Arbiter Counter Running Flag

This read-only bit indicates the arbiter counter is running. Reset clears ARUN.

1 = Arbiter counter running
0 = Arbiter counter stopped

If SCI_TxD senses 0 without having sensed a 0 before on RxD, the counter will be reset, arbitration operation will be restarted after the next rising edge of SCI_TxD.

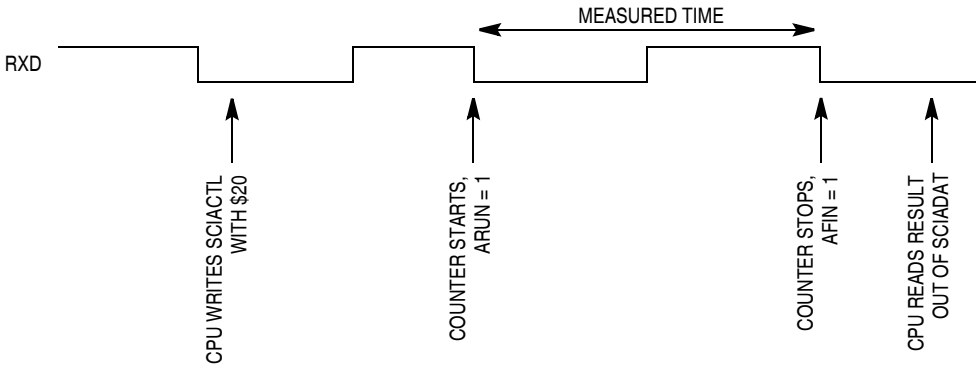


Figure 13-21. Bit Time Measurement with ACLK = 0

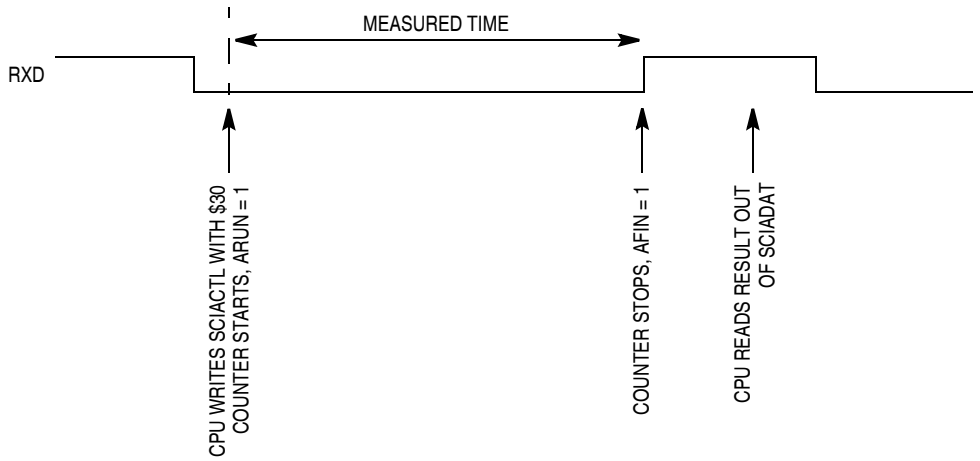


Figure 13-22. Bit Time Measurement with ACLK = 1, Scenario A

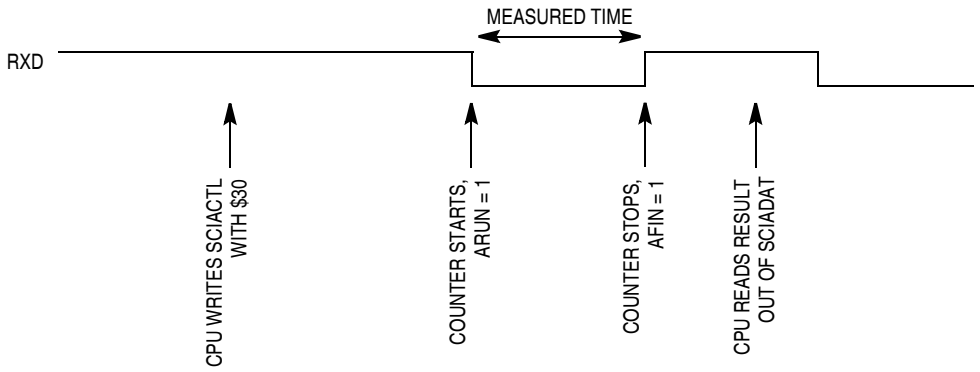


Figure 13-23. Bit Time Measurement with ACLK = 1, Scenario B

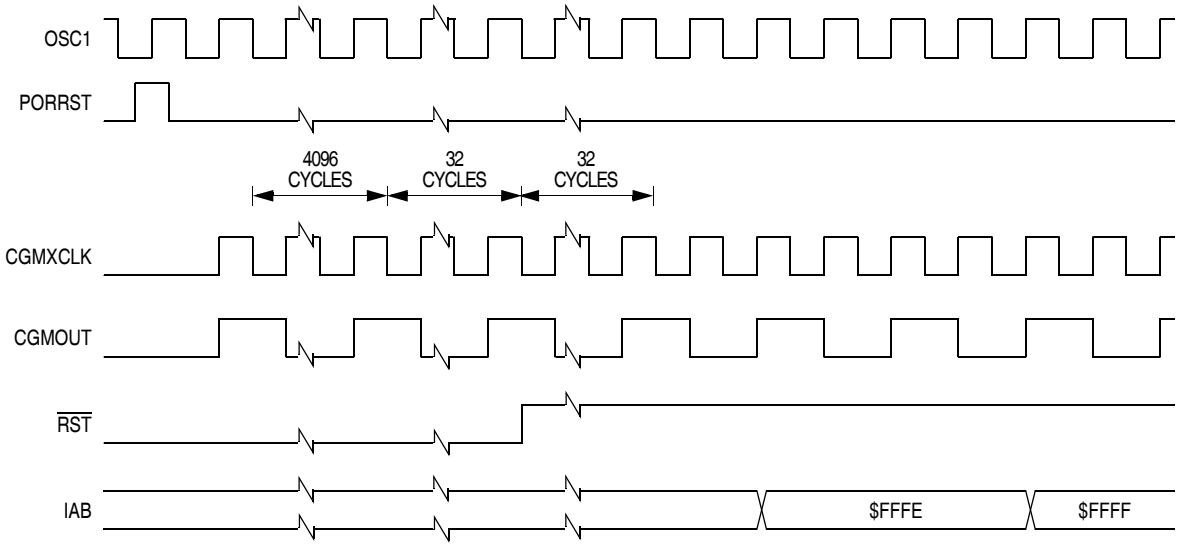


Figure 14-7. POR Recovery

14.3.2.3 Illegal Opcode Reset

The SIM decodes signals from the CPU to detect illegal instructions. An illegal instruction sets the ILOP bit in the SIM reset status register (SRSR) and causes a reset.

If the stop enable bit, STOP, in the CONFIG1 register is 0, the SIM treats the STOP instruction as an illegal opcode and causes an illegal opcode reset. The SIM actively pulls down the $\overline{\text{RST}}$ pin for all internal reset sources.

14.3.2.4 Illegal Address Reset

An opcode fetch from an unmapped address generates an illegal address reset. The SIM verifies that the CPU is fetching an opcode prior to asserting the ILAD bit in the SIM reset status register (SRSR) and resetting the MCU. A data fetch from an unmapped address does not generate a reset. The SIM actively pulls down the $\overline{\text{RST}}$ pin for all internal reset sources.

14.3.2.5 Low-Voltage Inhibit (LVI) Reset

The low-voltage inhibit module (LVI) asserts its output to the SIM when the V_{DD} voltage falls to the V_{TRIPF} voltage. The LVI bit in the SIM reset status register (SRSR) is set, and the external reset pin ($\overline{\text{RST}}$) is asserted if the LVIPWRD and LVIRSTD bits in the CONFIG1 register are 0. The $\overline{\text{RST}}$ pin will be held low while the SIM counter counts out 4096 + 32 CGMXCLK cycles after V_{DD} rises above V_{TRIPR}. Thirty-two CGMXCLK cycles later, the CPU is released from reset to allow the reset vector sequence to occur. The SIM actively pulls down the $\overline{\text{RST}}$ pin for all internal reset sources.

14.3.2.6 Monitor Mode Entry Module Reset (MODRST)

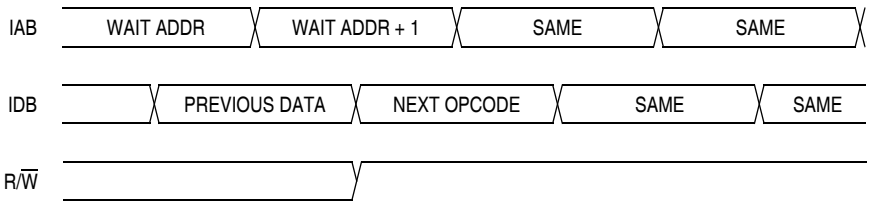
The monitor mode entry module reset (MODRST) asserts its output to the SIM when monitor mode is entered in the condition where the reset vectors are erased ($FF) (see 19.3.1.1 Normal Monitor Mode). When MODRST gets asserted, an internal reset occurs. The SIM actively pulls down the $\overline{\text{RST}}$ pin for all internal reset sources.

14.6.1 Wait Mode

In wait mode, the CPU clocks are inactive while the peripheral clocks continue to run. Figure 14-16 shows the timing for wait mode entry.

A module that is active during wait mode can wakeup the CPU with an interrupt if the interrupt is enabled. Stacking for the interrupt begins one cycle after the WAIT instruction during which the interrupt occurred. In wait mode, the CPU clocks are inactive. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

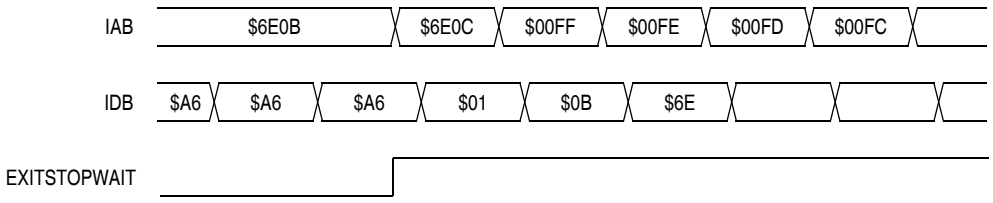
Wait mode also can be exited by a reset or break. A break interrupt during wait mode sets the SIM break stop/wait bit, SBSW, in the SIM break status register (BSR). If the COP disable bit, COPD, in the CONFIG1 register is 0, then the computer operating properly module (COP) is enabled and remains active in wait mode.



Note: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

Figure 14-16. Wait Mode Entry Timing

Figure 14-17 and Figure 14-18 show the timing for WAIT recovery.



Note: EXITSTOPWAIT = $\overline{\text{RST}}$ pin, CPU interrupt, or break interrupt

Figure 14-17. Wait Recovery from Interrupt or Break

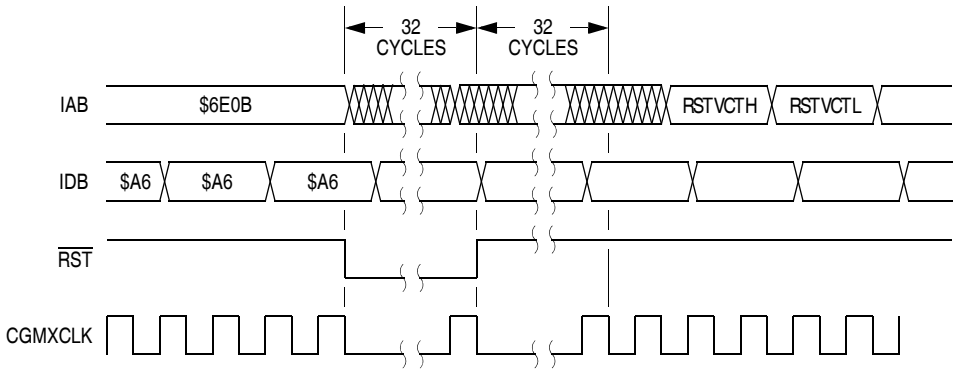


Figure 14-18. Wait Recovery from Internal Reset

19.2.2.3 Break Status Register

The break status register (BSR) contains a flag to indicate that a break caused an exit from wait mode. This register is only used in emulation mode.

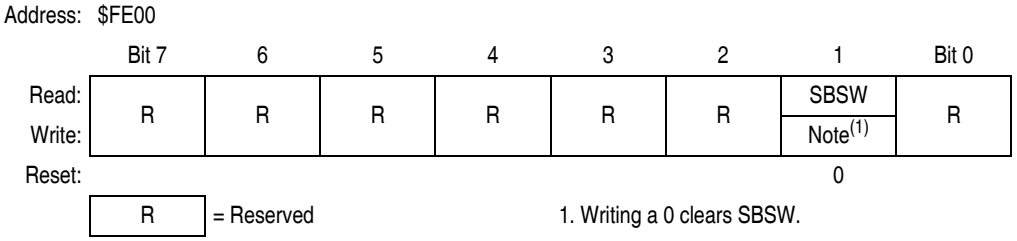


Figure 19-7. Break Status Register (BSR)

SBSW — SIM Break Stop/Wait

SBSW can be read within the break state SWI routine. The user can modify the return address on the stack by subtracting one from it.

1 = Wait mode was exited by break interrupt
0 = Wait mode was not exited by break interrupt

19.2.2.4 Break Flag Control Register

The break control register (BFCR) contains a bit that enables software to clear status bits while the MCU is in a break state.

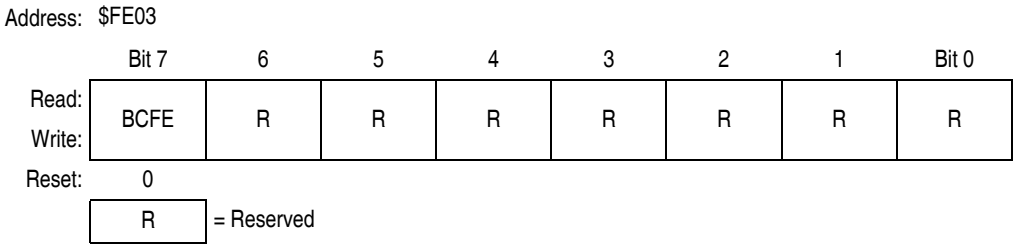


Figure 19-8. Break Flag Control Register (BFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break
0 = Status bits not clearable during break

19.2.3 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power- consumption standby modes. If enabled, the break module will remain enabled in wait and stop modes. However, since the internal address bus does not increment in these modes, a break interrupt will never be triggered.

20.7 5.0-Volt Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of operation Crystal option External clock option[2]	f_{OSC}	 1 dc	 8 32	MHz
Internal operating frequency	f_{OP} (f_{Bus})	—	8	MHz
Internal clock period ($1/f_{OP}$)	t_{CYC}	125	—	ns
RESET input pulse width low	t_{RL}	100	—	ns
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	100	—	ns
$\overline{IRQ}$ interrupt pulse period[3]	t_{ILIL}	Note 3	—	t_{CYC}

1. V_{SS} = 0 Vdc; timing shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.
2. No more than 10% duty cycle deviation from 50%.
3. The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1 t_{CYC}.

20.8 3.3-Volt Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of operation Crystal option External clock option[2]	f_{OSC}	 1 dc	 8 16	MHz
Internal operating frequency	f_{OP} (f_{Bus})	—	4	MHz
Internal clock period ($1/f_{OP}$)	t_{CYC}	250	—	ns
RESET input pulse width low	t_{RL}	200	—	ns
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	200	—	ns
$\overline{IRQ}$ interrupt pulse period[3]	t_{ILIL}	Note 3	—	t_{CYC}

1. V_{SS} = 0 Vdc; timing shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.
2. No more than 10% duty cycle deviation from 50%.
3. The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1 t_{CYC}.

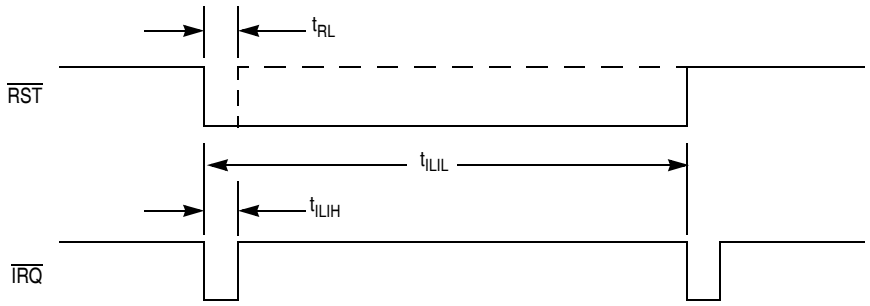
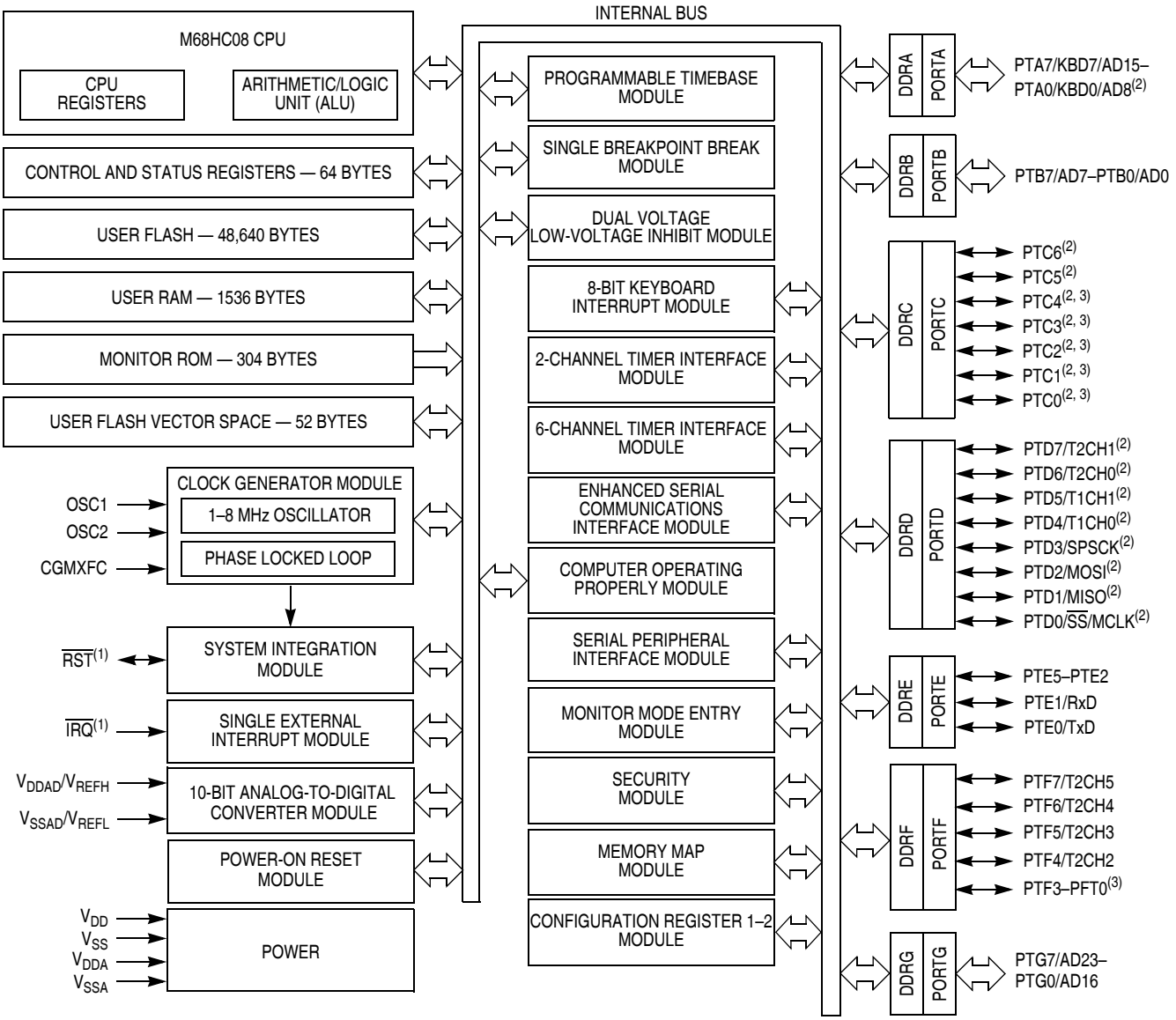


Figure 20-1. $\overline{RST}$ and $\overline{IRQ}$ Timing



1. Pin contains integrated pullup device.
2. Ports are software configurable with pullup device if input port or pullup/pulldown device for keyboard input.
3. Higher current drive port pins

Figure A-1. MC68HC908GR48A Block Diagram