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Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908gr32amfje

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V_{REFL} is the low reference supply for the ADC, and by default the V_{SSAD}/V_{REFL} pin should be connected to the same voltage potential as V_{SS} . See Chapter 3 Analog-to-Digital Converter (ADC).

1.5.8 Port A Input/Output (I/O) Pins (PTA7/KBD7/AD15–PTA0/KBD0/AD8)

PTA7–PTA0 are general-purpose, bidirectional I/O port pins. Any or all of the port A pins can be programmed to serve as keyboard interrupt pins or used as analog-to-digital inputs. PTA7–PTA4 are only available on the 48-pin LQFP and 64-pin QFP packages. See Chapter 12 Input/Output (I/O) Ports, Chapter 9 Keyboard Interrupt Module (KBI), and Chapter 3 Analog-to-Digital Converter (ADC).

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.9 Port B I/O Pins (PTB7/AD7–PTB0/AD0)

PTB7–PTB0 are general-purpose, bidirectional I/O port pins that can also be used for analog-to-digital converter (ADC) inputs. PTB7–PTB6 are only available on the 48-pin LQFP and 64-pin QFP packages. See Chapter 12 Input/Output (I/O) Ports and Chapter 3 Analog-to-Digital Converter (ADC).

1.5.10 Port C I/O Pins (PTC6–PTC0)

PTC6 and PTC5 are general-purpose, bidirectional I/O port pins.

PTC4–PTC0 are general-purpose, bidirectional I/O port pins that contain higher current sink/source capability. PTC6–PTC2 are only available on the 48-pin LQFP and 64-pin QFP packages. See Chapter 12 Input/Output (I/O) Ports.

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.11 Port D I/O Pins (PTD7/T2CH1–PTD0/SS)

PTD7–PTD0 are special-function, bidirectional I/O port pins. PTD3–PTD0 can be programmed to be serial peripheral interface (SPI) pins, while PTD7–PTD4 can be individually programmed to be timer interface module (TIM1 and TIM2) pins. PTD0 can be used to output a clock, MCLK. PTD7 is only available on the 48-pin LQFP and 64-pin QFP packages. See Chapter 17 Timer Interface Module (TIM1), Chapter 18 Timer Interface Module (TIM2), Chapter 15 Serial Peripheral Interface (SPI) Module, Chapter 12 Input/Output (I/O) Ports, and Chapter 5 Configuration Register (CONFIG).

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.12 Port E I/O Pins (PTE5–PTE2, PTE1/RxD, and PTE0/TxD)

PTE5–PTE0 are general-purpose, bidirectional I/O port pins. PTE1 and PTE0 can also be programmed to be enhanced serial communications interface (ESCI) pins. PTE5–PTE2 are only available on the 48-pin LQFP and 64-pin QFP packages. See Chapter 13 Enhanced Serial Communications Interface (ESCI) Module and Chapter 12 Input/Output (I/O) Ports.

1.5.13 Port F I/O Pins (PTF7/T2CH5–PTF0)

PTF7–PTF4 are special-function, bidirectional I/O port pins that can be individually programmed to be timer interface module (TIM2) pins.

Memory

\$0000 ↓ \$003F	I/O REGISTERS 64 BYTES	\$FE00	SIM BREAK STATUS REGISTER (BSR)
\$0040 ↓ \$043F	RAM-1 1024 BYTES	\$FE01	SIM RESET STATUS REGISTER (SRSR)
\$0440 ↓ \$0461	I/O REGISTERS 34 BYTES	\$FE02	RESERVED
\$0462 ↓ \$04FF	FLASH-2 158 BYTES	\$FE03	SIM BREAK FLAG CONTROL REGISTER (BFCR)
\$0500 ↓ \$057F	RESERVED 128 BYTES	\$FE04	INTERRUPT STATUS REGISTER 1 (INT1)
\$0580 ↓ \$097F	RAM-2 1024 BYTES	\$FE05	INTERRUPT STATUS REGISTER 2 (INT2)
\$0980 ↓ \$1B7F	FLASH-2 4608 BYTES	\$FE06	INTERRUPT STATUS REGISTER 3 (INT3)
\$1B80 ↓ \$1DFF	RESERVED 640 BYTES	\$FE07	INTERRUPT STATUS REGISTER 4 (INT4)
\$1E00 ↓ \$1E0F	MONITOR ROM 16 BYTES	\$FE08	FLASH-2 CONTROL REGISTER (FL2CR)
\$1E10 ↓ \$1E1F	RESERVED 16 BYTES	\$FE09	BREAK ADDRESS REGISTER HIGH (BRKH)
\$1E20 ↓ \$7FFF	FLASH-2 25,056 BYTES	\$FE0A	BREAK ADDRESS REGISTER LOW (BRKL)
\$8000 ↓ \$FDFF	FLASH-1 32,256 BYTES	\$FE0B	BREAK STATUS AND CONTROL REGISTER (BRKSCR)
		\$FE0C	LVI STATUS REGISTER (LVISR)
		\$FE0D	FLASH-2 TEST CONTROL REGISTER (FLT2CR)
		\$FE0E	FLASH-1 TEST CONTROL REGISTER (FLT1CR)
		\$FE0F	UNIMPLEMENTED
		\$FE10 ↓ \$FE1F	UNIMPLEMENTED 16 BYTES RESERVED FOR COMPATIBILITY WITH MONITOR CODE FOR A-FAMILY PART
		\$FE20 ↓ \$FF7F	MONITOR ROM 352 BYTES
		\$FF80	FLASH-1 BLOCK PROTECT REGISTER (FL1BPR)
		\$FF81	FLASH-2 BLOCK PROTECT REGISTER (FL2BPR)
		\$FF82 ↓ \$FF87	RESERVED 6 BYTES
		\$FF88	FLASH-1 CONTROL REGISTER (FL1CR)
		\$FF89 ↓ \$FFCB	RESERVED 67 BYTES
		\$FFCC ↓ \$FFFF ⁽¹⁾	FLASH-1 VECTORS 52 BYTES

1. \$FFF6–\$FFFD used for eight security bytes

Figure 2-1. MC68HC908GR60A Memory Map

3.7.4 ADC Voltage Reference Low Pin (V_{REFL})

The ADC analog portion uses V_{REFL} as its lower voltage reference pin. By default, connect the V_{REFL} pin to the same voltage potential as V_{SS} . External filtering is often necessary to ensure a clean V_{REFL} for good results. Any noise present on this pin will be reflected and possibly magnified in A/D conversion values.

NOTE

For maximum noise immunity, route V_{REFL} carefully and, if not connected to V_{SS} , place bypass capacitors as close as possible to the package. Routing V_{REFH} close and parallel to V_{REFL} may improve common mode noise rejection.

V_{SSAD} and V_{REFL} are bonded internally.

3.7.5 ADC Voltage In (V_{ADIN})

V_{ADIN} is the input voltage signal from one of the 24 ADC channels to the ADC module.

3.8 I/O Registers

These I/O registers control and monitor ADC operation:

- ADC status and control register (ADSCR)
- ADC data register (ADRH and ADRL)
- ADC clock register (ADCLK)

3.8.1 ADC Status and Control Register

Function of the ADC status and control register (ADSCR) is described here.

Address:	\$003C							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Write:	R							
Reset:	0	0	0	1	1	1	1	1
	R = Reserved							

Figure 3-4. ADC Status and Control Register (ADSCR)

COCO — Conversions Complete Bit

In non-interrupt mode ($AIEN = 0$), COCO is a read-only bit that is set at the end of each conversion. COCO will stay set until cleared by a read of the ADC data register. Reset clears this bit.

In interrupt mode ($AIEN = 1$), COCO is a read-only bit that is not set at the end of a conversion. It always reads as a 0.

1 = Conversion completed ($AIEN = 0$)

0 = Conversion not completed ($AIEN = 0$) or CPU interrupt enabled ($AIEN = 1$)

NOTE

The write function of the COCO bit is reserved. When writing to the ADSCR register, always have a 0 in the COCO bit position.

The most critical parameter which affects the reaction times of the PLL is the reference frequency, f_{RCLK} . This frequency is the input to the phase detector and controls how often the PLL makes corrections. For stability, the corrections must be small compared to the desired frequency, so several corrections are required to reduce the frequency error. Therefore, the slower the reference the longer it takes to make these corrections. This parameter is under user control via the choice of crystal frequency f_{XCLK} . (See 4.3.3 PLL Circuits and 4.3.6 Programming the PLL.)

Another critical parameter is the external filter network. The PLL modifies the voltage on the VCO by adding or subtracting charge from capacitors in this network. Therefore, the rate at which the voltage changes for a given frequency error (thus change in charge) is proportional to the capacitance. The size of the capacitor also is related to the stability of the PLL. If the capacitor is too small, the PLL cannot make small enough adjustments to the voltage and the system cannot lock. If the capacitor is too large, the PLL may not be able to adjust the voltage in a reasonable time. (See 4.8.3 Choosing a Filter.)

Also important is the operating voltage potential applied to V_{DDA} . The power supply potential alters the characteristics of the PLL. A fixed value is best. Variable supplies, such as batteries, are acceptable if they vary within a known range at very slow speeds. Noise on the power supply is not acceptable, because it causes small frequency errors which continually change the acquisition time of the PLL.

Temperature and processing also can affect acquisition time because the electrical characteristics of the PLL change. The part operates as specified as long as these influences stay within the specified limits. External factors, however, can cause drastic changes in the operation of the PLL. These factors include noise injected into the PLL through the filter capacitor, filter capacitor leakage, stray impedances on the circuit board, and even humidity or circuit board contamination.

4.8.3 Choosing a Filter

As described in 4.8.2 Parametric Influences on Reaction Time, the external filter network is critical to the stability and reaction time of the PLL. The PLL is also dependent on reference frequency and supply voltage.

Figure 4-9 shows two types of filter circuits. In low-cost applications, where stability and reaction time of the PLL are not critical, the three component filter network shown in Figure 4-9 (B) can be replaced by a single capacitor, C_F , as shown in Figure 4-9 (A). Refer to Table 4-5 for recommended filter components at various reference frequencies. For reference frequencies between the values listed in the table, extrapolate to the nearest common capacitor value. In general, a slightly larger capacitor provides more stability at the expense of increased lock time.

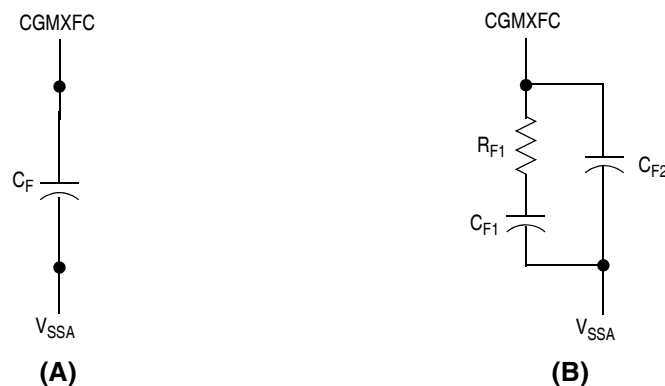


Figure 4-9. PLL Filter

Computer Operating Properly (COP) Module

The COP counter is a free-running 6-bit counter preceded by the 12-bit SIM counter. If not cleared by software, the COP counter overflows and generates an asynchronous reset after 262,128 or 8176 CGMXCLK cycles, depending on the state of the COP rate select bit, COPRS, in the configuration register. With a 262,128 CGMXCLK cycle overflow option, a 4.9152-MHz crystal gives a COP timeout period of 53.3 ms. Writing any value to location \$FFFF before an overflow occurs prevents a COP reset by clearing the COP counter and stages 12–5 of the SIM counter.

NOTE

Service the COP immediately after reset and before entering or after exiting stop mode to guarantee the maximum time before the first COP counter overflow.

A COP reset pulls the $\overline{\text{RST}}$ pin low for 32 CGMXCLK cycles and sets the COP bit in the reset status register (RSR).

In monitor mode, the COP is disabled if the $\overline{\text{RST}}$ pin or the $\overline{\text{IRQ}}$ is held at V_{TST} . During the break state, V_{TST} on the $\overline{\text{RST}}$ pin disables the COP.

NOTE

Place COP clearing instructions in the main program and not in an interrupt subroutine. Such an interrupt subroutine could keep the COP from generating a reset even while the main program is not working properly.

6.3 I/O Signals

The following paragraphs describe the signals shown in Figure 6-1.

6.3.1 CGMXCLK

CGMXCLK is the crystal oscillator output signal. CGMXCLK frequency is equal to the crystal frequency.

6.3.2 STOP Instruction

The STOP instruction clears the SIM counter.

6.3.3 COPCTL Write

Writing any value to the COP control register (COPCTL) clears the COP counter and clears stages 12–5 of the SIM counter. Reading the COP control register returns the low byte of the reset vector. See 6.4 COP Control Register.

6.3.4 Power-On Reset

The power-on reset (POR) circuit clears the SIM counter 4096 CGMXCLK cycles after power-up.

6.3.5 Internal Reset

An internal reset clears the SIM counter and the COP counter.

Chapter 8

External Interrupt (IRQ)

8.1 Introduction

The IRQ (external interrupt) module provides a maskable interrupt input.

8.2 Features

- Features of the IRQ module include:
- A dedicated external interrupt pin ($\overline{\text{IRQ}}$)
- IRQ interrupt control bits
- Hysteresis buffer
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Internal pullup resistor

8.3 Functional Description

A low applied to the external interrupt pin can latch a central processor unit (CPU) interrupt request. Figure 8-1 shows the structure of the IRQ module.

Interrupt signals on the $\overline{\text{IRQ}}$ pin are latched into the IRQ latch. An interrupt latch remains set until one of the following actions occurs:

- Vector fetch — A vector fetch automatically generates an interrupt acknowledge signal that clears the latch that caused the vector fetch.
- Software clear — Software can clear an interrupt latch by writing to the appropriate acknowledge bit in the interrupt status and control register (INTSCR). Writing a 1 to the ACK bit clears the IRQ latch.
- Reset — A reset automatically clears the interrupt latch.

The external interrupt pin is falling-edge triggered out of reset and is software-configurable to be either falling-edge or falling-edge and low-level triggered. The MODE bit in the INTSCR controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin.

When an interrupt pin is edge-triggered only (MODE = 0), the interrupt remains set until a vector fetch, software clear, or reset occurs.

When an interrupt pin is both falling-edge and low-level triggered (MODE = 1), the interrupt remains set until both of these events occur:

- Vector fetch or software clear
- Return of the interrupt pin to a high level

9.7.2 Keyboard Interrupt Enable Register

The keyboard interrupt enable register enables or disables each port A pin to operate as a keyboard interrupt pin.

Address: \$001B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	KBIE7	KBIE6	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
Write:	KBIE7	KBIE6	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
Reset:	0	0	0	0	0	0	0	0

Figure 9-5. Keyboard Interrupt Enable Register (INTKBIER)

KBIE7–KBIE0 — Keyboard Interrupt Enable Bits

Each of these read/write bits enables the corresponding keyboard interrupt pin to latch interrupt requests. Reset clears the keyboard interrupt enable register.

1 = PTAx pin enabled as keyboard interrupt pin

0 = PTAx pin not enabled as keyboard interrupt pin

9.7.3 Keyboard Interrupt Polarity Register

The KBIP7–KBIP0 bits determine the polarity of the keyboard pin detection. These bits along with the MODEK bit determine whether a logic level (0 or 1) and/or a falling (or rising) edge is being detected. The KBIPx bits also select the pullup resistor (KBIPx = 0) or pulldown resistor (KBIPx = 1) for each enabled keyboard interrupt pin.

Address: \$0448

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	KBIP7	KBIP6	KBIP5	KBIP4	KBIP3	KBIP2	KBIP1	KBIP0
Write:	KBIP7	KBIP6	KBIP5	KBIP4	KBIP3	KBIP2	KBIP1	KBIP0
Reset:	0	0	0	0	0	0	0	0

Figure 9-6. Keyboard Interrupt Polarity Register (INTKBIPR)

KBIP7–KBIP0 — Keyboard Interrupt Polarity Bits

Each of these read/write bits enables the polarity of the keyboard interrupt pin. Reset clears the keyboard interrupt polarity register.

1 = Keyboard polarity is rising edge and/or high level

0 = Keyboard polarity is falling edge and/or low level

10.7 External Interrupt Module (IRQ)

10.7.1 Wait Mode

The external interrupt (IRQ) module remains active in wait mode. Clearing the IMASK bit in the IRQ status and control register enables $\overline{\text{IRQ}}$ CPU interrupt requests to bring the MCU out of wait mode.

10.7.2 Stop Mode

The IRQ module remains active in stop mode. Clearing the IMASK bit in the IRQ status and control register enables $\overline{\text{IRQ}}$ CPU interrupt requests to bring the MCU out of stop mode.

10.8 Keyboard Interrupt Module (KBI)

10.8.1 Wait Mode

The keyboard interrupt (KBI) module remains active in wait mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

10.8.2 Stop Mode

The keyboard module remains active in stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

10.9 Low-Voltage Inhibit Module (LVI)

10.9.1 Wait Mode

If enabled, the low-voltage inhibit (LVI) module remains active in wait mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of wait mode.

10.9.2 Stop Mode

If enabled, the LVI module remains active in stop mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of stop mode.

10.10 Enhanced Serial Communications Interface Module (ESCI)

10.10.1 Wait Mode

The enhanced serial communications interface (ESCI), or SCI module for short, module remains active in wait mode. Any enabled CPU interrupt request from the SCI module can bring the MCU out of wait mode.

If SCI module functions are not required during wait mode, reduce power consumption by disabling the module before executing the WAIT instruction.

10.10.2 Stop Mode

The SCI module is inactive in stop mode. The STOP instruction does not affect SCI register states. SCI module operation resumes after the MCU exits stop mode.

Because the internal clock is inactive during stop mode, entering stop mode during an SCI transmission or reception results in invalid data.

10.14 Exiting Wait Mode

These events restart the CPU clock and load the program counter with the reset vector or with an interrupt vector:

- External reset — A low on the $\overline{\text{RST}}$ pin resets the MCU and loads the program counter with the contents of locations \$FFFE and \$FFFF.
- External interrupt — A high-to-low transition on an external interrupt pin ($\overline{\text{IRQ}}$ pin) loads the program counter with the contents of locations: \$FFFA and \$FFFB; $\overline{\text{IRQ}}$ pin.
- Break interrupt — In emulation mode, a break interrupt loads the program counter with the contents of \$FFFC and \$FFFD.
- Computer operating properly (COP) module reset — A timeout of the COP counter resets the MCU and loads the program counter with the contents of \$FFFE and \$FFFF.
- Low-voltage inhibit (LVI) module reset — A power supply voltage below the V_{TRIPF} voltage resets the MCU and loads the program counter with the contents of locations \$FFFE and \$FFFF.
- Clock generator module (CGM) interrupt — A CPU interrupt request from the CGM loads the program counter with the contents of \$FFF8 and \$FFF9.
- Keyboard interrupt (KBI) module — A CPU interrupt request from the KBI module loads the program counter with the contents of \$FFE0 and \$FFE1.
- Timer 1 interface (TIM1) module interrupt — A CPU interrupt request from the TIM1 loads the program counter with the contents of:
 - \$FFF2 and \$FFF3; TIM1 overflow
 - \$FFF4 and \$FFF5; TIM1 channel 1
 - \$FFF6 and \$FFF7; TIM1 channel 0
- Timer 2 interface module (TIM2) interrupt — A CPU interrupt request from the TIM2 loads the program counter with the contents of:
 - \$FFEC and \$FFED; TIM2 overflow
 - \$FFEE and \$FFEF; TIM2 channel 1
 - \$FFF0 and \$FFF1; TIM2 channel 0
 - \$FFCC and \$FFCD; TIM2 channel 5
 - \$FFCE and \$FFCF; TIM2 channel 4
 - \$FFD0 and \$FFD1; TIM2 channel 3
 - \$FFD2 and \$FFD3; TIM2 channel 2
- Serial peripheral interface (SPI) module interrupt — A CPU interrupt request from the SPI loads the program counter with the contents of:
 - \$FFE8 and \$FFE9; SPI transmitter
 - \$FFEA and \$FFEB; SPI receiver
- Serial communications interface (SCI) module interrupt — A CPU interrupt request from the SCI loads the program counter with the contents of:
 - \$FFE2 and \$FFE3; SCI transmitter
 - \$FFE4 and \$FFE5; SCI receiver
 - \$FFE6 and \$FFE7; SCI receiver error
- Analog-to-digital converter (ADC) module interrupt — A CPU interrupt request from the ADC loads the program counter with the contents of: \$FFDE and \$FFDF; ADC conversion complete.
- Timebase module (TBM) interrupt — A CPU interrupt request from the TBM loads the program counter with the contents of: \$FFDC and \$FFDD; TBM interrupt.

10.15 Exiting Stop Mode

These events restart the system clocks and load the program counter with the reset vector or with an interrupt vector:

- External reset — A low on the $\overline{\text{RST}}$ pin resets the MCU and loads the program counter with the contents of locations \$FFFE and \$FFFF.
- External interrupt — A high-to-low transition on an external interrupt pin loads the program counter with the contents of locations:
 - \$FFFA and \$FFFB; $\overline{\text{IRQ}}$ pin
 - \$FFE0 and \$FFE1; keyboard interrupt pins (low-to-high transition when KBIPx bits are set)
- Low-voltage inhibit (LVI) reset — A power supply voltage below the V_{TRIPF} voltage resets the MCU and loads the program counter with the contents of locations \$FFFE and \$FFFF.
- Break interrupt — In emulation mode, a break interrupt loads the program counter with the contents of locations \$FFFC and \$FFFD.
- Timebase module (TBM) interrupt — A TBM interrupt loads the program counter with the contents of locations \$FFDC and \$FFDD when the timebase counter has rolled over. This allows the TBM to generate a periodic wakeup from stop mode.

Upon exit from stop mode, the system clocks begin running after an oscillator stabilization delay. A 12-bit stop recovery counter inhibits the system clocks for 4096 CGMXCLK cycles after the reset or external interrupt.

The short stop recovery bit, SSREC, in the CONFIG1 register controls the oscillator stabilization delay during stop recovery. Setting SSREC reduces stop recovery time from 4096 CGMXCLK cycles to 32 CGMXCLK cycles.

NOTE

Use the full stop recovery time ($\text{SSREC} = 0$) in applications that use an external crystal unless the OSCENINSTOP bit is set.

Table 12-7. Port F Pin Functions

DDRF Bit	PTF Bit	I/O Pin Mode	Accesses to DDRF	Accesses to PTF	
			Read/Write	Read	Write
0	X ⁽¹⁾	Input, Hi-Z ⁽²⁾	DDRF7–DDRF0	Pin	PTF7–PTF0 ⁽³⁾
1	X	Output	DDRF7–DDRF0	PTF7–PTF0	PTF7–PTF0

1. X = Don't care

2. Hi-Z = High impedance

3. Writing affects data register, but does not affect input.

12.9 Port G

Port G is an 8-bit special-function port that shares all eight of its pins with the analog-to-digital converter (ADC) module.

12.9.1 Port G Data Register

The port G data register (PTG) contains a data latch for each of the eight port pins.

Address:	\$0441							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTG7	PTG6	PTG5	PTG4	PTG3	PTG2	PTG1	PTG0
Write:								
Reset:	Unaffected by reset							
Alternate Function:	AD23	AD22	AD21	AD20	AD19	AD18	AD17	AD16

Figure 12-23. Port G Data Register (PTG)

PTG7–PTG0 — Port G Data Bits

These read/write bits are software-programmable. Data direction of each port G pin is under the control of the corresponding bit in data direction register G. Reset has no effect on port G data.

AD23–AD16 — Analog-to-Digital Input Bits

AD23–AD16 are pins used for the input channels to the analog-to-digital converter module. The channel select bits in the ADC status and control register define which port G pin will be used as an ADC input and overrides any control from the port I/O logic by forcing that pin as the input to the analog circuitry.

NOTE

Care must be taken when reading port G while applying analog voltages to AD23–AD16 pins. If the appropriate ADC channel is not enabled, excessive current drain may occur if analog voltages are applied to the PTGx/ADx pin, while PTG is read as a digital input during the CPU read cycle. Those ports not selected as analog input channels are considered digital I/O ports.

13.4.2 Transmitter

Figure 13-5 shows the structure of the SCI transmitter and the registers are summarized in Figure 13-4. The baud rate clock source for the ESCI can be selected via the configuration bit, SCIBDSRC.

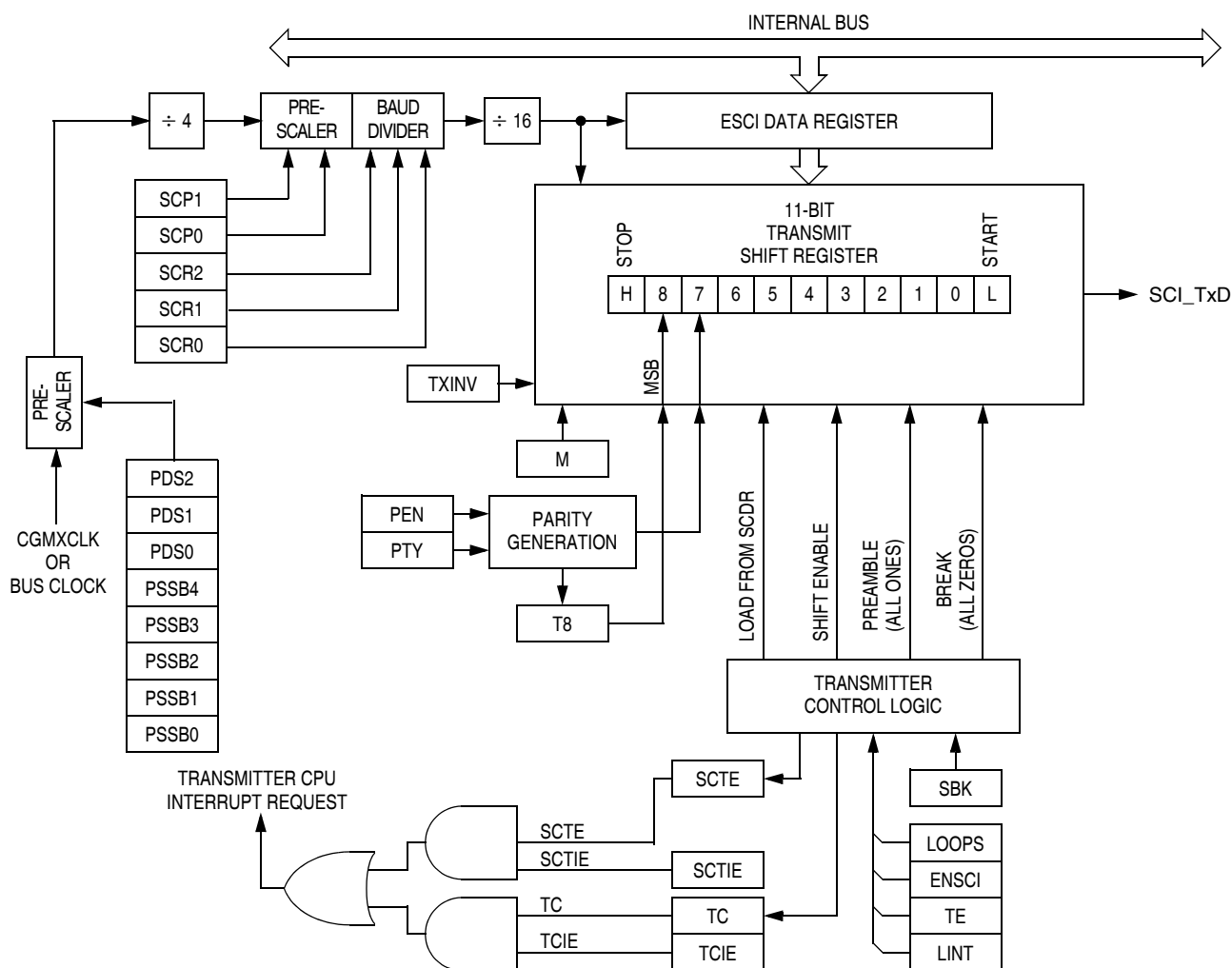


Figure 13-5. ESCI Transmitter

13.4.2.1 Character Length

The transmitter can accommodate either 8-bit or 9-bit data. The state of the M bit in ESCI control register 1 (SCC1) determines character length. When transmitting 9-bit data, bit T8 in ESCI control register 3 (SCC3) is the ninth bit (bit 8).

13.4.2.2 Character Transmission

During an ESCI transmission, the transmit shift register shifts a character out to the TxD pin. The ESCI data register (SCDR) is the write-only buffer between the internal data bus and the transmit shift register.

13.4.3.2 Character Reception

During an ESCI reception, the receive shift register shifts characters in from the RxD pin. The ESCI data register (SCDR) is the read-only buffer between the internal data bus and the receive shift register.

After a complete character shifts into the receive shift register, the data portion of the character transfers to the SCDR. The ESCI receiver full bit, SCRF, in ESCI status register 1 (SCS1) becomes set, indicating that the received byte can be read. If the ESCI receive interrupt enable bit, SCRIE, in SCC2 is also set, the SCRF bit generates a receiver CPU interrupt request.

13.4.3.3 Data Sampling

The receiver samples the RxD pin at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock is resynchronized at these times (see Figure 13-7):

- After every start bit
- After the receiver detects a data bit change from 1 to 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid 0)

To locate the start bit, data recovery logic does an asynchronous search for a 0 preceded by three 1s. When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

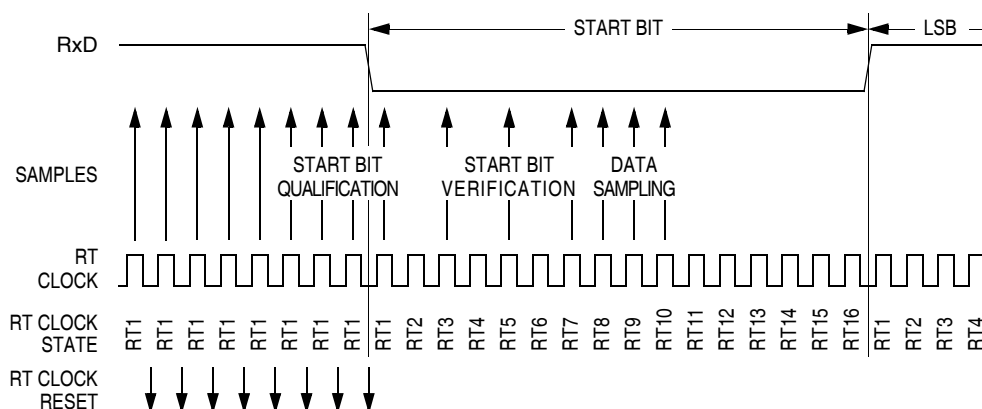


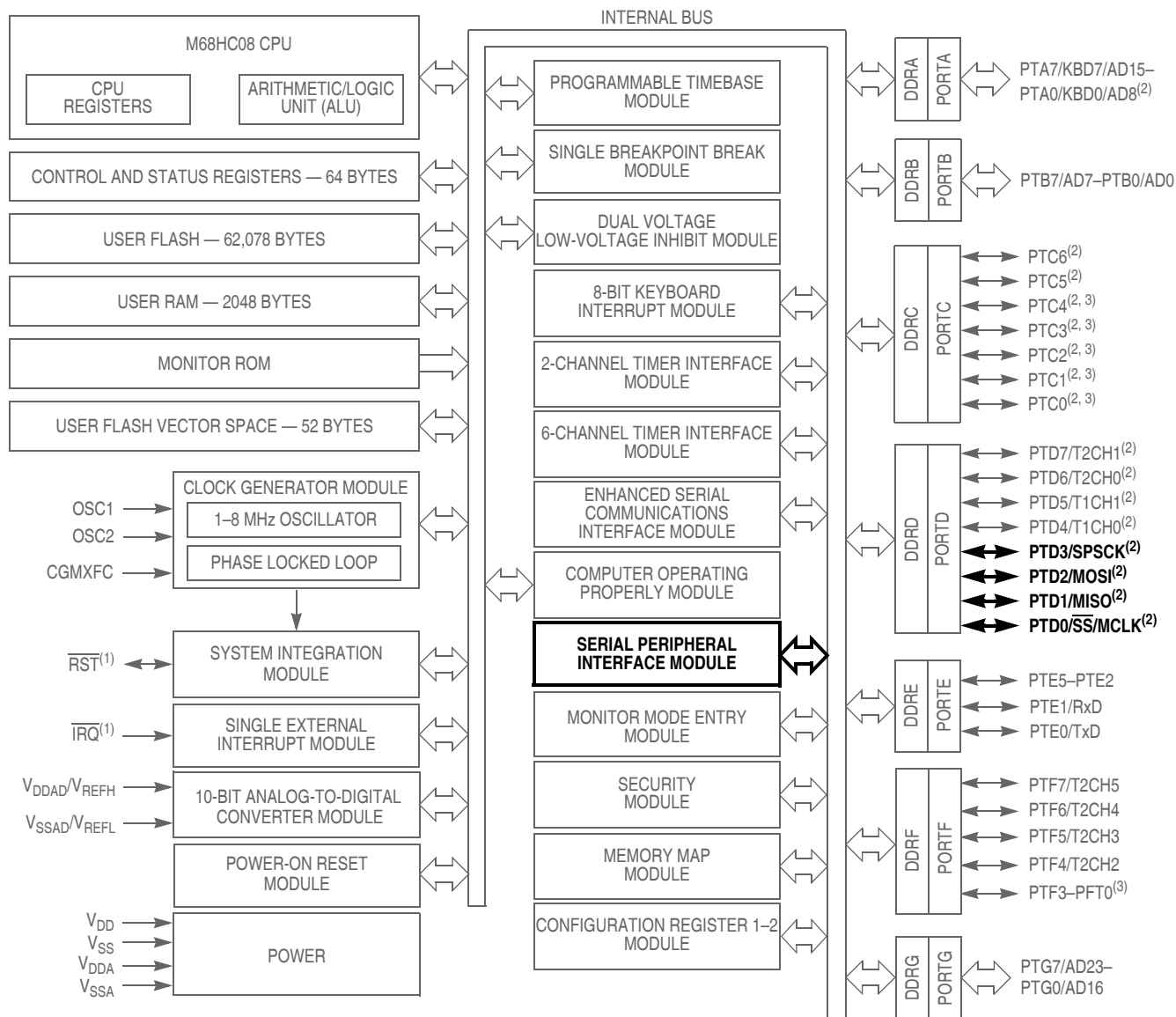
Figure 13-7. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Table 13-2 summarizes the results of the start bit verification samples.

Table 13-2. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

Serial Peripheral Interface (SPI) Module



1. Pin contains integrated pullup device.

2. Ports are software configurable with pullup device if input port or pullup/pulldown device for keyboard input.

3. Higher current drive port pins

Figure 15-1. Block Diagram Highlighting SPI Block and Pins

PS[2:0] — Prescaler Select Bits

These read/write bits select one of the seven prescaler outputs as the input to the TIM1 counter as Table 17-1 shows. Reset clears the PS[2:0] bits.

Table 17-1. Prescaler Selection

PS2	PS1	PS0	TIM1 Clock Source
0	0	0	Internal bus clock ÷ 1
0	0	1	Internal bus clock ÷ 2
0	1	0	Internal bus clock ÷ 4
0	1	1	Internal bus clock ÷ 8
1	0	0	Internal bus clock ÷ 16
1	0	1	Internal bus clock ÷ 32
1	1	0	Internal bus clock ÷ 64
1	1	1	Not available

17.8.2 TIM1 Counter Registers

The two read-only TIM1 counter registers contain the high and low bytes of the value in the TIM1 counter. Reading the high byte (T1CNTH) latches the contents of the low byte (T1CNTL) into a buffer. Subsequent reads of T1CNTH do not affect the latched T1CNTL value until T1CNTL is read. Reset clears the TIM1 counter registers. Setting the TIM1 reset bit (TRST) also clears the TIM1 counter registers.

NOTE

If you read T1CNTH during a break interrupt, be sure to unlatch T1CNTL by reading T1CNTL before exiting the break interrupt. Otherwise, T1CNTL retains the value latched during the break.

Address: \$0021	T1CNTH							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	0	0	0	0	0	0	0	0
Address: \$0022	T1CNTL							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0
	<div style="border: 1px solid black; width: 40px; height: 15px; display: inline-block;"></div> = Unimplemented							

Figure 17-6. TIM1 Counter Registers (T1CNTH:T1CNTL)

Table 18-2. Mode, Edge, and Level Selection

MSxB	MSxA	ELSxB	ELSxA	Mode	Configuration
X	0	0	0	Output preset	Pin under port control; initial output level high
X	1	0	0		Pin under port control; initial output level low
0	0	0	1	Input capture	Capture on rising edge only
0	0	1	0		Capture on falling edge only
0	0	1	1		Capture on rising or falling edge
0	1	0	0	Output compare or PWM	Software compare only
0	1	0	1		Toggle output on compare
0	1	1	0		Clear output on compare
0	1	1	1		Set output on compare
1	X	0	1	Buffered output compare or buffered PWM	Toggle output on compare
1	X	1	0		Clear output on compare
1	X	1	1		Set output on compare

ELSxB and ELSxA — Edge/Level Select Bits

When channel x is an input capture channel, these read/write bits control the active edge-sensing logic on channel x.

When channel x is an output compare channel, ELSxB and ELSxA control the channel x output behavior when an output compare occurs.

When ELSxB and ELSxA are both clear, channel x is not connected to port D or port F, and pin PTDx/T2CHx or pin PTFx/T2CHx is available as a general-purpose I/O pin. Table 18-2 shows how ELSxB and ELSxA work. Reset clears the ELSxB and ELSxA bits.

NOTE

After initially enabling a TIM2 channel register for input capture operation and selecting the edge sensitivity, clear CHxF to ignore any erroneous edge detection flags.

TOVx — Toggle-On-Overflow Bit

When channel x is an output compare channel, this read/write bit controls the behavior of the channel x output when the TIM2 counter overflows. When channel x is an input capture channel, TOVx has no effect. Reset clears the TOVx bit.

1 = Channel x pin toggles on TIM2 counter overflow.

0 = Channel x pin does not toggle on TIM2 counter overflow.

NOTE

When TOVx is set, a TIM2 counter overflow takes precedence over a channel x output compare if both occur at the same time.

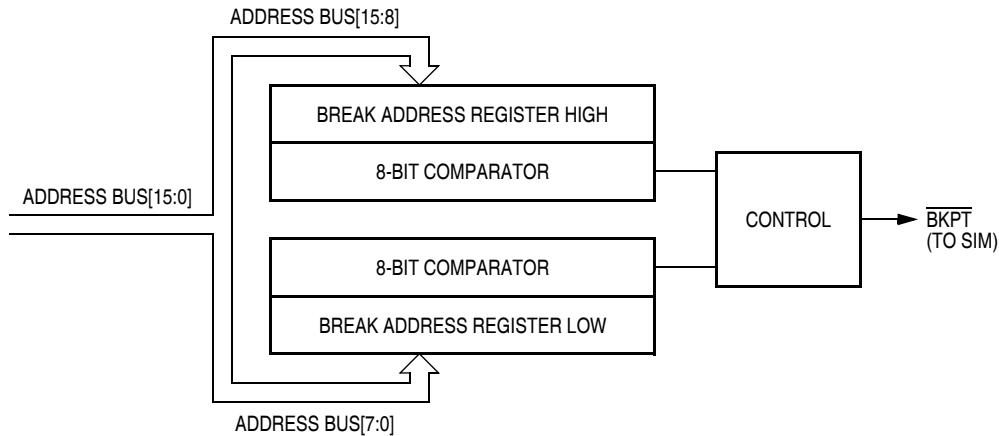


Figure 19-2. Break Module Block Diagram

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$FE00	Break Status Register (BSR) See page 266.	Read:	R	R	R	R	R	SBSW	R
		Write:	R	R	R	R	R	Note ⁽¹⁾	R
		Reset:	0						
\$FE03	Break Flag Control Register (BFCR) See page 266.	Read:	BCFE	R	R	R	R	R	R
		Write:	BCFE	R	R	R	R	R	R
		Reset:	0						
\$FE09	Break Address High Register (BRKH) See page 265.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9
		Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9
		Reset:	0	0	0	0	0	0	0
\$FE0A	Break Address Low Register (BRKL) See page 265.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
		Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
		Reset:	0	0	0	0	0	0	0
\$FE0B	Break Status and Control Register (BRKSCR) See page 265.	Read:	BRKE	BRKA	0	0	0	0	0
		Write:	BRKE	BRKA					
		Reset:	0	0	0	0	0	0	0

1. Writing a 0 clears SBSW.

 = Unimplemented R = Reserved

Figure 19-3. Break I/O Register Summary

Electrical Specifications

Characteristic ⁽¹⁾	Symbol	Min	Typ ⁽²⁾	Max	Unit
Pullup/pulldown resistors (as input only) Ports PTA7/KBD7–PTA0/KBD0, PTC6–PTC0, PTD7/T2CH1–PTD0/SS	R_{PU}	20	45	65	$k\Omega$
Capacitance Ports (as input or output)	C_{Out} C_{In}	— —	— —	12 8	pF
Monitor mode entry voltage	V_{TST}	$V_{DD} + 2.5$	—	$V_{DD} + 4.0$	V
Low-voltage inhibit, trip falling voltage	V_{TRIPF}	2.35	2.6	2.8	V
Low-voltage inhibit, trip rising voltage	V_{TRIPR}	2.4	2.66	2.9	V
Low-voltage inhibit reset/recover hysteresis ($V_{TRIPF} + V_{HYS} = V_{TRIPR}$)	V_{HYS}	—	100	—	mV
POR rearm voltage ⁽¹²⁾	V_{POR}	0	—	100	mV
POR reset voltage ⁽¹³⁾	V_{PORRST}	0	700	800	mV
POR rise time ramp rate ⁽¹⁴⁾	R_{POR}	0.02	—	—	V/ms

- $V_{DD} = 3.3 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = T_A (\text{min})$ to $T_A (\text{max})$, unless otherwise noted
- Typical values reflect average measurements at midpoint of voltage range, 25°C only.
- Run (operating) I_{DD} measured using external square wave clock source ($f_{OSC} = 16 \text{ MHz}$). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. $C_L = 20 \text{ pF}$ on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects run I_{DD} . Measured with all modules enabled.
- Wait I_{DD} measured using external square wave clock source ($f_{OSC} = 16 \text{ MHz}$). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. $C_L = 20 \text{ pF}$ on OSC2. All ports configured as inputs. OSC2 capacitance linearly affects wait I_{DD} . Measured with CGM and LVI enabled.
- Stop I_{DD} is measured with $OSC1 = V_{SS}$. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. Typical values at midpoint of voltage range, 25°C only.
- Stop I_{DD} with TBM enabled is measured using an external square wave clock source ($f_{OSC} = 4 \text{ MHz}$). All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All inputs configured as inputs.
- This parameter is characterized and not tested on each device.
- All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .
- Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
- Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).
- Pullups and pulldowns are disabled.
- Maximum is highest voltage that POR is guaranteed.
- Maximum is highest voltage that POR is possible.
- If minimum V_{DD} is not reached before the internal POR reset is released, \overline{RST} must be driven low externally until minimum V_{DD} is reached.

