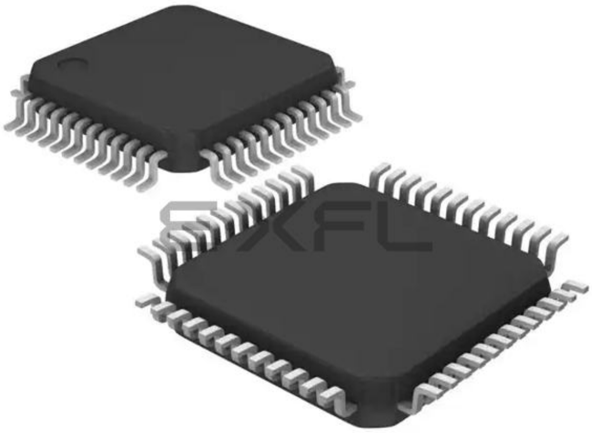
NXP USA Inc. - MC908GR60AMFAE Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	37
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908gr60amfae

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- Master reset pin and power-on reset (POR)
- On-chip FLASH memory:
    - MC68HC908GR60A — 60 Kbytes
    - MC68HC908GR48A — 48 Kbytes
    - MC68HC908GR32A — 32 Kbytes
- Random-access memory (RAM):
    - MC68HC908GR60A — 2048 bytes
    - MC68HC908GR48A — 1536 bytes
    - MC68HC908GR32A — 1536 bytes
- Serial peripheral interface (SPI) module
- Enhanced serial communications interface (ESCI) module
- One 16-bit, 2-channel timer interface module (TIM1) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- One 16-bit, 6-channel timer interface module (TIM2) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- Timebase module with clock prescaler circuitry for eight user selectable periodic real-time interrupts with optional active clock source during stop mode for periodic wakeup from stop using an external crystal
- 24-channel, 10-bit successive approximation analog-to-digital converter (ADC)
- 8-bit keyboard wakeup port with software selectable rising or falling edge detect, as well as high or low level detection
- Up to 53 general-purpose input/output (I/O) pins, including:
    - 40 shared-function I/O pins, depending on package choice
    - Up to 13 dedicated I/O pins, depending on package choice
- Selectable pullups on inputs only on ports A, C, and D. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce customer system cost
- High current 10-mA sink/source capability on all port pins
- Higher current 20-mA sink/source capability on PTC0–PTC4 and PTF0–PTF3
- User selectable clockout feature with divide by 1, 2, and 4 of the bus or crystal frequency
- User selection of having the oscillator enabled or disabled during stop mode
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Available packages:
    - 32-pin low-profile quad flat pack (LQFP)
    - 48-pin low-profile quad flat pack (LQFP)
    - 64-pin quad flat pack (QFP)
- Specific features in 32-pin LQFP are:
    - Port A is only 4 bits: PTA0–PTA3; shared with ADC and KBI modules
    - Port B is only 6 bits: PTB0–PTB5; shared with ADC module
    - Port C is only 2 bits: PTC0–PTC1
    - Port D is only 7 bits: PTD0–PTD6; shared with SPI, TIM1 and TIM2 modules
    - Port E is only 2 bits: PTE0–PTE1; shared with ESCI module

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FF80	FLASH-1 Block Protect Register (FL1BPR)[1] See page 43.	Read:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
		Write:								
		Reset:	Unaffected by reset							
$FF81	FLASH-2 Block Protect Register (FL2BPR)[1] See page 51.	Read:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
		Write:								
		Reset:	Unaffected by reset							
$FF88	FLASH-1 Control Register (FL1CR) See page 42.	Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
		Write:	▨	▨	▨	▨				
		Reset:	0	0	0	0	0	0	0	0
$FFFF	COP Control Register (COPCTL) See page 95.	Read:	Low byte of reset vector							
		Write:	Writing clears COP counter (any value)							
		Reset:	Unaffected by reset							

[1] Non-volatile FLASH register

▨ = Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 9 of 9)

Table 2-1. Vector Addresses

Vector Priority	Vector	Address	Vector
Lowest	IF24	$FFCC	TIM2 Channel 5 Vector (High)
		$FFCD	TIM2 Channel 5 Vector (Low)
	IF23	$FFCE	TIM2 Channel 4 Vector (High)
		$FFCF	TIM2 Channel 4 Vector (Low)
	IF22	$FFD0	TIM2 Channel 3 Vector (High)
		$FFD1	TIM2 Channel 3 Vector (Low)
	IF21	$FFD2	TIM2 Channel 2 Vector (High)
		$FFD3	TIM2 Channel 2 Vector (Low)
	IF20 ↓ IF17	$FFD4 ↓ $FFDB	Reserved
	IF16	$FFDC	Timebase Vector (High)
		$FFDD	Timebase Vector (Low)
	IF15	$FFDE	ADC Conversion Complete Vector (High)
↓		$FFDF	ADC Conversion Complete Vector (Low)

Continued on next page

Table 7-2. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write						Control		Register/Memory							
	DIR	DIR	REL	DIR	INH	INH	IX1	SP1	IX	INH	INH	IMM	DIR	EXT	IX2	SP2	IX1	SP1	IX
MSB LSB	0	1	2	3	4	5	6	9E6	7	8	9	A	B	C	D	9ED	E	9EE	F
0	5 BRSET0 3 DIR	4 BSET0 2 DIR	3 BRA 2 REL	4 NEG 2 DIR	1 NEGA 1 INH	1 NEGX 1 INH	4 NEG 2 IX1	5 NEG 3 SP1	3 NEG 1 IX	7 RTI 1 INH	3 BGE 2 REL	2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	4 SUB 3 IX2	5 SUB 4 SP2	3 SUB 2 IX1	4 SUB 3 SP1	2 SUB 1 IX
1	5 BRCLR0 3 DIR	4 BCLR0 2 DIR	3 BRN 2 REL	5 CBEQ 3 DIR	4 CBEQA 3 IMM	4 CBEQX 3 IMM	5 CBEQ 3 IX1+	6 CBEQ 4 SP1	4 CBEQ 2 IX+	4 RTS 1 INH	3 BLT 2 REL	2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	4 CMP 3 IX2	5 CMP 4 SP2	3 CMP 2 IX1	4 CMP 3 SP1	2 CMP 1 IX
2	5 BRSET1 3 DIR	4 BSET1 2 DIR	3 BHI 2 REL		5 MUL 1 INH	7 DIV 1 INH	3 NSA 1 INH		2 DAA 1 INH		3 BGT 2 REL	2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	4 SBC 3 IX2	5 SBC 4 SP2	3 SBC 2 IX1	4 SBC 3 SP1	2 SBC 1 IX
3	5 BRCLR1 3 DIR	4 BCLR1 2 DIR	3 BLS 2 REL	4 COM 2 DIR	1 COMA 1 INH	1 COMX 1 INH	4 COM 2 IX1	5 COM 3 SP1	3 COM 1 IX	9 SWI 1 INH	3 BLE 2 REL	2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	4 CPX 3 IX2	5 CPX 4 SP2	3 CPX 2 IX1	4 CPX 3 SP1	2 CPX 1 IX
4	5 BRSET2 3 DIR	4 BSET2 2 DIR	3 BCC 2 REL	4 LSR 2 DIR	1 LSRA 1 INH	1 LSRX 1 INH	4 LSR 2 IX1	5 LSR 3 SP1	3 LSR 1 IX	2 TAP 1 INH	2 TXS 1 INH	2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	4 AND 3 IX2	5 AND 4 SP2	3 AND 2 IX1	4 AND 3 SP1	2 AND 1 IX
5	5 BRCLR2 3 DIR	4 BCLR2 2 DIR	3 BCS 2 REL	4 STHX 2 DIR	3 LDHX 3 IMM	4 LDHX 2 DIR	3 CPHX 3 IMM		4 CPHX 2 DIR	1 TPA 1 INH	2 TSX 1 INH	2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	4 BIT 3 IX2	5 BIT 4 SP2	3 BIT 2 IX1	4 BIT 3 SP1	2 BIT 1 IX
6	5 BRSET3 3 DIR	4 BSET3 2 DIR	3 BNE 2 REL	4 ROR 2 DIR	1 RORA 1 INH	1 RORX 1 INH	4 ROR 2 IX1	5 ROR 3 SP1	3 ROR 1 IX	2 PULA 1 INH		2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	4 LDA 3 IX2	5 LDA 4 SP2	3 LDA 2 IX1	4 LDA 3 SP1	2 LDA 1 IX
7	5 BRCLR3 3 DIR	4 BCLR3 2 DIR	3 BEQ 2 REL	4 ASR 2 DIR	1 ASRA 1 INH	1 ASRX 1 INH	4 ASR 2 IX1	5 ASR 3 SP1	3 ASR 1 IX	2 PSHA 1 INH	1 TAX 1 INH	2 AIS 2 IMM	3 STA 2 DIR	4 STA 3 EXT	4 STA 3 IX2	5 STA 4 SP2	3 STA 2 IX1	4 STA 3 SP1	2 STA 1 IX
8	5 BRSET4 3 DIR	4 BSET4 2 DIR	3 BHCC 2 REL	4 LSL 2 DIR	1 LSLA 1 INH	1 LSLX 1 INH	4 LSL 2 IX1	5 LSL 3 SP1	3 LSL 1 IX	2 PULX 1 INH	1 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	4 EOR 3 IX2	5 EOR 4 SP2	3 EOR 2 IX1	4 EOR 3 SP1	2 EOR 1 IX
9	5 BRCLR4 3 DIR	4 BCLR4 2 DIR	3 BHCS 2 REL	4 ROL 2 DIR	1 ROLA 1 INH	1 ROLX 1 INH	4 ROL 2 IX1	5 ROL 3 SP1	3 ROL 1 IX	2 PSHX 1 INH	1 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	4 ADC 3 IX2	5 ADC 4 SP2	3 ADC 2 IX1	4 ADC 3 SP1	2 ADC 1 IX
A	5 BRSET5 3 DIR	4 BSET5 2 DIR	3 BPL 2 REL	4 DEC 2 DIR	1 DECA 1 INH	1 DECX 1 INH	4 DEC 2 IX1	5 DEC 3 SP1	3 DEC 1 IX	2 PULH 1 INH	2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	4 ORA 3 IX2	5 ORA 4 SP2	3 ORA 2 IX1	4 ORA 3 SP1	2 ORA 1 IX
B	5 BRCLR5 3 DIR	4 BCLR5 2 DIR	3 BMI 2 REL	5 DBNZ 3 DIR	3 DBNZA 2 INH	3 DBNZX 2 INH	5 DBNZ 3 IX1	6 DBNZ 4 SP1	4 DBNZ 2 IX	2 PSHH 1 INH	2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	4 ADD 3 IX2	5 ADD 4 SP2	3 ADD 2 IX1	4 ADD 3 SP1	2 ADD 1 IX
C	5 BRSET6 3 DIR	4 BSET6 2 DIR	3 BMC 2 REL	4 INC 2 DIR	1 INCA 1 INH	1 INCX 1 INH	4 INC 2 IX1	5 INC 3 SP1	3 INC 1 IX	1 CLRH 1 INH	1 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2		3 JMP 2 IX1		2 JMP 1 IX
D	5 BRCLR6 3 DIR	4 BCLR6 2 DIR	3 BMS 2 REL	3 TST 2 DIR	1 TSTA 1 INH	1 TSTX 1 INH	3 TST 2 IX1	4 TST 3 SP1	2 TST 1 IX		1 NOP 1 INH	4 BSR 2 REL	4 JSR 2 DIR	5 JSR 3 EXT	6 JSR 3 IX2		5 JSR 2 IX1		4 JSR 1 IX
E	5 BRSET7 3 DIR	4 BSET7 2 DIR	3 BIL 2 REL		5 MOV 3 DD	4 MOV 2 DIX+	4 MOV 3 IMD		4 MOV 2 IX+D	1 STOP 1 INH	*	2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	4 LDX 3 IX2	5 LDX 4 SP2	3 LDX 2 IX1	4 LDX 3 SP1	2 LDX 1 IX
F	5 BRCLR7 3 DIR	4 BCLR7 2 DIR	3 BIH 2 REL	3 CLR 2 DIR	1 CLRA 1 INH	1 CLRX 1 INH	3 CLR 2 IX1	4 CLR 3 SP1	2 CLR 1 IX	1 WAIT 1 INH	1 TXA 1 INH	2 AIX 2 IMM	3 STX 2 DIR	4 STX 3 EXT	4 STX 3 IX2	5 STX 4 SP2	3 STX 2 IX1	4 STX 3 SP1	2 STX 1 IX

INH	Inherent	REL	Relative	SP1	Stack Pointer, 8-Bit Offset
IMM	Immediate	IX	Indexed, No Offset	SP2	Stack Pointer, 16-Bit Offset
DIR	Direct	IX1	Indexed, 8-Bit Offset	IX+	Indexed, No Offset with Post Increment
EXT	Extended	IX2	Indexed, 16-Bit Offset		
DD	Direct-Direct	IMD	Immediate-Direct	IX1+	Indexed, 1-Byte Offset with Post Increment
IX+D	Indexed-Direct	DIX+	Direct-Indexed		

*Pre-byte for stack pointer indexed instructions

	MSB LSB	0	High Byte of Opcode in Hexadecimal
Low Byte of Opcode in Hexadecimal	0	5 BRSET0 3 DIR	Cycles Opcode Mnemonic Number of Bytes / Addressing Mode

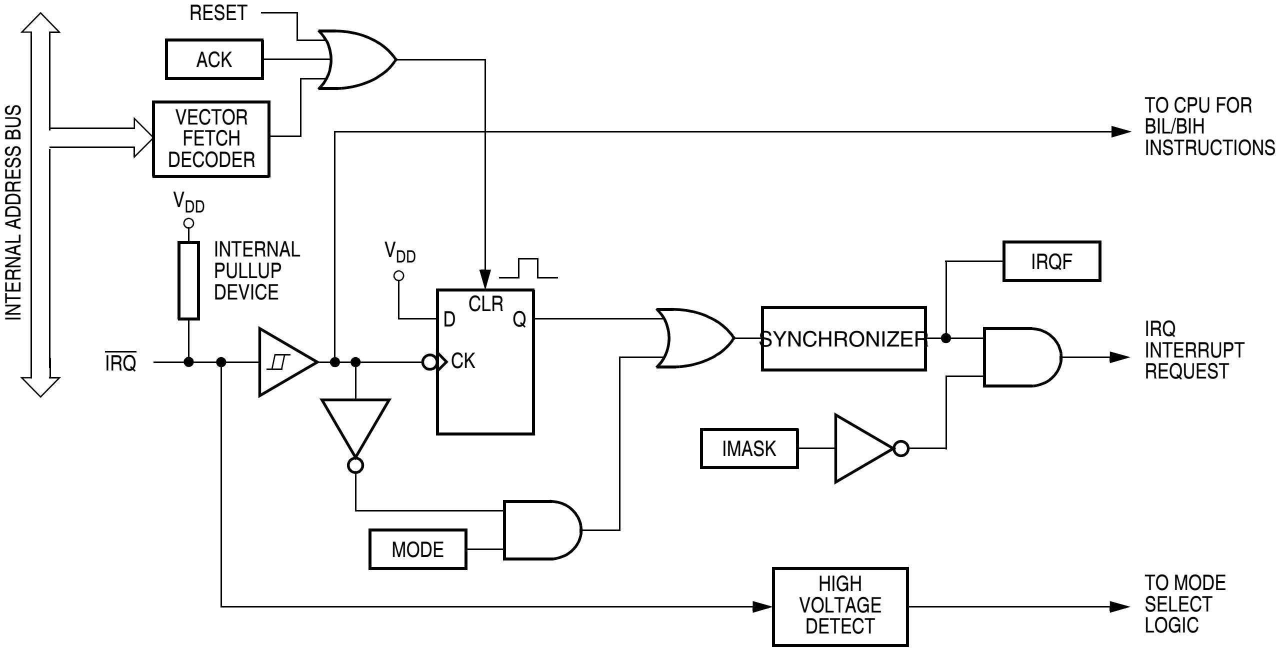


Figure 8-1. IRQ Module Block Diagram

The vector fetch or software clear may occur before or after the interrupt pin returns to a high level. As long as the pin is low, the interrupt request remains pending. A reset will clear the latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

When set, the IMASK bit in the INTSCR masks all external interrupt requests. A latched interrupt request is not presented to the interrupt priority logic unless the IMASK bit is clear.

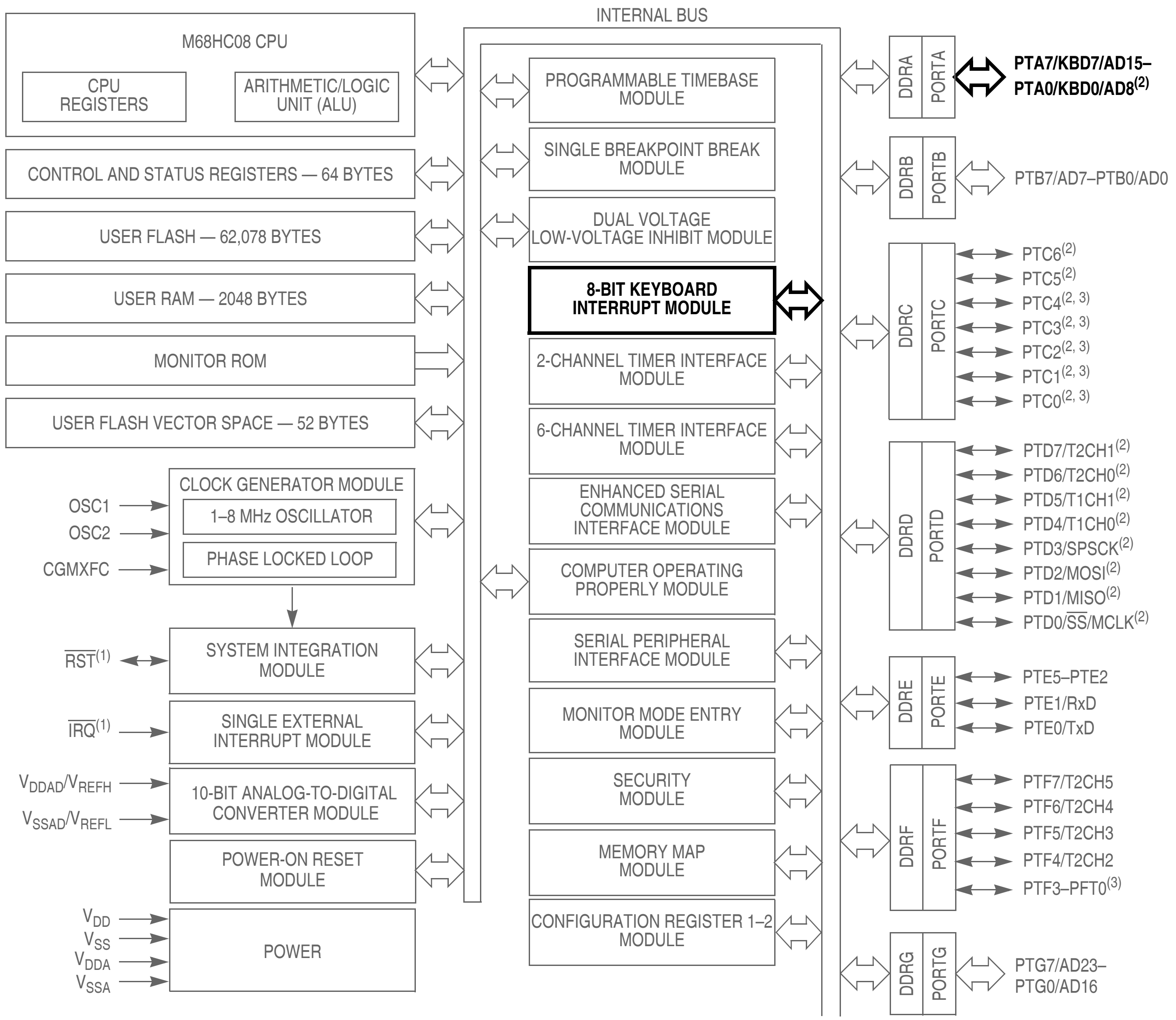
NOTE

The interrupt mask (I) in the condition code register (CCR) masks all interrupt requests, including external interrupt requests.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001D	IRQ Status and Control Register (INTSCR) See page 112.	Read:	0	0	0	0	IRQF	0	IMASK	MODE
		Write:	▨	▨	▨	▨	▨	ACK		
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 8-2. IRQ I/O Register Summary


INTERNAL BUS
M68HC08 CPU
CPU REGISTERS
ARITHMETIC/LOGIC UNIT (ALU)
CONTROL AND STATUS REGISTERS — 64 BYTES
USER FLASH — 62,078 BYTES
USER RAM — 2048 BYTES
MONITOR ROM
USER FLASH VECTOR SPACE — 52 BYTES
CLOCK GENERATOR MODULE
1–8 MHz OSCILLATOR
PHASE LOCKED LOOP
OSC1
OSC2
CGMXFC
SYSTEM INTEGRATION MODULE
RST(1)
SINGLE EXTERNAL INTERRUPT MODULE
IRQ(1)
10-BIT ANALOG-TO-DIGITAL CONVERTER MODULE
VDDAD/VREFH
VSSAD/VREFL
POWER-ON RESET MODULE
POWER
VDD
VSS
VDDA
VSSA
PROGRAMMABLE TIMEBASE MODULE
SINGLE BREAKPOINT BREAK MODULE
DUAL VOLTAGE LOW-VOLTAGE INHIBIT MODULE
8-BIT KEYBOARD INTERRUPT MODULE
2-CHANNEL TIMER INTERFACE MODULE
6-CHANNEL TIMER INTERFACE MODULE
ENHANCED SERIAL COMMUNICATIONS INTERFACE MODULE
COMPUTER OPERATING PROPERLY MODULE
SERIAL PERIPHERAL INTERFACE MODULE
MONITOR MODE ENTRY MODULE
SECURITY MODULE
MEMORY MAP MODULE
CONFIGURATION REGISTER 1–2 MODULE
DDRA
PORTA
PTA7/KBD7/AD15–PTA0/KBD0/AD8(2)
DDRB
PORTB
PTB7/AD7–PTB0/AD0
DDRC
PORTC
PTC6(2)
PTC5(2)
PTC4(2, 3)
PTC3(2, 3)
PTC2(2, 3)
PTC1(2, 3)
PTC0(2, 3)
DDRD
PORTD
PTD7/T2CH1(2)
PTD6/T2CH0(2)
PTD5/T1CH1(2)
PTD4/T1CH0(2)
PTD3/SPSCK(2)
PTD2/MOSI(2)
PTD1/MISO(2)
PTD0/SS/MCLK(2)
DDRE
PORTE
PTE5–PTE2
PTE1/RxD
PTE0/TxD
DDRF
PORTF
PTF7/T2CH5
PTF6/T2CH4
PTF5/T2CH3
PTF4/T2CH2
PTF3–PFT0(3)
DDRG
PORTG
PTG7/AD23–PTG0/AD16

1. Pin contains integrated pullup device.

2. Ports are software configurable with pullup device if input port or pullup/pulldown device for keyboard input.

3. Higher current drive port pins

Figure 9-1. Block Diagram Highlighting KBI Block and Pins

10.14 Exiting Wait Mode

These events restart the CPU clock and load the program counter with the reset vector or with an interrupt vector:

- External reset — A low on the $\overline{\text{RST}}$ pin resets the MCU and loads the program counter with the contents of locations $FFFE and $FFFF.
- External interrupt — A high-to-low transition on an external interrupt pin ($\overline{\text{IRQ}}$ pin) loads the program counter with the contents of locations: $FFFA and $FFFB; $\overline{\text{IRQ}}$ pin.
- Break interrupt — In emulation mode, a break interrupt loads the program counter with the contents of $FFFC and $FFFD.
- Computer operating properly (COP) module reset — A timeout of the COP counter resets the MCU and loads the program counter with the contents of $FFFE and $FFFF.
- Low-voltage inhibit (LVI) module reset — A power supply voltage below the V_{TRIPF} voltage resets the MCU and loads the program counter with the contents of locations $FFFE and $FFFF.
- Clock generator module (CGM) interrupt — A CPU interrupt request from the CGM loads the program counter with the contents of $FFF8 and $FFF9.
- Keyboard interrupt (KBI) module — A CPU interrupt request from the KBI module loads the program counter with the contents of $FFE0 and $FFE1.
- Timer 1 interface (TIM1) module interrupt — A CPU interrupt request from the TIM1 loads the program counter with the contents of:
  - $FFF2 and $FFF3; TIM1 overflow
  - $FFF4 and $FFF5; TIM1 channel 1
  - $FFF6 and $FFF7; TIM1 channel 0
- Timer 2 interface module (TIM2) interrupt — A CPU interrupt request from the TIM2 loads the program counter with the contents of:
  - $FFEC and $FFED; TIM2 overflow
  - $FFEE and $FFEF; TIM2 channel 1
  - $FFF0 and $FFF1; TIM2 channel 0
  - $FFCC and $FFCD; TIM2 channel 5
  - $FFCE and $FFCF; TIM2 channel 4
  - $FFD0 and $FFD1; TIM2 channel 3
  - $FFD2 and $FFD3; TIM2 channel 2
- Serial peripheral interface (SPI) module interrupt — A CPU interrupt request from the SPI loads the program counter with the contents of:
  - $FFE8 and $FFE9; SPI transmitter
  - $FFEA and $FFEB; SPI receiver
- Serial communications interface (SCI) module interrupt — A CPU interrupt request from the SCI loads the program counter with the contents of:
  - $FFE2 and $FFE3; SCI transmitter
  - $FFE4 and $FFE5; SCI receiver
  - $FFE6 and $FFE7; SCI receiver error
- Analog-to-digital converter (ADC) module interrupt — A CPU interrupt request from the ADC loads the program counter with the contents of: $FFDE and $FFDF; ADC conversion complete.
- Timebase module (TBM) interrupt — A CPU interrupt request from the TBM loads the program counter with the contents of: $FFDC and $FFDD; TBM interrupt.

LVISTOP, LVIPWRD, LVI5OR3, and LVIRSTD are in the configuration register (CONFIG1). See Figure 5-2. Configuration Register 1 (CONFIG1) for details of the LVI's configuration bits. Once an LVI reset occurs, the MCU remains in reset until V_{DD} rises above a voltage, V_{TRIPR}, which causes the MCU to exit reset. See 14.3.2.5 Low-Voltage Inhibit (LVI) Reset for details of the interaction between the SIM and the LVI. The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR).

An LVI reset also drives the $\overline{\text{RST}}$ pin low to provide low-voltage protection to external peripheral devices.

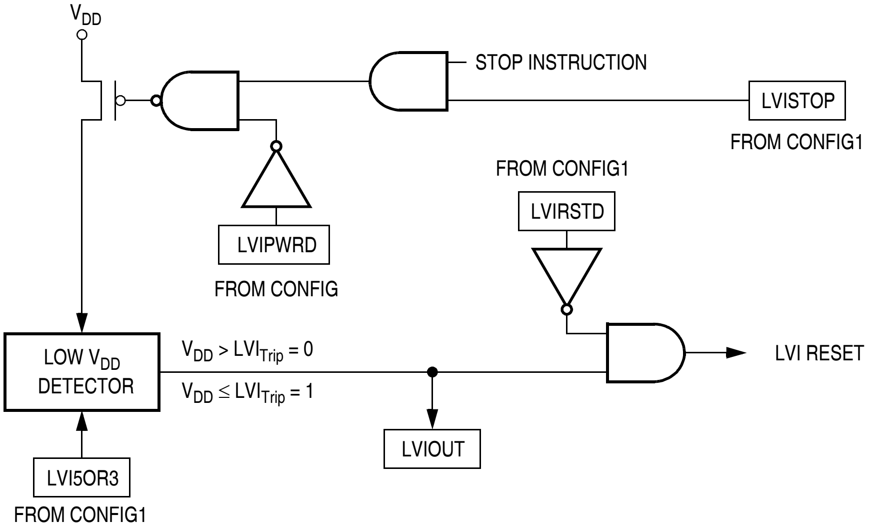


Figure 11-1. LVI Module Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE0C	LVI Status Register (LVISR) See page 129.	Read:	LVIOUT	0	0	0	0	0	0	0
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 11-2. LVI I/O Register Summary

11.3.1 Polled LVI Operation

In applications that can operate at V_{DD} levels below the V_{TRIPF} level, software can monitor V_{DD} by polling the LVIOUT bit. In the configuration register, the LVIPWRD bit must be 0 to enable the LVI module, and the LVIRSTD bit must be 1 to disable LVI resets.

11.3.2 Forced Reset Operation

In applications that require V_{DD} to remain above the V_{TRIPF} level, enabling LVI resets allows the LVI module to reset the MCU when V_{DD} falls below the V_{TRIPF} level. In the configuration register, the LVIPWRD and LVIRSTD bits must be cleared to enable the LVI module and to enable LVI resets.

Table 12-1. Port Control Register Bits Summary (Continued)

Port	Bit	DDR	Module Control		Module Control		Pin
C	0	DDRC0			—	—	PTC0
	1	DDRC1					PTC1
	2	DDRC2					PTC2
	3	DDRC3					PTC3
	4	DDRC4					PTC4
	5	DDRC5					PTC5
	6	DDRC6					PTC6
D	0	DDRD0	SPI	SPE	—	—	PTD0/$\overline{SS}$/MCLK
	1	DDRD1					PTD1/MISO
	2	DDRD2					PTD2/MOSI
	3	DDRD3					PTD3/SPSCK
	4	DDRD4	TIM1	ELS0B:ELS0A			PTD4/T1CH0
	5	DDRD5		ELS1B:ELS1A			PTD5/T1CH1
	6	DDRD6	TIM2	ELS0B:ELS0A			PTD6/T2CH0
	7	DDRD7		ELS1B:ELS1A			PTD7/T2CH1
E	0	DDRE0	SCI	ENSCI	—	—	PTE0/TxD
	1	DDRE1					PTE1/RxD
	2	DDRE2					PTE2
	3	DDRE3					PTE3
	4	DDRE4					PTE4
	5	DDRE5					PTE5
F	0	DDRF0			—	—	PTF0
	1	DDRF1					PTF1
	2	DDRF2					PTF2
	3	DDRF3					PTF3
	4	DDRF4	TIM2	ELS2B:ELS2A			PTF4/T2CH2
	5	DDRF5		ELS3B:ELS3A			PTF5/T2CH3
	6	DDRF6		ELS4B:ELS4A			PTF6/T2CH4
	7	DDRF7		ELS5B:ELS5A			PTF7/T2CH5
G	0	DDRG0	ADC	ADCH[23:16]	—	—	PTG0/AD16
	1	DDRG1					PTG1/AD17
	2	DDRG2					PTG2/AD18
	3	DDRG3					PTG3/AD19
	4	DDRG4					PTG4/AD20
	5	DDRG5					PTG5/AD21
	6	DDRG6					PTG6/AD22
	7	DDRG7					PTG7/AD23

12.3 Port A

Port A is an 8-bit special-function port that shares all eight of its pins with the keyboard interrupt (KBI) module and the ADC module. Port A also has software configurable pullup devices if configured as an input port.

12.3.1 Port A Data Register

The port A data register (PTA) contains a data latch for each of the eight port A pins.

Address:	$0000							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
Reset:	Unaffected by reset							
Alternate Function:	KBD7	KBD6	KBD5	KBD4	KBD3	KBD2	KBD1	KBD0
Alternate Function:	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

Figure 12-2. Port A Data Register (PTA)

PTA7–PTA0 — Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

KBD7–KBD0 — Keyboard Inputs

The keyboard interrupt enable bits, KBIE7–KBIE0, in the keyboard interrupt control register (KBICR) enable the port A pins as external interrupt pins. See Chapter 9 Keyboard Interrupt Module (KBI)

AD15–AD8 — Analog-to-Digital Input Bits

AD15–AD8 are pins used for the input channels to the analog-to-digital converter module. The channel select bits in the ADC status and control register define which port A pin will be used as an ADC input and overrides any control from the port I/O logic by forcing that pin as the input to the analog circuitry.

NOTE

Care must be taken when reading port A while applying analog voltages to AD15–AD8 pins. If the appropriate ADC channel is not enabled, excessive current drain may occur if analog voltages are applied to the PTAx/KBDx/ADx pin, while PTA is read as a digital input during the CPU read cycle. Those ports not selected as analog input channels are considered digital I/O ports.

13.4.2.4 Idle Characters

For TXINV = 0 (output not inverted), a transmitted idle character contains all 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCC1. The preamble is a synchronizing idle character that begins every transmission.

If the TE bit is cleared during a transmission, the TxD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the character currently being transmitted.

NOTE

When a break sequence is followed immediately by an idle character, this SCI design exhibits a condition in which the break character length is reduced by one half bit time. In this instance, the break sequence will consist of a valid start bit, eight or nine data bits (as defined by the M bit in SCC1) of 0 and one half data bit length of 0 in the stop bit position followed immediately by the idle character. To ensure a break character of the proper length is transmitted, always queue up a byte of data to be transmitted while the final break sequence is in progress.

When queueing an idle character, return the TE bit to 1 before the stop bit of the current character shifts out to the TxD pin. Setting TE after the stop bit appears on TxD causes data previously written to the SCDR to be lost. A good time to toggle the TE bit for a queued idle character is when the SCTE bit becomes set and just before writing the next byte to the SCDR.

13.4.2.5 Inversion of Transmitted Output

The transmit inversion bit (TXINV) in ESCI control register 1 (SCC1) reverses the polarity of transmitted data. All transmitted values including idle, break, start, and stop bits, are inverted when TXINV is at 1. See 13.8.1 ESCI Control Register 1.

13.4.2.6 Transmitter Interrupts

These conditions can generate CPU interrupt requests from the ESCI transmitter:

- ESCI transmitter empty (SCTE) — The SCTE bit in SCS1 indicates that the SCDR has transferred a character to the transmit shift register. SCTE can generate a transmitter CPU interrupt request. Setting the ESCI transmit interrupt enable bit, SCTIE, in SCC2 enables the SCTE bit to generate transmitter CPU interrupt requests.
- Transmission complete (TC) — The TC bit in SCS1 indicates that the transmit shift register and the SCDR are empty and that no break or idle character has been generated. The transmission complete interrupt enable bit, TCIE, in SCC2 enables the TC bit to generate transmitter CPU interrupt requests.

13.4.3 Receiver

Figure 13-6 shows the structure of the ESCI receiver. The receiver I/O registers are summarized in Figure 13-4.

NOTE

With the WAKE bit clear, setting the RWU bit after the RxD pin has been idle will cause the receiver to wake up.

13.4.3.7 Receiver Interrupts

These sources can generate CPU interrupt requests from the ESCI receiver:

- ESCI receiver full (SCRF) — The SCRF bit in SCS1 indicates that the receive shift register has transferred a character to the SCDR. SCRF can generate a receiver CPU interrupt request. Setting the ESCI receive interrupt enable bit, SCRIE, in SCC2 enables the SCRF bit to generate receiver CPU interrupts.
- Idle input (IDLE) — The IDLE bit in SCS1 indicates that 10 or 11 consecutive 1s shifted in from the RxD pin. The idle line interrupt enable bit, ILIE, in SCC2 enables the IDLE bit to generate CPU interrupt requests.

13.4.3.8 Error Interrupts

These receiver error flags in SCS1 can generate CPU interrupt requests:

- Receiver overrun (OR) — The OR bit indicates that the receive shift register shifted in a new character before the previous character was read from the SCDR. The previous character remains in the SCDR, and the new character is lost. The overrun interrupt enable bit, ORIE, in SCC3 enables OR to generate ESCI error CPU interrupt requests.
- Noise flag (NF) — The NF bit is set when the ESCI detects noise on incoming data or break characters, including start, data, and stop bits. The noise error interrupt enable bit, NEIE, in SCC3 enables NF to generate ESCI error CPU interrupt requests.
- Framing error (FE) — The FE bit in SCS1 is set when a 0 occurs where the receiver expects a stop bit. The framing error interrupt enable bit, FEIE, in SCC3 enables FE to generate ESCI error CPU interrupt requests.
- Parity error (PE) — The PE bit in SCS1 is set when the ESCI detects a parity error in incoming data. The parity error interrupt enable bit, PEIE, in SCC3 enables PE to generate ESCI error CPU interrupt requests.

13.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

13.5.1 Wait Mode

The ESCI module remains active in wait mode. Any enabled CPU interrupt request from the ESCI module can bring the MCU out of wait mode.

If ESCI module functions are not required during wait mode, reduce power consumption by disabling the module before executing the WAIT instruction.

13.5.2 Stop Mode

The ESCI module is inactive in stop mode. The STOP instruction does not affect ESCI register states. ESCI module operation resumes after the MCU exits stop mode.

Because the internal clock is inactive during stop mode, entering stop mode during an ESCI transmission or reception results in invalid data.

Interrupt Status Register 4

Address: $FE07

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	IF24	IF23
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 14-15. Interrupt Status Register 4 (INT4)

Bits 7–2 — Always read 0

IF24–IF23 — Interrupt Flags 24–23

These flags indicate the presence of an interrupt request from the source shown in Table 14-3.

1 = Interrupt request present
0 = No interrupt request present

14.5.2 Reset

All reset sources always have equal and highest priority and cannot be arbitrated.

14.5.3 Break Interrupts

The break module can stop normal program flow at a software-programmable break point by asserting its break interrupt output (see Chapter 17 Timer Interface Module (TIM1) and Chapter 18 Timer Interface Module (TIM2)). The SIM puts the CPU into the break state by forcing it to the SWI vector location. Refer to the break interrupt subsection of each module to see how each module is affected by the break state.

14.5.4 Status Flag Protection in Break Mode

The SIM controls whether status flags contained in other modules can be cleared during break mode. The user can select whether flags are protected from being cleared by properly initializing the break clear flag enable bit (BCFE) in the SIM break flag control register (BFCR).

Protecting flags in break mode ensures that set flags will not be cleared while in break mode. This protection allows registers to be freely read and written during break mode without losing status flag information.

Setting the BCFE bit enables the clearing mechanisms. Once cleared in break mode, a flag remains cleared even when break mode is exited. Status flags with a 2-step clearing mechanism — for example, a read of one register followed by the read or write of another — are protected, even when the first step is accomplished prior to entering break mode. Upon leaving break mode, execution of the second step will clear the flag as normal.

14.6 Low-Power Modes

Executing the WAIT or STOP instruction puts the MCU in a low power-consumption mode for standby situations. The SIM holds the CPU in a non-clocked state. The operation of each of these modes is described in the following subsections. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupts to occur.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0023	TIM1 Counter Modulo Register High (T1MODH) See page 236.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$0024	TIM1 Counter Modulo Register Low (T1MODL) See page 236.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$0025	TIM1 Channel 0 Status and Control Register (T1SC0) See page 237.	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0026	TIM1 Channel 0 Register High (T1CH0H) See page 240.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	Indeterminate after reset							
$0027	TIM1 Channel 0 Register Low (T1CH0L) See page 240.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Indeterminate after reset							
$0028	TIM1 Channel 1 Status and Control Register (T1SC1) See page 237.	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0		▨					
		Reset:	0	0	0	0	0	0	0	0
$0029	TIM1 Channel 1 Register High (T1CH1H) See page 240.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	Indeterminate after reset							
$002A	TIM1 Channel 1 Register Low (T1CH1L) See page 240.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	Indeterminate after reset							

▨ = Unimplemented

Figure 17-3. TIM1 I/O Register Summary (Continued)

17.3.1 TIM1 Counter Prescaler

The TIM1 clock source is one of the seven prescaler outputs. The prescaler generates seven clock rates from the internal bus clock. The prescaler select bits, PS[2:0], in the TIM1 status and control register (T1SC) select the TIM1 clock source.

17.3.2 Input Capture

With the input capture function, the TIM1 can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIM1 latches the contents of the TIM1 counter into the TIM1 channel registers, T1CHxH:T1CHxL. The polarity of the active edge is programmable. Input captures can generate TIM1 central processor unit (CPU) interrupt requests.

NOTE

When TOVx is set, a TIM1 counter overflow takes precedence over a channel x output compare if both occur at the same time.

CHxMAX — Channel x Maximum Duty Cycle Bit

When the TOVx bit is at 1, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100%. As Figure 17-9 shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at the 100% duty cycle level until the cycle after CHxMAX is cleared.

NOTE

The 100% PWM duty cycle is defined as a continuous high level if the PWM polarity is 1 and a continuous low level if the PWM polarity is 0. Conversely, a 0% PWM duty cycle is defined as a continuous low level if the PWM polarity is 1 and a continuous high level if the PWM polarity is 0.

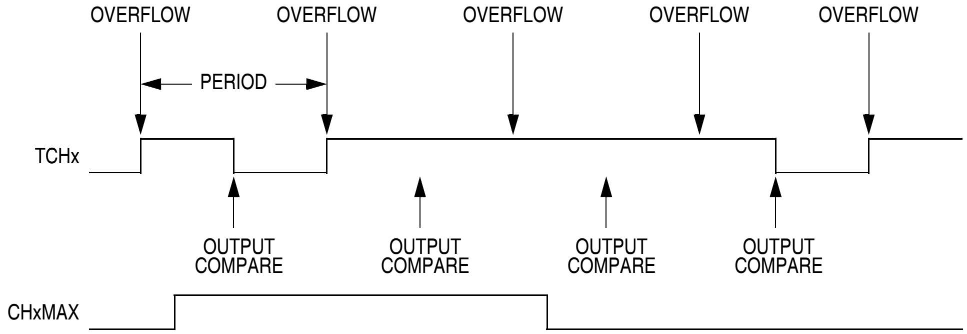


Figure 17-9. CHxMAX Latency

17.8.5 TIM1 Channel Registers

These read/write registers contain the captured TIM1 counter value of the input capture function or the output compare value of the output compare function. The state of the TIM1 channel registers after reset is unknown.

In input capture mode (MSxB:MSxA = 0:0), reading the high byte of the TIM1 channel x registers (T1CHxH) inhibits input captures until the low byte (T1CHxL) is read.

In output compare mode (MSxB:MSxA ≠ 0:0), writing to the high byte of the TIM1 channel x registers (T1CHxH) inhibits output compares until the low byte (T1CHxL) is written.

18.3.2 Input Capture

An input capture function has three basic parts: edge select logic, an input capture latch, and a 16-bit counter. Two 8-bit registers, which make up the 16-bit input capture register, are used to latch the value of the free-running counter after the corresponding input capture edge detector senses a defined transition. The polarity of the active edge is programmable. The level transition which triggers the counter transfer is defined by the corresponding input edge bits (ELSxB and ELSxA in T2SC0 through T2SC5 control registers with x referring to the active channel number). When an active edge occurs on the pin of an input capture channel, the TIM2 latches the contents of the TIM2 counter into the TIM2 channel registers, T2CHxH:T2CHxL. Input captures can generate TIM2 CPU interrupt requests. Software can determine that an input capture event has occurred by enabling input capture interrupts or by polling the status flag bit.

The free-running counter contents are transferred to the TIM2 channel registers (T2CHxH:T2CHxL) (see 18.8.5 TIM2 Channel Registers) on each proper signal transition regardless of whether the TIM2 channel flag (CH0F–CH5F in T2SC0–T2SC5 registers) is set or clear. When the status flag is set, a CPU interrupt is generated if enabled. The value of the count latched or “captured” is the time of the event. Because this value is stored in the input capture register when the actual event occurs, user software can respond to this event at a later time and determine the actual time of the event. However, this must be done prior to another input capture on the same pin; otherwise, the previous time value will be lost.

By recording the times for successive edges on an incoming signal, software can determine the period and/or pulse width of the signal. To measure a period, two successive edges of the same polarity are captured. To measure a pulse width, two alternate polarity edges are captured. Software should track the overflows at the 16-bit module counter to extend its range.

Another use for the input capture function is to establish a time reference. In this case, an input capture function is used in conjunction with an output compare function. For example, to activate an output signal a specified number of clock cycles after detecting an input event (edge), use the input capture function to record the time at which the edge occurred. A number corresponding to the desired delay is added to this captured value and stored to an output compare register (see 18.8.5 TIM2 Channel Registers). Because both input captures and output compares are referenced to the same 16-bit modulo counter, the delay can be controlled to the resolution of the counter independent of software latencies.

Reset does not affect the contents of the input capture channel (T2CHxH:T2CHxL) registers.

18.3.3 Output Compare

With the output compare function, the TIM2 can generate a periodic pulse with a programmable polarity, duration, and frequency. When the counter reaches the value in the registers of an output compare channel, the TIM2 can set, clear, or toggle the channel pin. Output compares can generate TIM2 CPU interrupt requests.

18.3.3.1 Unbuffered Output Compare

Any output compare channel can generate unbuffered output compare pulses as described in 18.3.3 Output Compare. The pulses are unbuffered because changing the output compare value requires writing the new value over the old value currently in the TIM2 channel registers.

An unsynchronized write to the TIM2 channel registers to change an output compare value could cause incorrect operation for up to two counter overflow periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that counter overflow period. Also, using a TIM2 overflow interrupt routine to write a new, smaller output

CHxMAX — Channel x Maximum Duty Cycle Bit

When the TOVx bit is at a 1 and clear output on compare is selected, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100%. As Figure 18-9 shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at 100% duty cycle level until the cycle after CHxMAX is cleared.

NOTE

The 100% PWM duty cycle is defined as a continuous high level if the PWM polarity is 1 and a continuous low level if the PWM polarity is 0. Conversely, a 0% PWM duty cycle is defined as a continuous low level if the PWM polarity is 1 and a continuous high level if the PWM polarity is 0.

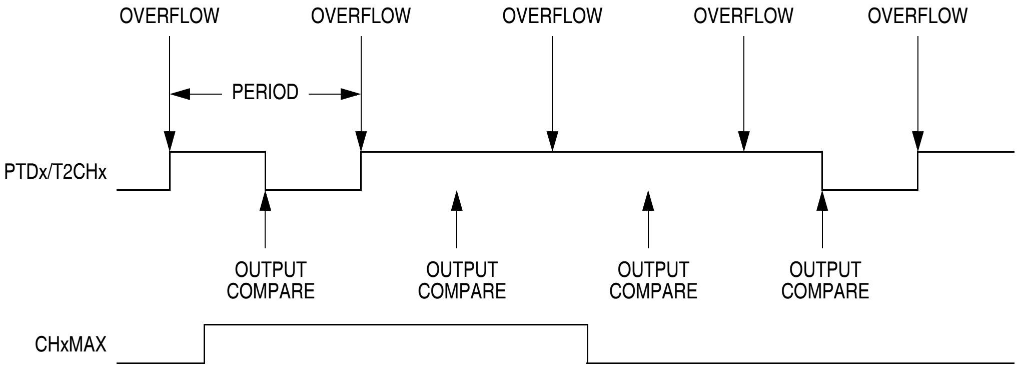


Figure 18-9. CHxMAX Latency

18.8.5 TIM2 Channel Registers

These read/write registers contain the captured TIM2 counter value of the input capture function or the output compare value of the output compare function. The state of the TIM2 channel registers after reset is unknown.

In input capture mode (MSxB:MSxA = 0:0), reading the high byte of the TIM2 channel x registers (T2CHxH) inhibits input captures until the low byte (T2CHxL) is read.

In output compare mode (MSxB:MSxA ≠ 0:0), writing to the high byte of the TIM2 channel x registers (T2CHxH) inhibits output compares until the low byte (T2CHxL) is written.

Address: $0031 T2CH0H

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	Indeterminate after reset							

Address: $0032 T2CH0L

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	Indeterminate after reset							

Figure 18-10. TIM2 Channel Registers (T2CH0H/L:T2CH5H/L) (Sheet 1 of 3)

19.3 Monitor Module (MON)

The monitor module allows debugging and programming of the microcontroller unit (MCU) through a single-wire interface with a host computer. Monitor mode entry can be achieved without use of the higher test voltage, V_{TST}, as long as vector addresses $FFFE and $FFFF are blank, thus reducing the hardware requirements for in-circuit programming.

Features of the monitor module include:

- Normal user-mode pin functionality
- One pin dedicated to serial communication between MCU and host computer
- Standard non-return-to-zero (NRZ) communication with host computer
- Standard communication baud rate (7200 @ 2-MHz bus frequency)
- Execution of code in random-access memory (RAM) or FLASH
- FLASH memory security feature[1]
- FLASH memory programming interface
- Monitor mode entry without high voltage, V_{TST}, if reset vector is blank ($FFFE and $FFFF contain $FF)
- Normal monitor mode entry if V_{TST} is applied to $\overline{\text{IRQ}}$

19.3.1 Functional Description

Figure 19-9 shows a simplified diagram of the monitor mode.

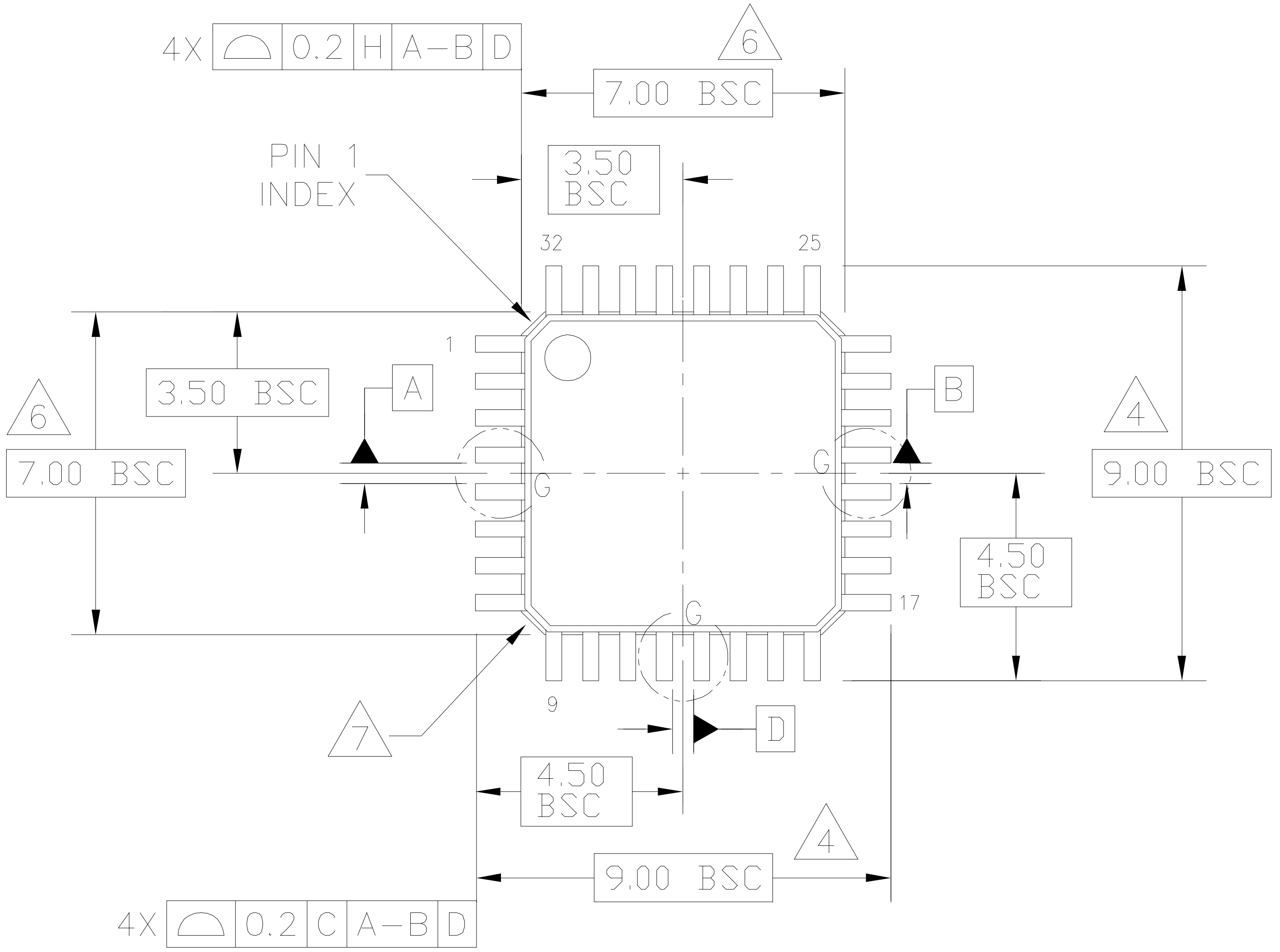
The monitor module receives and executes commands from a host computer.
Figure 19-10 and Figure 19-11 show example circuits used to enter monitor mode and communicate with a host computer via a standard RS-232 interface.

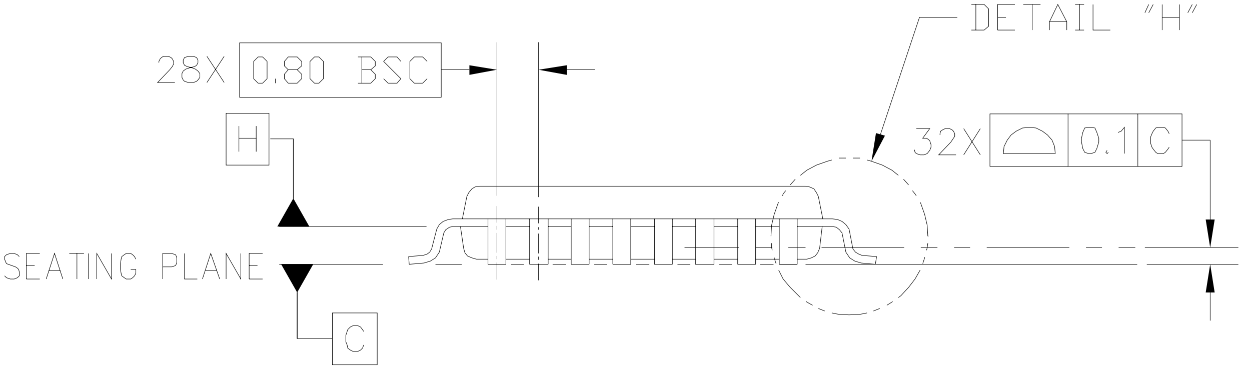
Simple monitor commands can access any memory address. In monitor mode, the MCU can execute code downloaded into RAM by a host computer while most MCU pins retain normal operating mode functions. All communication between the host computer and the MCU is through the PTA0 pin. A level-shifting and multiplexing interface is required between PTA0 and the host computer. PTA0 is used in a wired-OR configuration and requires a pullup resistor.

Table 19-1 shows the pin conditions for entering monitor mode. As specified in the table, monitor mode may be entered after a power-on reset (POR) and will allow communication at 7200 baud provided one of the following sets of conditions is met:

- If $FFFE and $FFFF does not contain $FF (programmed state):
  – The external clock is 4.0 MHz (7200 baud)
  – PTB4 = low
  – $\overline{\text{IRQ}} = V_{TST}$
- If $FFFE and $FFFF do not contain $FF (programmed state):
  – The external clock is 8.0 MHz (7200 baud)
  – PTB4 = high
  – IRQ = V_{TST}
- If $FFFE and $FFFF contain $FF (erased state):
  – The external clock is 8.0 MHz (7200 baud)
  – $\overline{\text{IRQ}} = V_{DD}$ (this can be implemented through the internal $\overline{\text{IRQ}}$ pullup) or V_{SS}

[1] No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.





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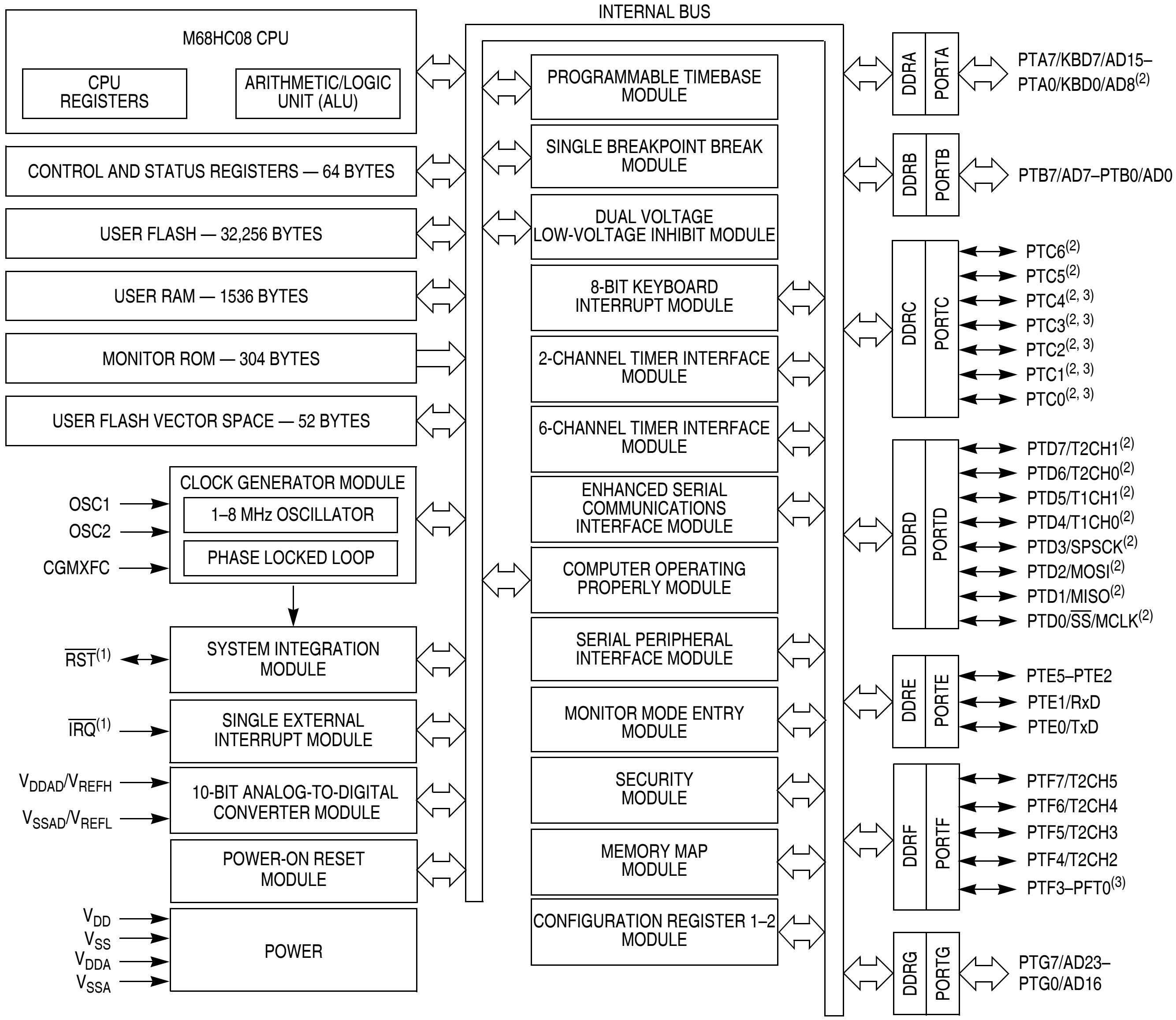
	CASE NUMBER: 873A-04	01 APR 2005
	STANDARD: JEDEC MS-026 BBA	


INTERNAL BUS
M68HC08 CPU
CPU REGISTERS
ARITHMETIC/LOGIC UNIT (ALU)
CONTROL AND STATUS REGISTERS — 64 BYTES
USER FLASH — 32,256 BYTES
USER RAM — 1536 BYTES
MONITOR ROM — 304 BYTES
USER FLASH VECTOR SPACE — 52 BYTES
CLOCK GENERATOR MODULE
1–8 MHz OSCILLATOR
PHASE LOCKED LOOP
OSC1
OSC2
CGMXFC
RST(1)
SYSTEM INTEGRATION MODULE
IRQ(1)
SINGLE EXTERNAL INTERRUPT MODULE
VDDAD/VREFH
VSSAD/VREFL
10-BIT ANALOG-TO-DIGITAL CONVERTER MODULE
POWER-ON RESET MODULE
VDD
VSS
VDDA
VSSA
POWER
PROGRAMMABLE TIMEBASE MODULE
SINGLE BREAKPOINT BREAK MODULE
DUAL VOLTAGE LOW-VOLTAGE INHIBIT MODULE
8-BIT KEYBOARD INTERRUPT MODULE
2-CHANNEL TIMER INTERFACE MODULE
6-CHANNEL TIMER INTERFACE MODULE
ENHANCED SERIAL COMMUNICATIONS INTERFACE MODULE
COMPUTER OPERATING PROPERLY MODULE
SERIAL PERIPHERAL INTERFACE MODULE
MONITOR MODE ENTRY MODULE
SECURITY MODULE
MEMORY MAP MODULE
CONFIGURATION REGISTER 1–2 MODULE
DDRA
PORTA
PTA7/KBD7/AD15–PTA0/KBD0/AD8(2)
DDRB
PORTB
PTB7/AD7–PTB0/AD0
DDRC
PORTC
PTC6(2)
PTC5(2)
PTC4(2, 3)
PTC3(2, 3)
PTC2(2, 3)
PTC1(2, 3)
PTC0(2, 3)
DDRD
PORTD
PTD7/T2CH1(2)
PTD6/T2CH0(2)
PTD5/T1CH1(2)
PTD4/T1CH0(2)
PTD3/SPSCK(2)
PTD2/MOSI(2)
PTD1/MISO(2)
PTD0/SS/MCLK(2)
DDRE
PORTE
PTE5–PTE2
PTE1/RxD
PTE0/TxD
DDRF
PORTF
PTF7/T2CH5
PTF6/T2CH4
PTF5/T2CH3
PTF4/T2CH2
PTF3–PFT0(3)
DDRG
PORTG
PTG7/AD23–PTG0/AD16

1. Pin contains integrated pullup device.
2. Ports are software configurable with pullup device if input port or pullup/pulldown device for keyboard input.
3. Higher current drive port pins

Figure B-1. MC68HC908GR32A Block Diagram