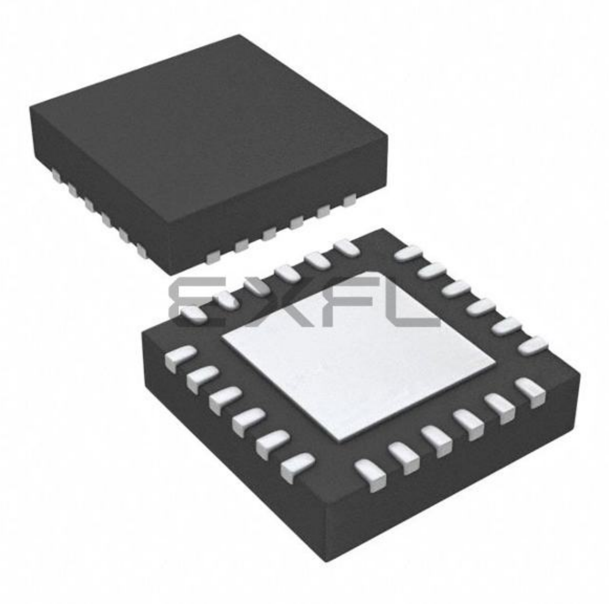


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 2x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VQFN Exposed Pad
Supplier Device Package	24-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg110f16-qfn24

3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on T_{AMB}=25°C and V_{DD}=3.0 V, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 9) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 9) .

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150[1]	°C
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		V_{DD}+0.3	V

[1]Based on programmed devices tested for 10000 hours at 150°C. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	°C
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			32	MHz
f_{AHB}	Internal AHB clock frequency			32	MHz

Figure 3.1. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.

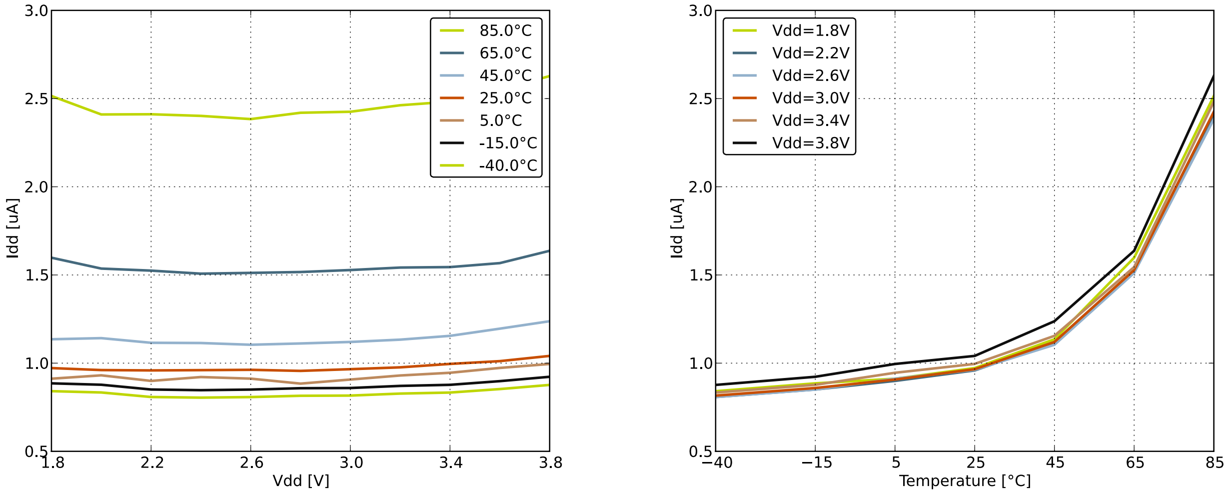


Figure 3.2. EM3 current consumption.

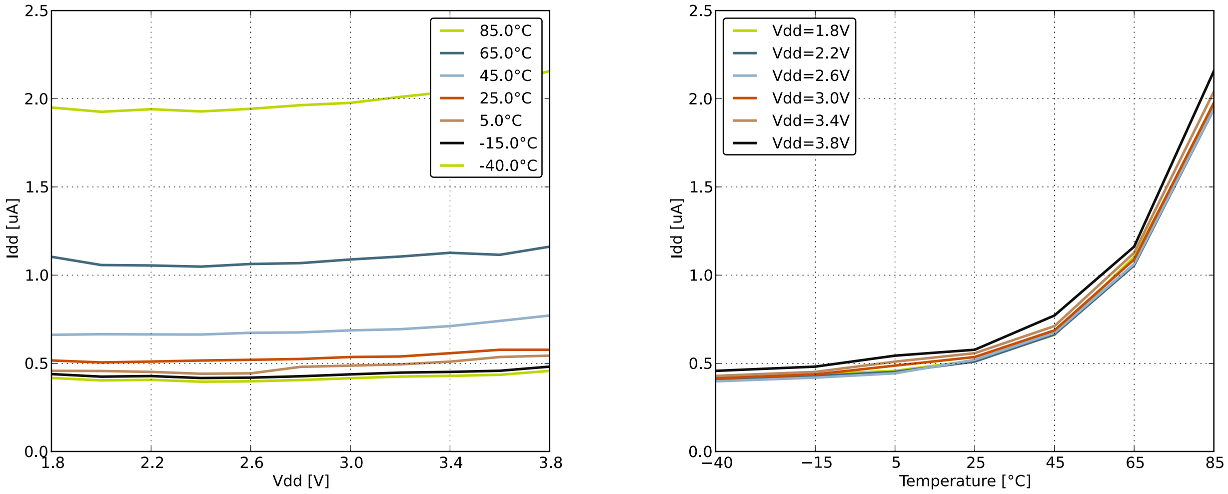


Figure 3.3. EM4 current consumption.

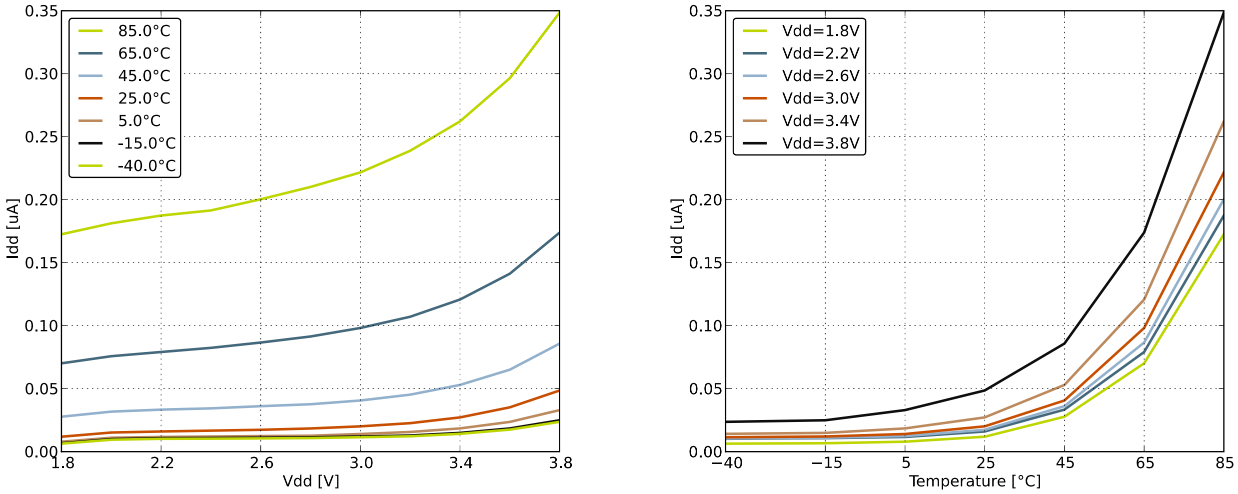
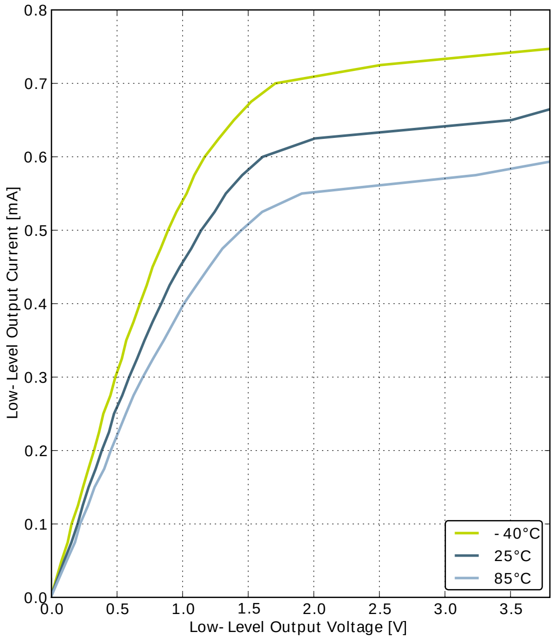
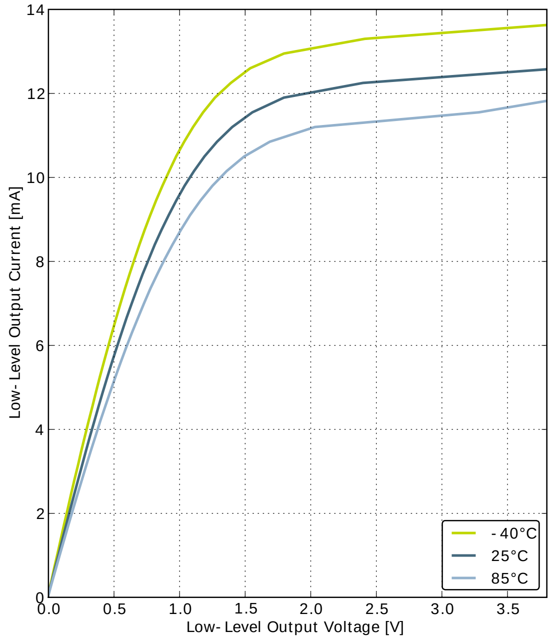


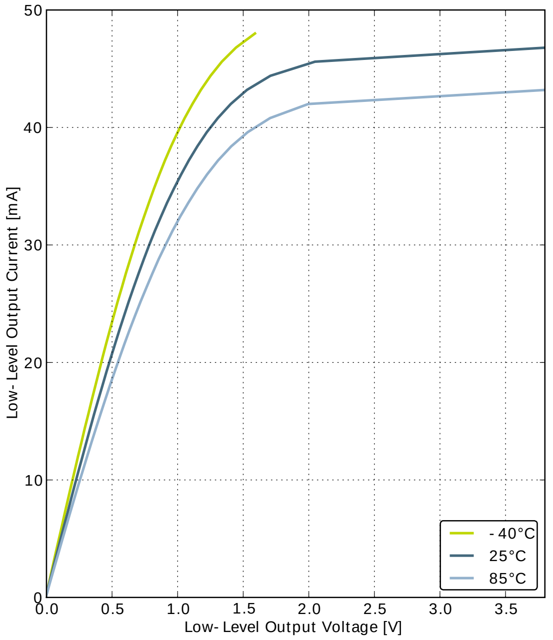
Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage



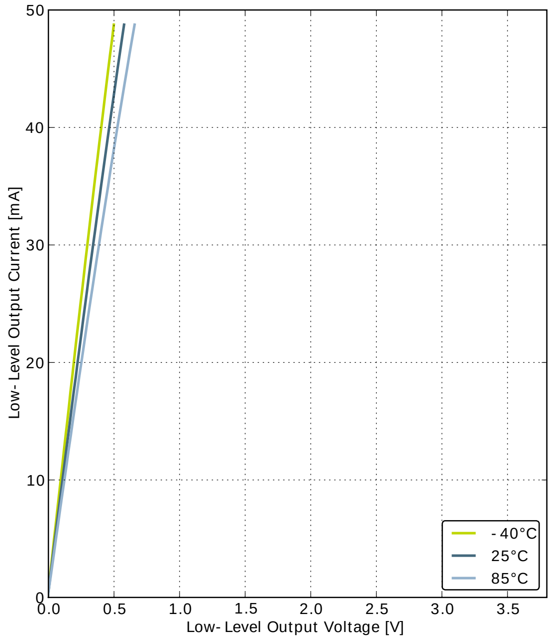
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

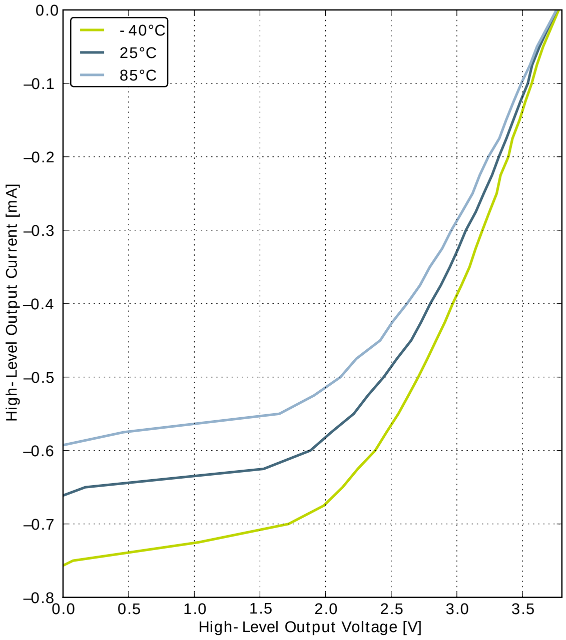


GPIO_Px_CTRL DRIVEMODE = STANDARD

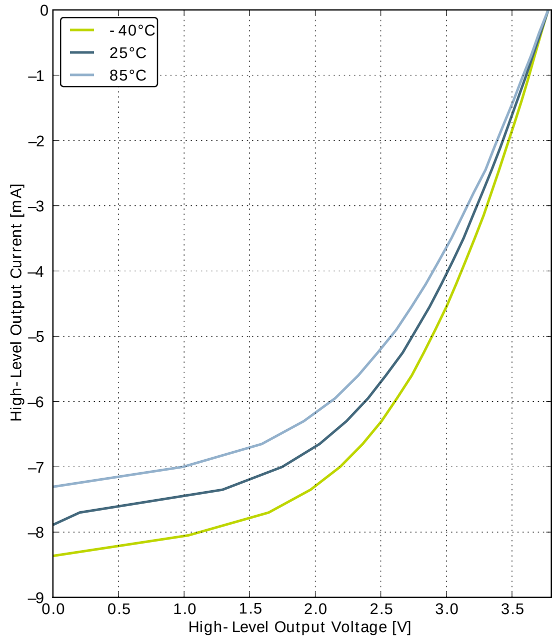


GPIO_Px_CTRL DRIVEMODE = HIGH

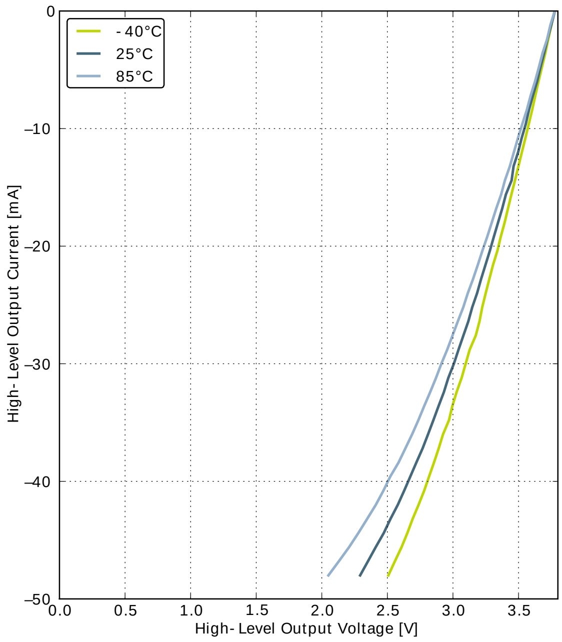
Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage



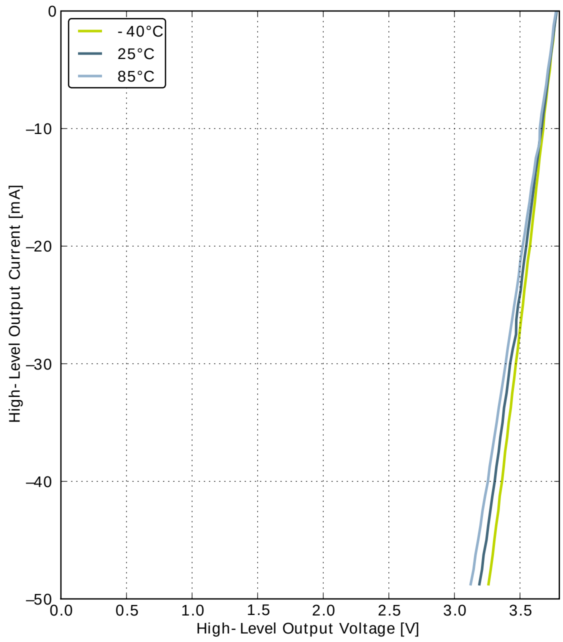
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		f_{HFRCO} = 14 MHz		104	120	µA
		f_{HFRCO} = 11 MHz		94	110	µA
		f_{HFRCO} = 6.6 MHz		63	90	µA
		f_{HFRCO} = 1.2 MHz		22	32	µA
$TUNESTEP_{HFRCO}$	Frequency step for LSB change in TUNING value			0.3[3]		%

[1]For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

[2]For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

[3]The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

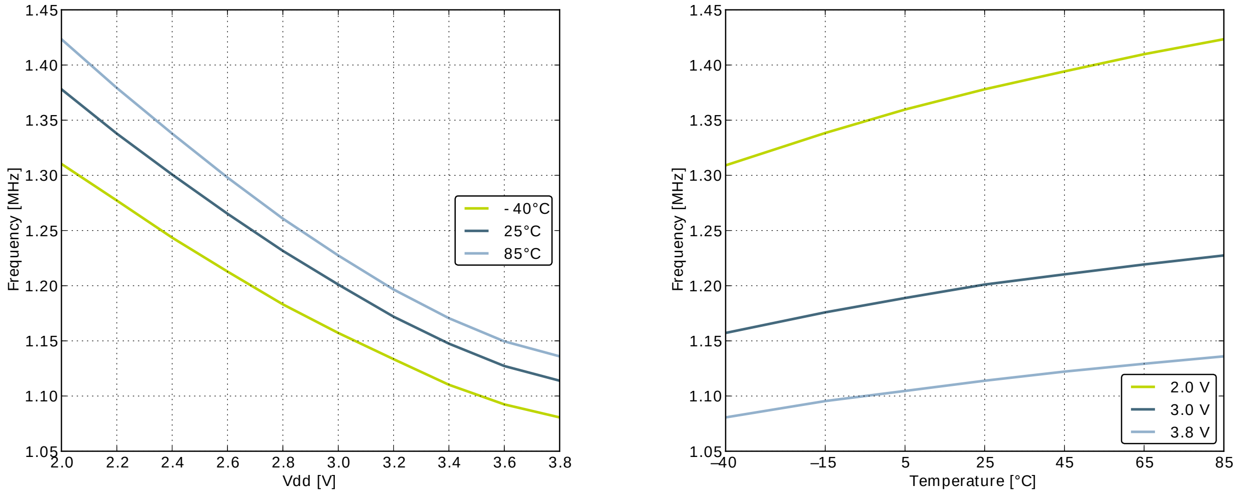


Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

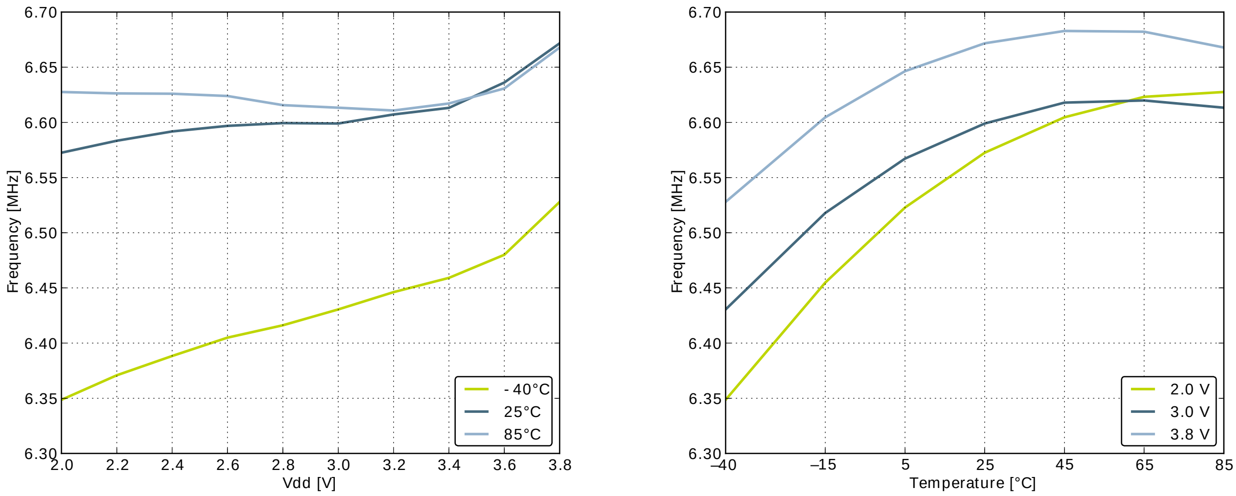


Figure 3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

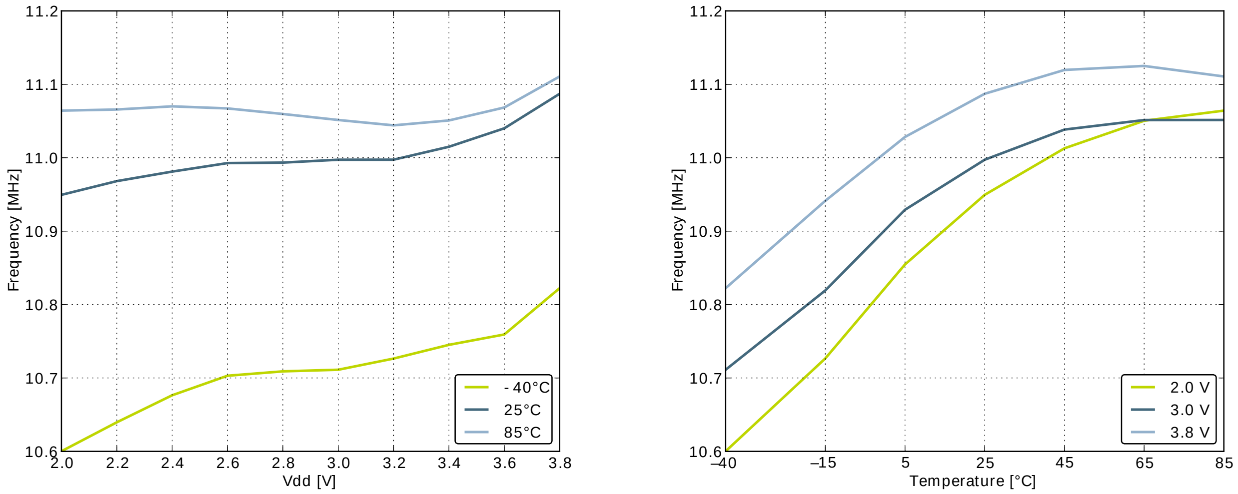


Figure 3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

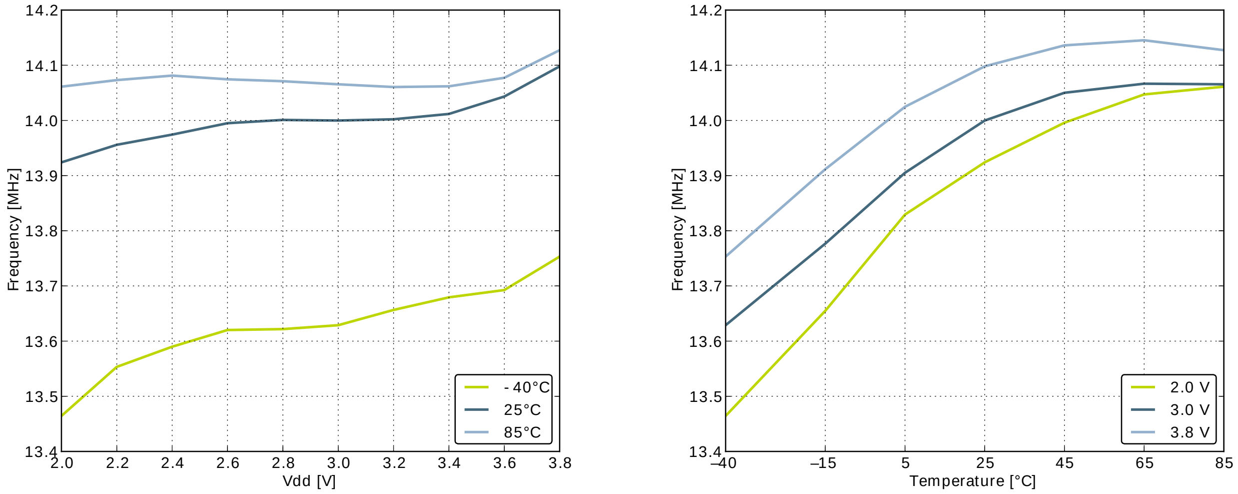
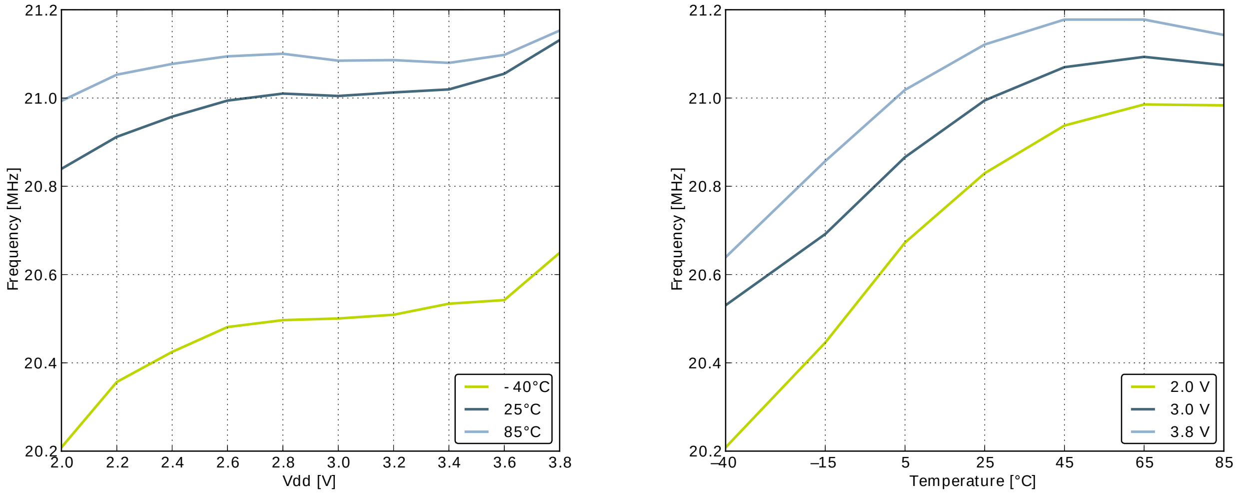


Figure 3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

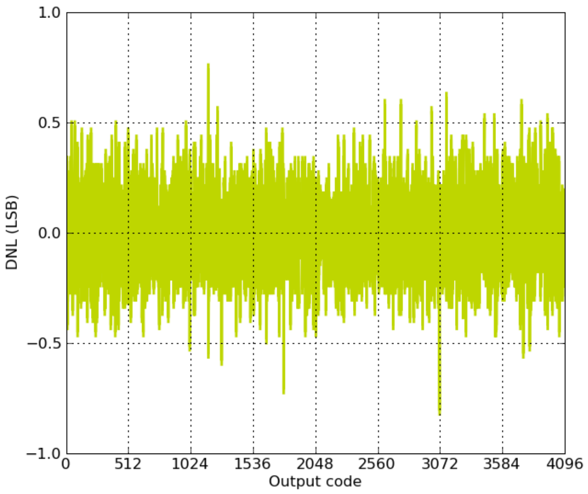


Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ADCCLK}	ADC Clock Frequency				13	MHz
$t_{ADCCONV}$	Conversion time	6 bit	7			ADC-CLK Cycles
		8 bit	11			ADC-CLK Cycles
		12 bit	13			ADC-CLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1		256	ADC-CLK Cycles
$t_{ADCACQVDD3}$	Required acquisition time for VDD/3 reference		2			µs
$t_{ADCSTART}$	Startup time of reference generator and ADC core in NORMAL mode			5		µs
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		µs
SNR_{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		69		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V_{DD} reference	63	67		dB

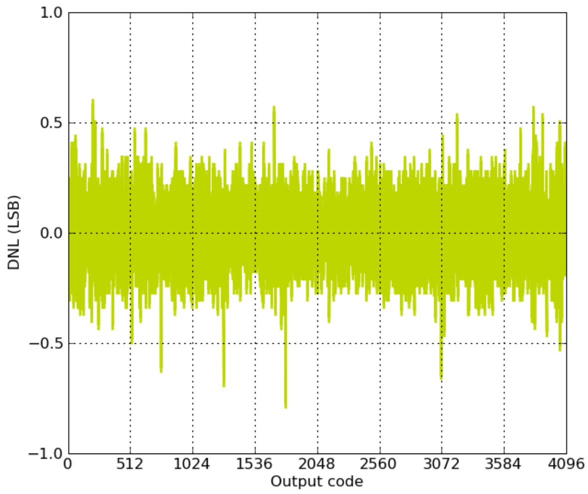
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		1 MSamples/s, 12 bit, single ended, V_{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		77		dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference		75		dBc
		1 MSamples/s, 12 bit, differential, 5V reference		69		dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V_{DD} reference	68	76		dBc
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V_{DD} reference		79		dBc
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference		79		dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single ended	-4	0.3	4	mV
		After calibration, differential		0.3		mV
$TGRAD_{ADCTH}$	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/°C
DNL_{ADC}	Differential non-linearity (DNL)	V_{DD}= 3.0 V, external 2.5V reference	-1	±0.7	4	LSB
INL_{ADC}	Integral non-linearity (INL), End point method	V_{DD}= 3.0 V, external 2.5V reference		±1.2	±3	LSB
MC_{ADC}	No missing codes		11.999[1]	12		bits
$GAIN_{ED}$	Gain error drift	1.25V reference		0.01[2]	0.033[3]	%/°C
		2.5V reference		0.01[2]	0.03[3]	%/°C
$OFFSET_{ED}$	Offset error drift	1.25V reference		0.2[2]	0.7[3]	LSB/°C
		2.5V reference		0.2[2]	0.62[3]	LSB/°C

[1]On the average every ADC will have one missing code, most likely to appear around 2048 ± n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic

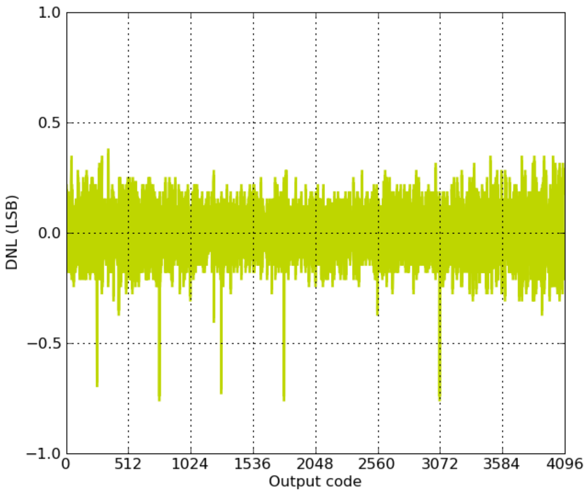
Figure 3.21. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C



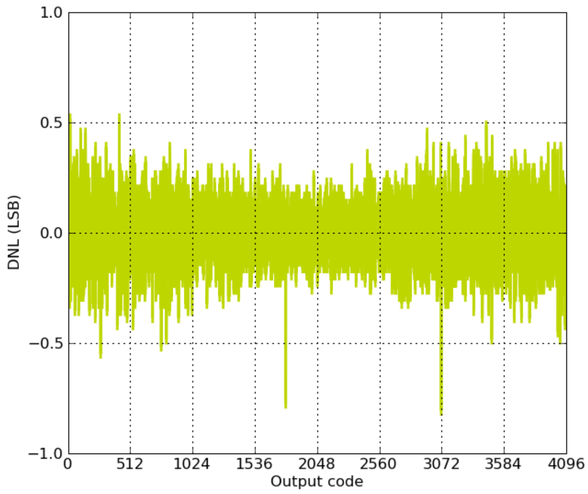
1.25V Reference



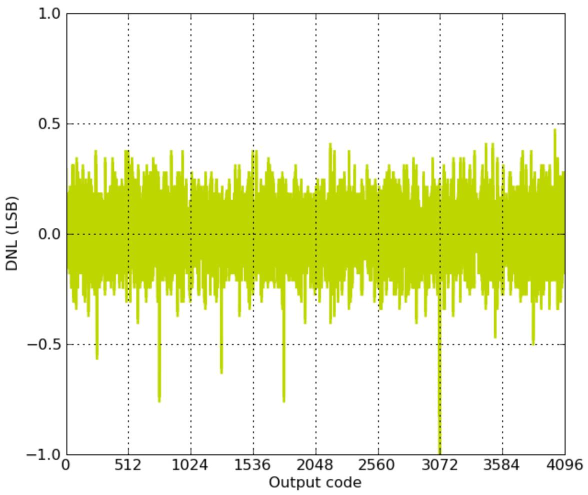
2.5V Reference



2XVDDVSS Reference



5VDIFF Reference



VDD Reference

Figure 3.25. OPAMP Positive Power Supply Rejection Ratio

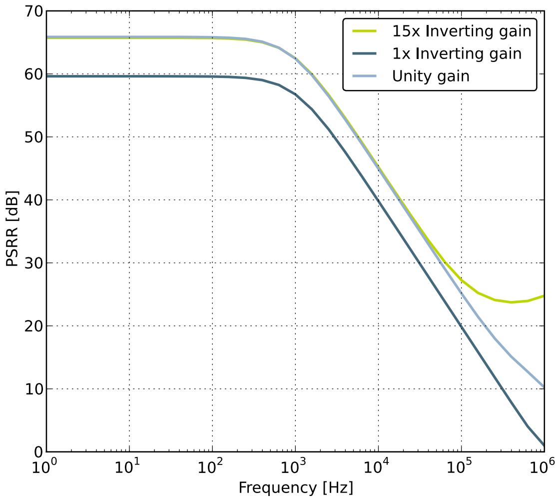


Figure 3.26. OPAMP Negative Power Supply Rejection Ratio

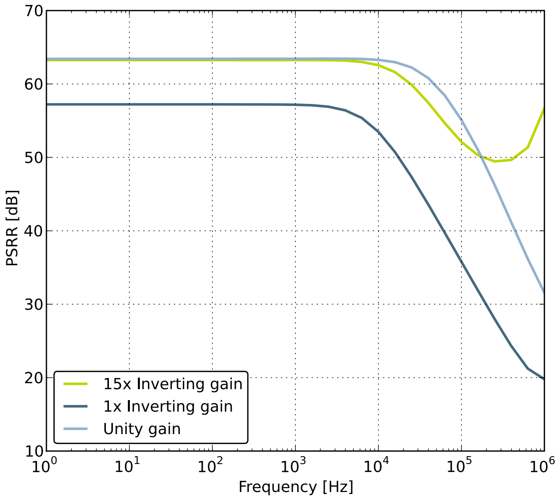


Figure 3.27. OPAMP Voltage Noise Spectral Density (Unity Gain) V_{out}=1V

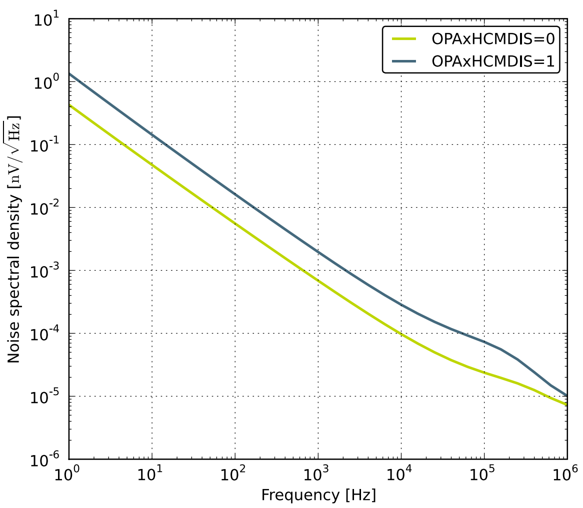
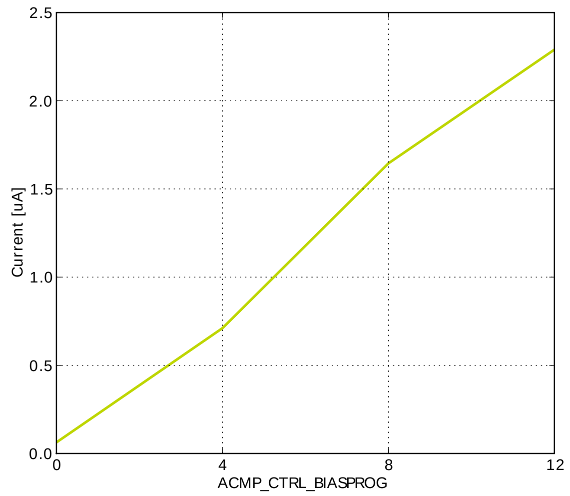
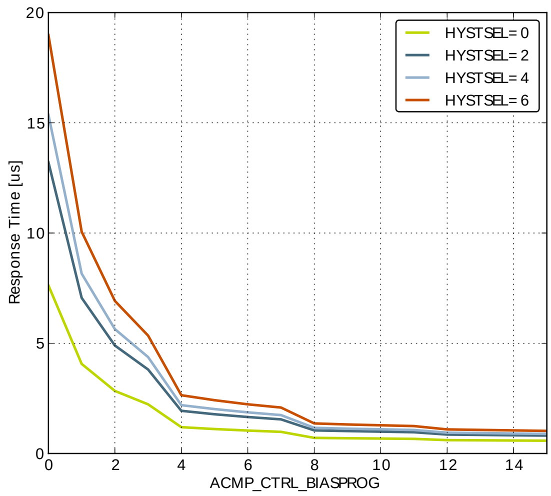


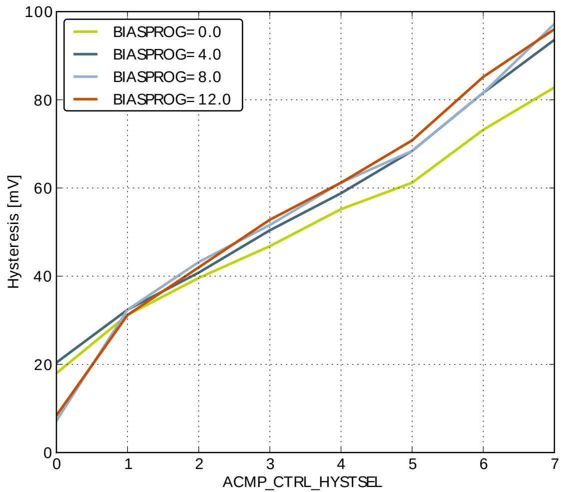
Figure 3.29. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time , V_{cm} = 1.25V, CP+ to CP- = 100mV



Hysteresis

Table 3.20. I2C Fast-mode (Fm)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		400[1]	kHz
t_{LOW}	SCL clock low time	1.3			µs
t_{HIGH}	SCL clock high time	0.6			µs
$t_{SU,DAT}$	SDA set-up time	100			ns
$t_{HD,DAT}$	SDA hold time	8		900[2,3]	ns
$t_{SU,STA}$	Repeated START condition set-up time	0.6			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.6			µs
$t_{SU,STO}$	STOP condition set-up time	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32TG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 3.21. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000[1]	kHz
t_{LOW}	SCL clock low time	0.5			µs
t_{HIGH}	SCL clock high time	0.26			µs
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			µs
$t_{SU,STO}$	STOP condition set-up time	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32TG Reference Manual.

3.16 Digital Peripherals

Table 3.22. Digital Peripherals

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{USART}	USART current	USART idle current, clock enabled		7.5		µA/MHz
I_{LEUART}	LEUART current	LEUART idle current, clock enabled		150		nA
I_{I2C}	I2C current	I2C idle current, clock enabled		6.25		µA/MHz
I_{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		8.75		µA/MHz
$I_{LETIMER}$	LETIMER current	LETIMER idle current, clock enabled		75		nA
I_{PCNT}	PCNT current	PCNT idle current, clock enabled		60		nA

4 Pinout and Package

Note

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32TG110.

4.1 Pinout

The *EFM32TG110* pinout is shown in Figure 4.1 (p. 45) and Table 4.1 (p. 45). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

Figure 4.1. EFM32TG110 Pinout (top view, not to scale)

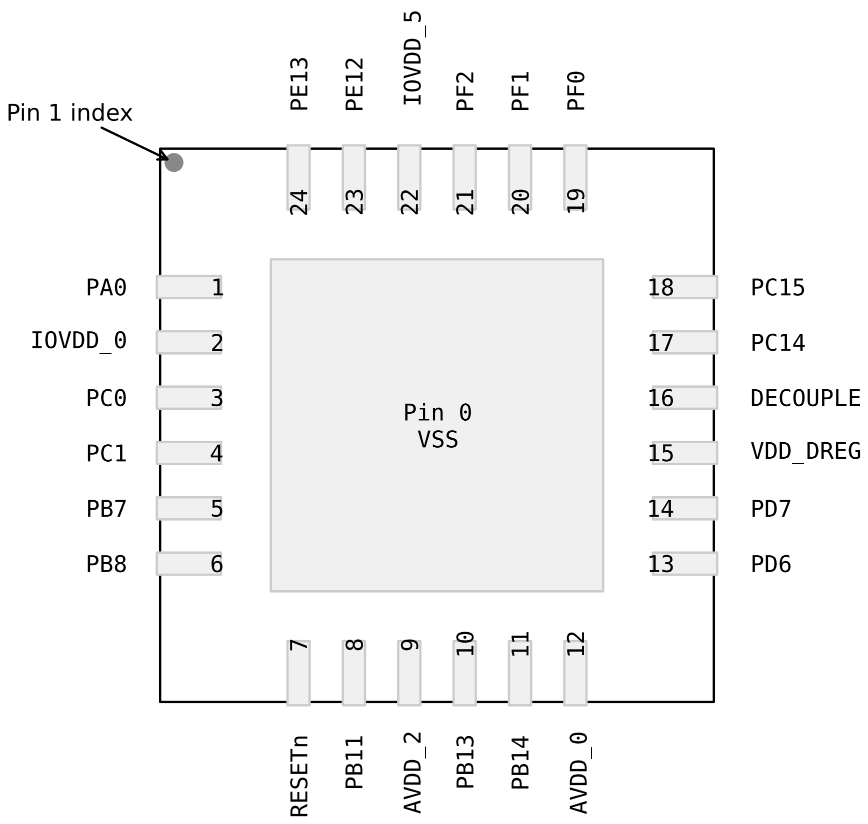


Table 4.1. Device Pinout

QFN24 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	IOVDD_0	Digital IO power supply 0.			

QFN24 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
3	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
4	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
5	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
6	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
7	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
8	PB11	DAC0_OUT0 / OPAMP_OUT0	TIM1_CC2 #3 LETIM0_OUT0 #1		
9	AVDD_2	Analog power supply 2.			
10	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
11	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
12	AVDD_0	Analog power supply 0.			
13	PD6	ADC0_CH6 DAC0_P1 / OPAMP_P1	TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2
14	PD7	ADC0_CH7 DAC0_N1 / OPAMP_N1	TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2
15	VDD_DREG	Power supply for on-chip voltage regulator.			
16	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
17	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT	TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3	LES_CH14 #0
18	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT	TIM1_CC2 #0	US0_CLK #3	LES_CH15 #0 DBG_SWO #1
19	PF0		TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1 BOOT_TX
20	PF1		TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1 GPIO_EM4WU3 BOOT_RX
21	PF2		TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
22	IOVDD_5	Digital IO power supply 5.			
23	PE12		TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
24	PE13			US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5

4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 47). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 4.2. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PF1							Bootloader RX.
BOOT_TX	PF0							Bootloader TX.
CMU_CLK0			PD7					Clock Management Unit, clock output number 0.
CMU_CLK1			PE12					Clock Management Unit, clock output number 1.
DAC0_N1 / OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT	PC0	PC1						Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1ALT / OPAMP_OUT1ALT			PC14	PC15				Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
DAC0_P1 / OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
DBG_SWCLK	PF0	PF0						Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1						Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15						Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
US1_TX	PC0		PD7					USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32TG110* is shown in Table 4.3 (p. 49). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 4.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	-	-	-	-	-	-	-	-	-	-	-	-	PC1	PC0
Port D	-	-	-	-	-	-	-	-	PD7	PD6	-	-	-	-	-	-
Port E	-	-	PE13	PE12	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	-	PF2	PF1	PF0

4.4 Opamp Pinout Overview

The specific opamp terminals available in *EFM32TG110* is shown in Figure 4.2 (p. 49) .

Figure 4.2. Opamp Pinout

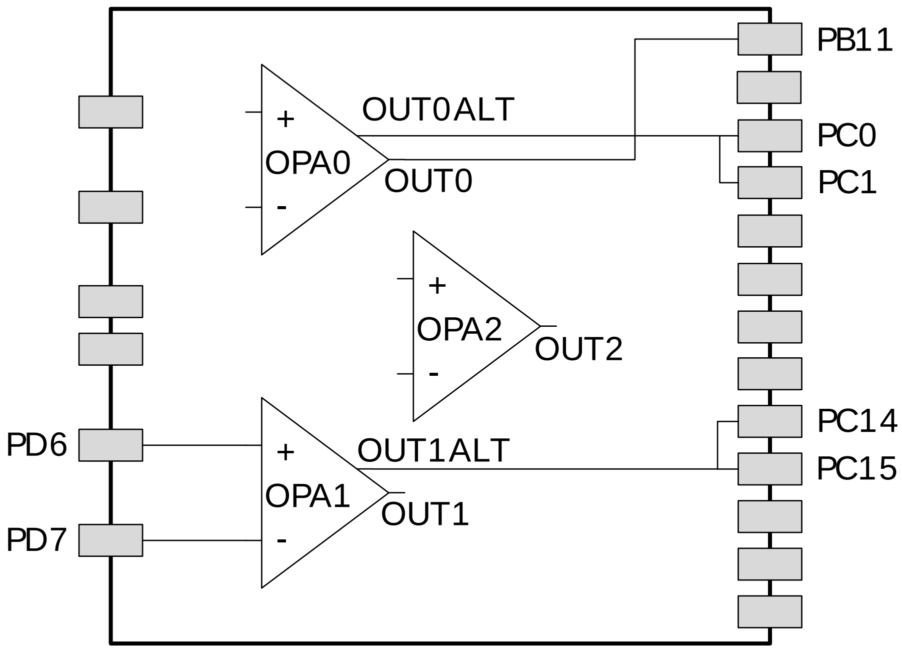


Figure 5.2. QFN24 PCB Solder Mask

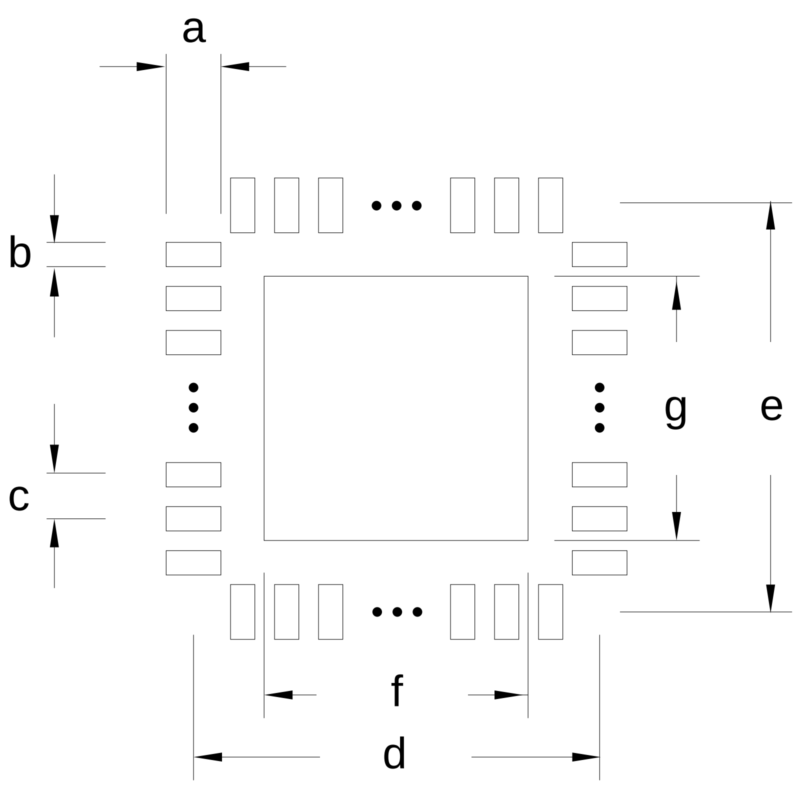


Table 5.2. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.92	e	5.00
b	0.42	f	3.72
c	0.65	g	3.72
d	5.00	-	-

Figure 5.3. QFN24 PCB Stencil Design

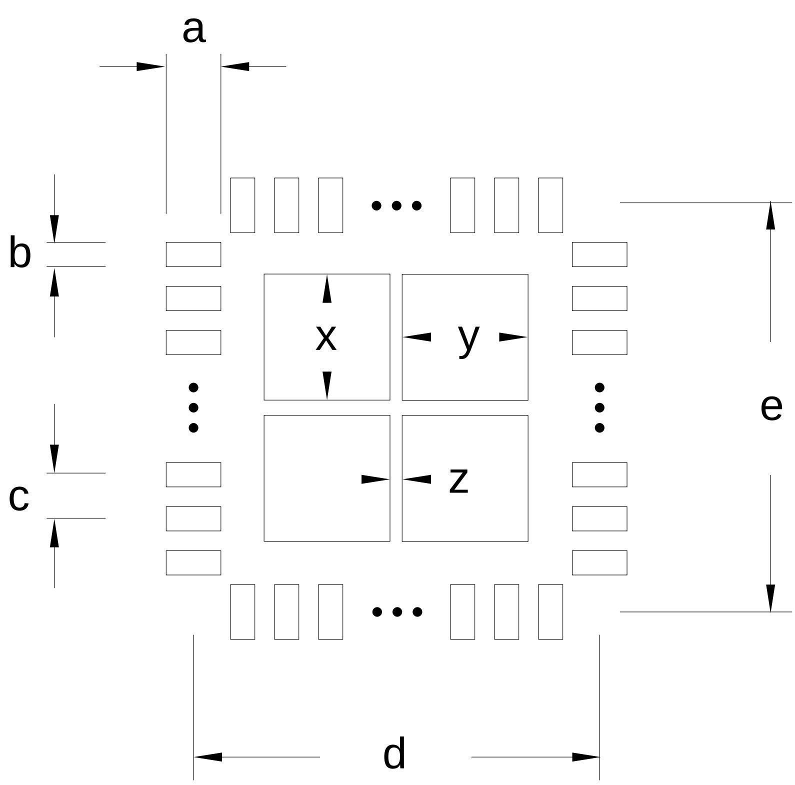


Table 5.3. QFN24 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.60	e	5.00
b	0.25	x	1.00
c	0.65	y	1.00
d	5.00	z	0.50

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.3 (p. 50) .

5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions. Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

List of Figures

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ZERO
ARM Cortex-M0+

TINY
ARM Cortex-M3

GECKO
ARM Cortex-M3

LEOPARD
ARM Cortex-M3

GIANT
ARM Cortex-M3

WONDER
ARM Cortex-M4