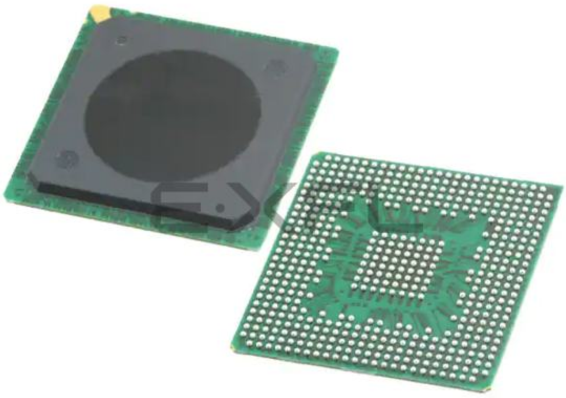

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8321cvraddc

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 6. Estimated Typical I/O Power Dissipation (continued)

Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 32 bits	—	—	0.12	W	—
PCI I/O load = 30 pF	66 MHz, 32 bits	—	—	0.057	W	—
QUICC Engine block and other I/Os	UTOPIA 8-bit 31 PHYs	—	—	0.041	W	Multiply by number of interfaces used.
	TDM serial	—	—	0.001	W	
	TDM nibble	—	—	0.004	W	
	HDLC/TRAN serial	—	—	0.003	W	
	HDLC/TRAN nibble	—	—	0.025	W	
	DUART	—	—	0.017	W	
	MIIs	—	—	0.009	W	
	RMII	—	—	0.009	W	
	Ethernet management	—	—	0.002	W	
	USB	—	—	0.001	W	
	SPI	—	—	0.001	W	
	Timer output	—	—	0.002	W	

NOTE

$AV_{DD}n$ (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of $\overline{\text{CFG\_CLKIN\_DIV}}$. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—

Table 11. Reset Signals DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input current	I_{IN}	$0\ V \le V_{IN} \le OV_{DD}$	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3 V supply.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR1 and DDR2 SDRAM interface of the MPC8323E. Note that DDR1 SDRAM is Dn_GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is Dn_GV_{DD}(typ) = 1.8 V. The AC electrical specifications are the same for DDR1 and DDR2 SDRAM.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8323E when Dn_GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for Dn_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	Dn_GV_{DD}	1.71	1.89	V	1
I/O reference voltage	$MVREFn_{REF}$	$0.49 \times Dn\_GV_{DD}$	$0.51 \times Dn\_GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MVREFn_{REF} - 0.04$	$MVREFn_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MVREFn_{REF} + 0.125$	$Dn\_GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MVREFn_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.35 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.
2. $MVREFn_{REF}$ is expected to be equal to $0.5 \times Dn\_GV_{DD}$, and to track Dn_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MVREFn_{REF}$ may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to $MVREFn_{REF}$. This rail should track variations in the DC level of $MVREFn_{REF}$.
4. Output leakage is measured with all outputs disabled, $0\ V \le V_{OUT} \le Dn\_GV_{DD}$.

Table 13 provides the DDR2 capacitance when Dn_GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for Dn_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1

Figure 4 shows the input timing diagram for the DDR controller.

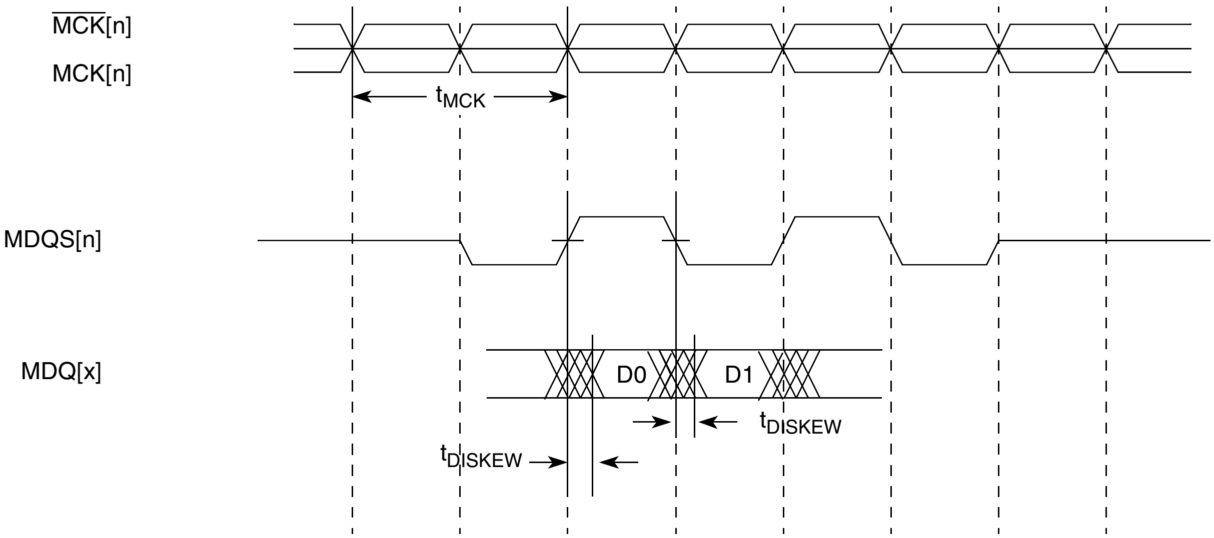

Figure 4. DDR Input Timing Diagram

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

Table 19 provides the output AC timing specifications for the DDR1 and DDR2 SDRAM interfaces.

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with D*n*_GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK cycle time, (MCK/$\overline{\text{MCK}}$ crossing)	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.5 3.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHAX}	 2.5 3.5	 — —	ns	3
$\overline{\text{MCS}}$ output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 2.5 3.5	 — —	ns	3
$\overline{\text{MCS}}$ output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 2.5 3.5	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with D*n*_GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.9 1.0	 — —	ns	5
MDQ/MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100 1200	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

8.2.2.1 RMII Transmit AC Timing Specifications

Table 23 provides the RMII transmit AC timing specifications.

Table 25. RMII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the RMII transmit AC timing diagram.

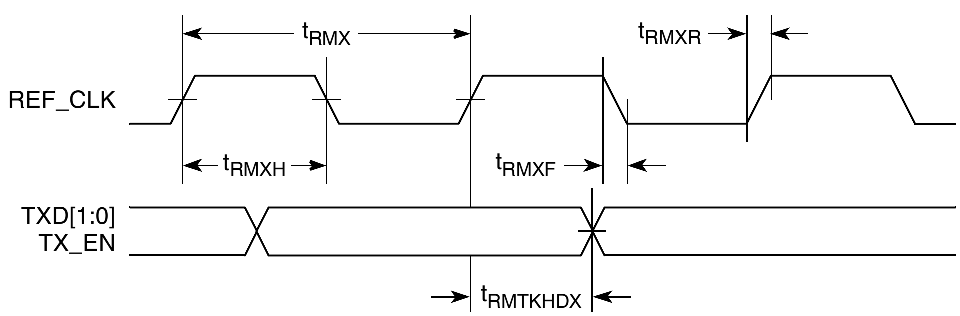

Figure 10. RMII Transmit AC Timing Diagram

8.2.2.2 RMII Receive AC Timing Specifications

Table 24 provides the RMII receive AC timing specifications.

Table 26. RMII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns

Table 26. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load.

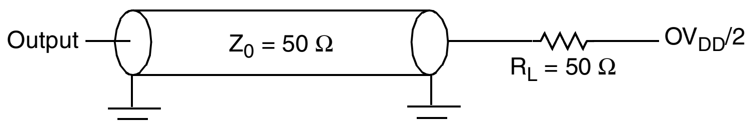

Figure 11. AC Test Load

Figure 12 shows the RMII receive AC timing diagram.

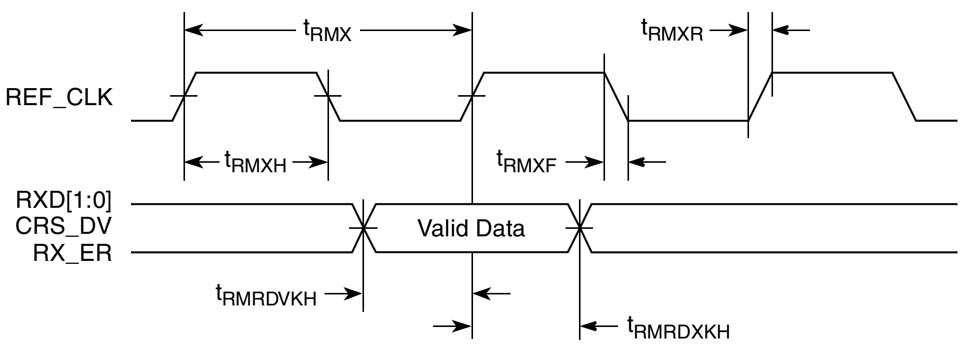

Figure 12. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, “Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics.”

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.10	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII Management AC Electrical Specifications

Table 28 provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 15 through Figure 17 show the local bus signals.

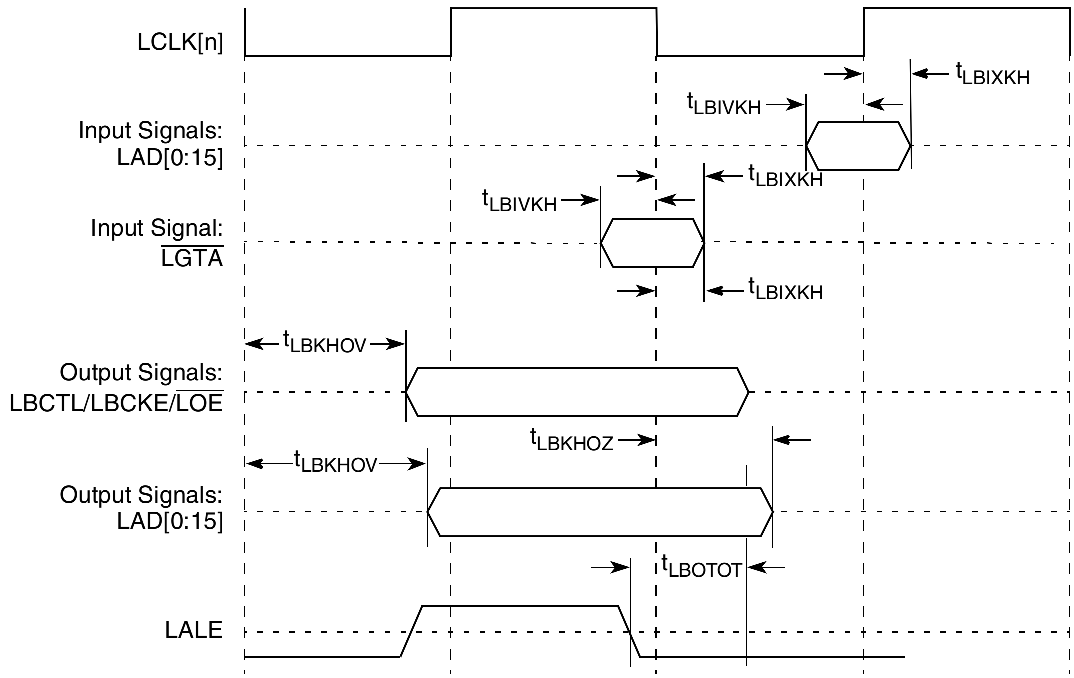

Figure 15. Local Bus Signals, Nonspecial Signals Only

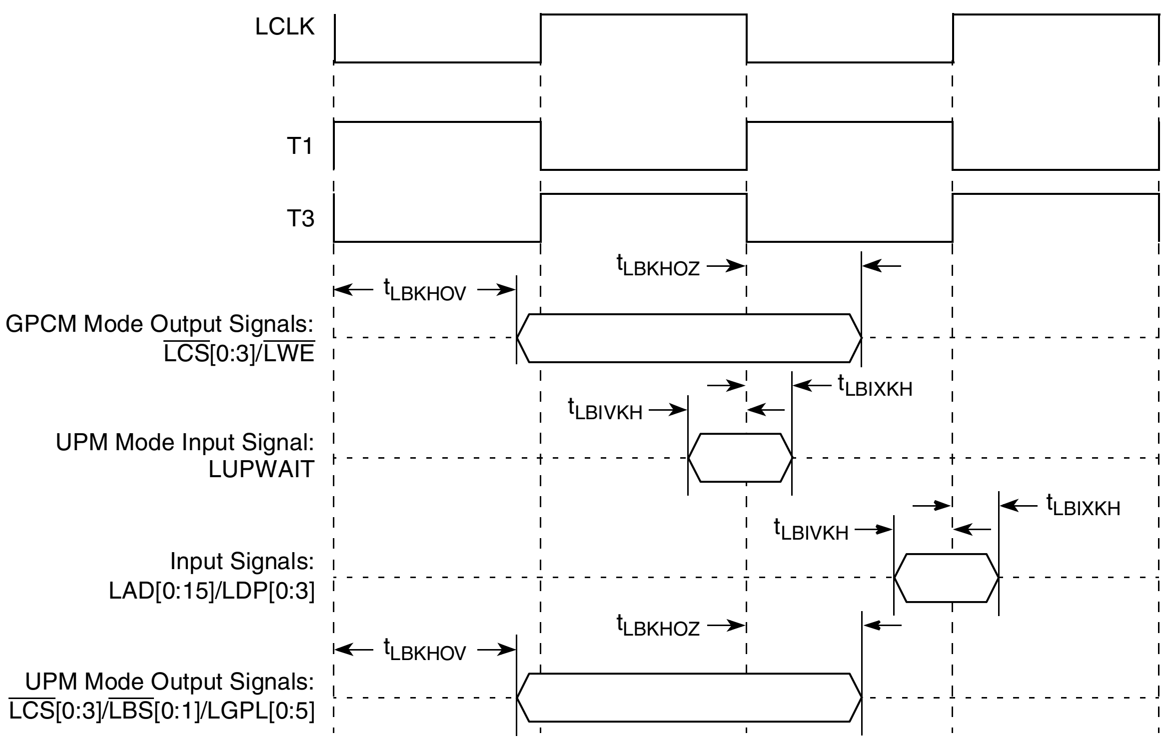

Figure 16. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

Table 37 shows the PCI AC timing specifications at 33 MHz.

Table 37. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedence	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 25 provides the AC test load for PCI.

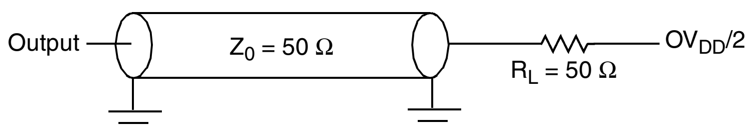

Figure 25. PCI AC Test Load

Figure 26 shows the PCI input AC timing conditions.

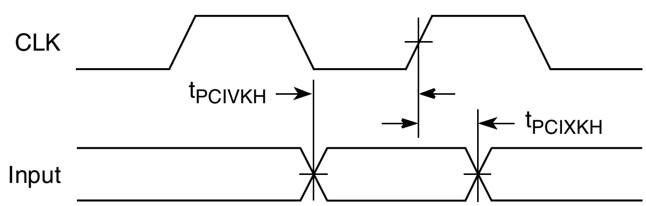

Figure 26. PCI Input AC Timing Measurement Conditions

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 52. Synchronous UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	5.5	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	10	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	5.5	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	8	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	4	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	0	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{UAIKHOX}$ symbolizes the outputs internal timing (UAI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 38 provides the AC test load.

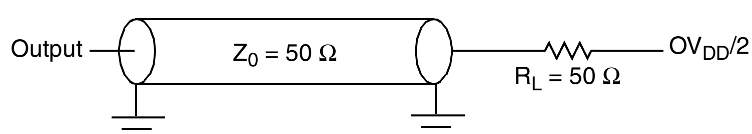

Figure 38. AC Test Load

Figure 39 and Figure 40 represent the AC timing from Table 51. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

Table 55. MPC8323E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	AE9	IO	GV_{DD}	—
MEMC_MDQ1	AD10	IO	GV_{DD}	—
MEMC_MDQ2	AF10	IO	GV_{DD}	—
MEMC_MDQ3	AF9	IO	GV_{DD}	—
MEMC_MDQ4	AF7	IO	GV_{DD}	—
MEMC_MDQ5	AE10	IO	GV_{DD}	—
MEMC_MDQ6	AD9	IO	GV_{DD}	—
MEMC_MDQ7	AF8	IO	GV_{DD}	—
MEMC_MDQ8	AE6	IO	GV_{DD}	—
MEMC_MDQ9	AD7	IO	GV_{DD}	—
MEMC_MDQ10	AF6	IO	GV_{DD}	—
MEMC_MDQ11	AC7	IO	GV_{DD}	—
MEMC_MDQ12	AD8	IO	GV_{DD}	—
MEMC_MDQ13	AE7	IO	GV_{DD}	—
MEMC_MDQ14	AD6	IO	GV_{DD}	—
MEMC_MDQ15	AF5	IO	GV_{DD}	—
MEMC_MDQ16	AD18	IO	GV_{DD}	—
MEMC_MDQ17	AE19	IO	GV_{DD}	—
MEMC_MDQ18	AF17	IO	GV_{DD}	—
MEMC_MDQ19	AF19	IO	GV_{DD}	—
MEMC_MDQ20	AF18	IO	GV_{DD}	—
MEMC_MDQ21	AE18	IO	GV_{DD}	—
MEMC_MDQ22	AF20	IO	GV_{DD}	—
MEMC_MDQ23	AD19	IO	GV_{DD}	—
MEMC_MDQ24	AD21	IO	GV_{DD}	—
MEMC_MDQ25	AF22	IO	GV_{DD}	—
MEMC_MDQ26	AC21	IO	GV_{DD}	—
MEMC_MDQ27	AF21	IO	GV_{DD}	—
MEMC_MDQ28	AE21	IO	GV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MDQ29	AD20	IO	GV_{DD}	—
MEMC_MDQ30	AF23	IO	GV_{DD}	—
MEMC_MDQ31	AD22	IO	GV_{DD}	—
MEMC_MDM0	AC9	O	GV_{DD}	—
MEMC_MDM1	AD5	O	GV_{DD}	—
MEMC_MDM2	AE20	O	GV_{DD}	—
MEMC_MDM3	AE22	O	GV_{DD}	—
MEMC_MDQS0	AE8	IO	GV_{DD}	—
MEMC_MDQS1	AE5	IO	GV_{DD}	—
MEMC_MDQS2	AC19	IO	GV_{DD}	—
MEMC_MDQS3	AE23	IO	GV_{DD}	—
MEMC_MBA0	AD16	O	GV_{DD}	—
MEMC_MBA1	AD17	O	GV_{DD}	—
MEMC_MBA2	AE17	O	GV_{DD}	—
MEMC_MA0	AD12	O	GV_{DD}	—
MEMC_MA1	AE12	O	GV_{DD}	—
MEMC_MA2	AF12	O	GV_{DD}	—
MEMC_MA3	AC13	O	GV_{DD}	—
MEMC_MA4	AD13	O	GV_{DD}	—
MEMC_MA5	AE13	O	GV_{DD}	—
MEMC_MA6	AF13	O	GV_{DD}	—
MEMC_MA7	AC15	O	GV_{DD}	—
MEMC_MA8	AD15	O	GV_{DD}	—
MEMC_MA9	AE15	O	GV_{DD}	—
MEMC_MA10	AF15	O	GV_{DD}	—
MEMC_MA11	AE16	O	GV_{DD}	—
MEMC_MA12	AF16	O	GV_{DD}	—
MEMC_MA13	AB16	O	GV_{DD}	—
$\overline{\text{MEMC\_MWE}}$	AC17	O	GV_{DD}	—
$\overline{\text{MEMC\_MRAS}}$	AE11	O	GV_{DD}	—
$\overline{\text{MEMC\_MCAS}}$	AD11	O	GV_{DD}	—
$\overline{\text{MEMC\_MCS}}$	AC11	O	GV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	O	GV_{DD}	3
MEMC_MCK	AF14	O	GV_{DD}	—
$\overline{\text{MEMC\_MCK}}$	AE14	O	GV_{DD}	—
MEMC_MODT	AF11	O	GV_{DD}	—
Local Bus Controller Interface				
LAD0	N25	IO	OV_{DD}	7
LAD1	P26	IO	OV_{DD}	7
LAD2	P25	IO	OV_{DD}	7
LAD3	R26	IO	OV_{DD}	7
LAD4	R25	IO	OV_{DD}	7
LAD5	T26	IO	OV_{DD}	7
LAD6	T25	IO	OV_{DD}	7
LAD7	U25	IO	OV_{DD}	7
LAD8	M24	IO	OV_{DD}	7
LAD9	N24	IO	OV_{DD}	7
LAD10	P24	IO	OV_{DD}	7
LAD11	R24	IO	OV_{DD}	7
LAD12	T24	IO	OV_{DD}	7
LAD13	U24	IO	OV_{DD}	7
LAD14	U26	IO	OV_{DD}	7
LAD15	V26	IO	OV_{DD}	7
LA16	K25	O	OV_{DD}	7
LA17	L25	O	OV_{DD}	7
LA18	L26	O	OV_{DD}	7
LA19	L24	O	OV_{DD}	7
LA20	M26	O	OV_{DD}	7
LA21	M25	O	OV_{DD}	7
LA22	N26	O	OV_{DD}	7
LA23	AC24	O	OV_{DD}	7
LA24	AC25	O	OV_{DD}	7
LA25	AB23	O	OV_{DD}	7
$\overline{\text{LCS0}}$	AB24	O	OV_{DD}	4

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PB17/BRGO1/CE_EXT_REQ1	D10	IO	OV_{DD}	—
GPIO_PB18/Enet4_TXD[0]/SER4_TXD[0]/ TDMD_TXD[0]	C10	IO	OV_{DD}	—
GPIO_PB19/Enet4_TXD[1]/SER4_TXD[1]/ TDMD_TXD[1]	C9	IO	OV_{DD}	—
GPIO_PB20/Enet4_TXD[2]/SER4_TXD[2]/ TDMD_TXD[2]	D8	IO	OV_{DD}	—
GPIO_PB21/Enet4_TXD[3]/SER4_TXD[3]/ TDMD_TXD[3]	C8	IO	OV_{DD}	—
GPIO_PB22/Enet4_RXD[0]/SER4_RXD[0]/ TDMD_RXD[0]	C15	IO	OV_{DD}	—
GPIO_PB23/Enet4_RXD[1]/SER4_RXD[1]/ TDMD_RXD[1]	C14	IO	OV_{DD}	—
GPIO_PB24/Enet4_RXD[2]/SER4_RXD[2]/ TDMD_RXD[2]	D13	IO	OV_{DD}	—
GPIO_PB25/Enet4_RXD[3]/SER4_RXD[3]/ TDMD_RXD[3]	C13	IO	OV_{DD}	—
GPIO_PB26/Enet4_RX_ER/SER4_CD/TDMD_REQ	C12	IO	OV_{DD}	—
GPIO_PB27/Enet4_TX_ER/TDMD_CLKO	D11	IO	OV_{DD}	—
GPIO_PB28/Enet4_RX_DV/SER4_CTS/ TDMD_RSYNC	D12	IO	OV_{DD}	—
GPIO_PB29/Enet4_COL/RXD[4]/SER4_RXD[4]/ TDMD_STROBE	D7	IO	OV_{DD}	—
GPIO_PB30/Enet4_TX_EN/SER4_RTS/ TDMD_TSYNC	C11	IO	OV_{DD}	—
GPIO_PB31/Enet4_CRS/SDET	C7	IO	OV_{DD}	—
GPIO_PC0/UPC1_TxDATA[0]/SER5_TXD[0]	A18	IO	OV_{DD}	—
GPIO_PC1/UPC1_TxDATA[1]/SER5_TXD[1]	A19	IO	OV_{DD}	—
GPIO_PC2/UPC1_TxDATA[2]/SER5_TXD[2]	B18	IO	OV_{DD}	—
GPIO_PC3/UPC1_TxDATA[3]/SER5_TXD[3]	B19	IO	OV_{DD}	—
GPIO_PC4/UPC1_TxDATA[4]	A24	IO	OV_{DD}	—
GPIO_PC5/UPC1_TxDATA[5]	B24	IO	OV_{DD}	—
GPIO_PC6/UPC1_TxDATA[6]	A23	IO	OV_{DD}	—
GPIO_PC7/UPC1_TxDATA[7]	B26	IO	OV_{DD}	—
GPIO_PC8/UPC1_RxDATA[0]/SER5_RXD[0]	A21	IO	OV_{DD}	—
GPIO_PC9/UPC1_RxDATA[1]/SER5_RXD[1]	B20	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PD10/GTM1_TIN2/GTM2_TIN1/CLK17	J24	IO	OV_{DD}	—
GPIO_PD11/GTM1_TGATE2/GTM2_TGATE1	B25	IO	OV_{DD}	—
GPIO_PD12/GTM1_TOUT2/GTM2_TOUT1	C4	IO	OV_{DD}	—
GPIO_PD13/GTM1_TIN3/GTM2_TIN4/BRGO8	D4	IO	OV_{DD}	—
GPIO_PD14/GTM1_TGATE3/GTM2_TGATE4	D5	IO	OV_{DD}	—
GPIO_PD15/GTM1_TOUT3	A5	IO	OV_{DD}	—
GPIO_PD16/GTM1_TIN4/GTM2_TIN3	B5	IO	OV_{DD}	—
GPIO_PD17/GTM1_TGATE4/GTM2_TGATE3	C5	IO	OV_{DD}	—
GPIO_PD18/GTM1_TOUT4/GTM2_TOUT3	A6	IO	OV_{DD}	—
GPIO_PD19/CE_RISC1_INT/CE_EXT_REQ4	B6	IO	OV_{DD}	—
GPIO_PD20/CLK18/BRGO6	D21	IO	OV_{DD}	—
GPIO_PD21/CLK16/BRGO5/UPC1_CLKO	C19	IO	OV_{DD}	—
GPIO_PD22/CLK4/BRGO9/UCC2_CLKO	A7	IO	OV_{DD}	—
GPIO_PD23/CLK3/BRGO10/UCC3_CLKO	B7	IO	OV_{DD}	—
GPIO_PD24/CLK10/BRGO2/UCC4_CLKO	A12	IO	OV_{DD}	—
GPIO_PD25/CLK13/BRGO16/UCC5_CLKO	B10	IO	OV_{DD}	—
GPIO_PD26/CLK2/BRGO4/UCC1_CLKO	E4	IO	OV_{DD}	—
GPIO_PD27/CLK1/BRGO3	F4	IO	OV_{DD}	—
GPIO_PD28/CLK19/BRGO11	D15	IO	OV_{DD}	—
GPIO_PD29/CLK15/BRGO8	C6	IO	OV_{DD}	—
GPIO_PD30/CLK14	D6	IO	OV_{DD}	—
GPIO_PD31/CLK7/BRGO15	E24	IO	OV_{DD}	—
Power and Ground Supplies				
GV_{DD}	AA8, AA10, AA11, AA13, AA14, AA16, AA17, AA19, AA21, AB9, AB10, AB11, AB12, AB14, AB18, AB20, AB21, AC6, AC8, AC14, AC18	GV_{DD}	—	—
OV_{DD}	E5, E6, E8, E9, E10, E12, E14, E15, E16, E18, E19, E20, E22, F5, F6, F8, F10, F14, F16, F19, F22, G22, H5, H6, H21, J5, J22, K21, K22, L5, L6, L22, M5, M22, N5, N21, N22, P6, P22, P23, R5, R23, T5, T21, T22, U6, U22, V5, V22, W22, Y5, AB5, AB6, AC5	OV_{DD}	—	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	K10, K11, K12, K13, K14, K15, K16, K17, L10, L17, M10, M17, N10, N17, P10, P17, R10, R17, T10, T17, U10, U11, U12, U13, U14, U15, U16, U17	V_{DD}	—	—
V_{SS}	B23, E7, E11, E13, E17, E21, F11, F13, F17, F21, F23, G5, H22, K5, K6, L11, L12, L13, L14, L15, L16, L21, M11, M12, M13, M14, M15, M16, N6, N11, N12, N13, N14, N15, N16, P5, P11, P12, P13, P14, P15, P16, P21, R11, R12, R13, R14, R15, R16, R22, T6, T11, T12, T13, T14, T15, T16, U5, U21, V23, W5, W6, W21, W23, W24, Y22, AA5, AA6, AA22, AA25, AB7, AB13, AB19, AB22, AC10, AC12, AC16, AC20	V_{SS}	—	—
No Connect				
NC	C22	—	—	—

Notes:
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG and local bus pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow the PCI specification's recommendation.
6. This pin must always be tied to GND. 7.This pin has weak internal pull-down N-FET that is always enabled.8.Though this pin has weak internal pull-up yet it is recommended to apply an external pull-up.

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

When CLKIN is the primary input clock,

$$ce\_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$$

When PCI_CLK is the primary input clock,

$$ce\_clk = [\text{primary clock input} \times \text{CEPMF} \times (1 + \sim\text{CFG\_CLKIN\_DIV})] \div (1 + \text{CEPDF})$$

See the “QUICC Engine PLL Multiplication Factor” section and the “QUICC Engine PLL Division Factor” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

The DDR SDRAM memory controller operates with a frequency equal to twice the frequency of *csb_clk*. Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The local bus memory controller operates with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBC clock divider ratio is controlled by LCRR[CLKDIV]. See the “LBC Bus Clock and Clock Ratios” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 56 specifies which units have a configurable clock frequency. Refer to the “System Clock Control Register (SCCR)” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for a detailed description.

Table 56. Configurable Clock Units

Unit	Default Frequency	Options
Security core, I2C, SAP, TPR	*csb_clk*	Off, *csb_clk*/2, *csb_clk*/3
PCI and DMA complex	*csb_clk*	Off, *csb_clk*

NOTE

Setting the clock ratio of these units must be performed prior to any access to them.

Table 57 provides the operating frequencies for the 8323E PBGA under recommended operating conditions (see Table 2).

Table 57. Operating Frequencies for PBGA

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	333	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
QUICC Engine frequency (*ce_clk*)	200	MHz

Table 57. Operating Frequencies for PBGA (continued)

Characteristic[1]	Max Operating Frequency	Unit
DDR1/DDR2 memory bus frequency (MCLK)[2]	133	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz
PCI input frequency (CLKIN or PCI_CLK)	66	MHz

[1] The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
[2] The DDR1/DDR2 data rate is 2× the DDR1/DDR2 memory bus frequency.
[3] The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

22.4 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 300–600 MHz.

Table 58. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

As described in Section 22, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG\_CLKIN\_DIV}}$ configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59 where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800