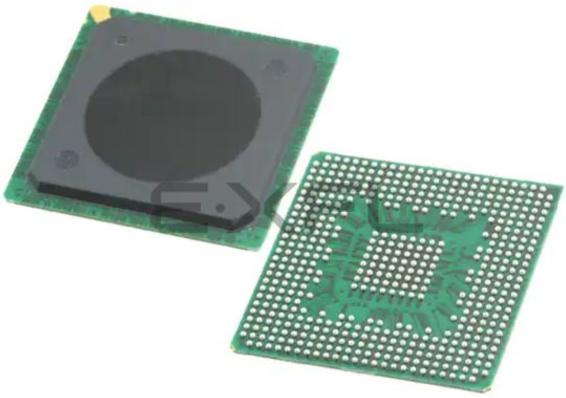

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8321czqaddc

Table 7. CLKIN DC Electrical Characteristics (continued)

CLKIN input current	$0\ V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±5	μA
PCI_SYNC_IN input current	$0\ V \le V_{IN} \le 0.5\ V$ or $OV_{DD} - 0.5\ V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±5	μA
PCI_SYNC_IN input current	$0.5\ V \le V_{IN} \le OV_{DD} - 0.5\ V$	I_{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 8 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the MPC8323E.

Table 8. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	25	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN rise and fall time	t_{KH}, t_{KL}	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core, security, and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

5 RESET Initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8323E. Table 9 provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{HRESET}$ or $\overline{SRESET}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{PORESET}$ with stable clock applied to CLKIN when the MPC8323E is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{PORESET}$ with stable clock applied to PCI_SYNC_IN when the MPC8323E is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of $\overline{\text{CFG\_CLKIN\_DIV}}$. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{OH} = -6.0$ mA	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 6.0$ mA	—	0.5	V	1
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR1 and DDR2 SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM (Dn_GV$_{DD}$(typ) = 1.8 V).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with Dn_GV$_{DD}$ of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MVREFn_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MVREFn_{REF} + 0.25	—	V	—

Table 17 provides the input AC timing specifications for the DDR1 SDRAM (Dn_GV$_{DD}$(typ) = 2.5 V).

Table 17. DDR1 SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with Dn_GV$_{DD}$ of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MVREFn_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MVREFn_{REF} + 0.31	—	V	—

Table 18 provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 18. DDR1 and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with Dn_GV$_{DD}$ of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
266 MHz		–750	750		
200 MHz		–1250	1250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = ±(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.

Figure 4 shows the input timing diagram for the DDR controller.

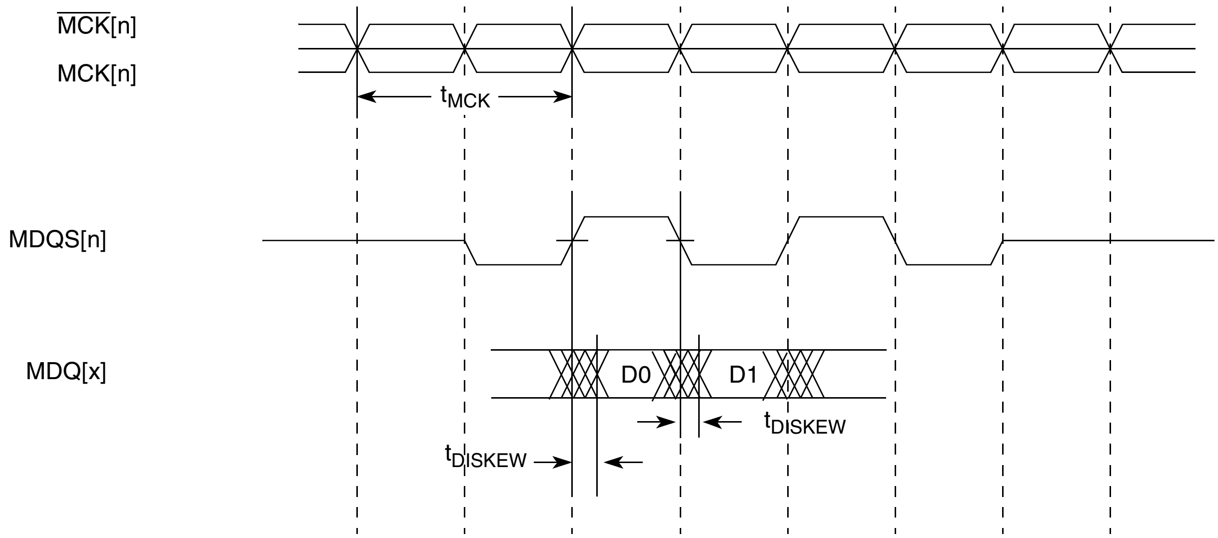


Figure 4. DDR Input Timing Diagram

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

Table 19 provides the output AC timing specifications for the DDR1 and DDR2 SDRAM interfaces.

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with D*n*_GV$_{DD}$ of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK cycle time, (MCK/$\overline{\text{MCK}}$ crossing)	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.5 3.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHAX}	 2.5 3.5	 — —	ns	3
$\overline{\text{MCS}}$ output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 2.5 3.5	 — —	ns	3
$\overline{\text{MCS}}$ output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 2.5 3.5	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4

Table 23. MII Transmit AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK data clock fall time	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 7 shows the MII transmit AC timing diagram.

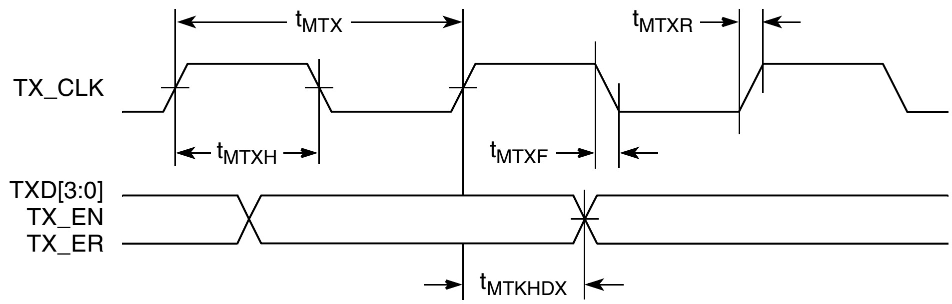


Figure 7. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time	t_{MRXR}	1.0	—	4.0	ns

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock fall time	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

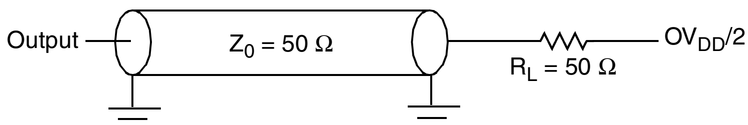


Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

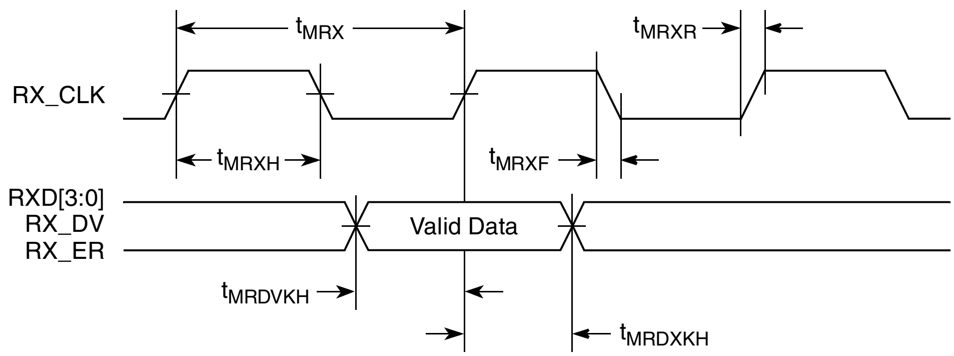


Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

Table 26. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load.

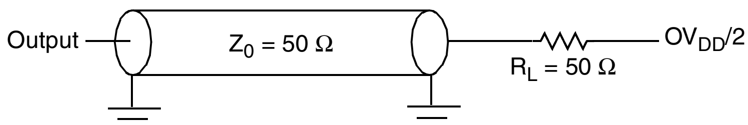


Figure 11. AC Test Load

Figure 12 shows the RMII receive AC timing diagram.

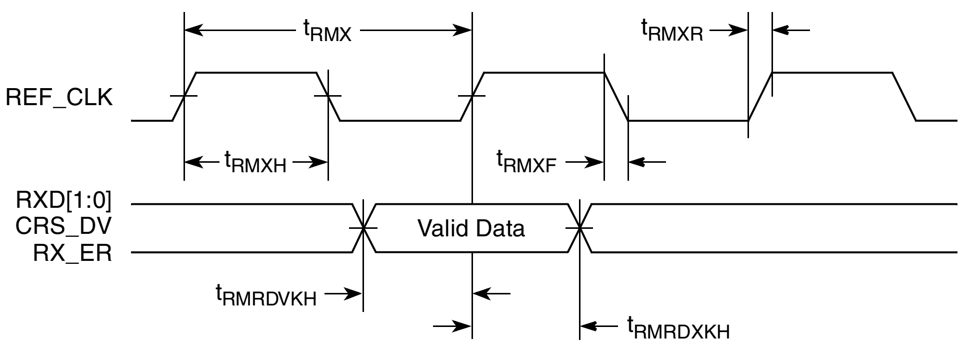


Figure 12. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, "Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.10	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII Management AC Electrical Specifications

Table 28 provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

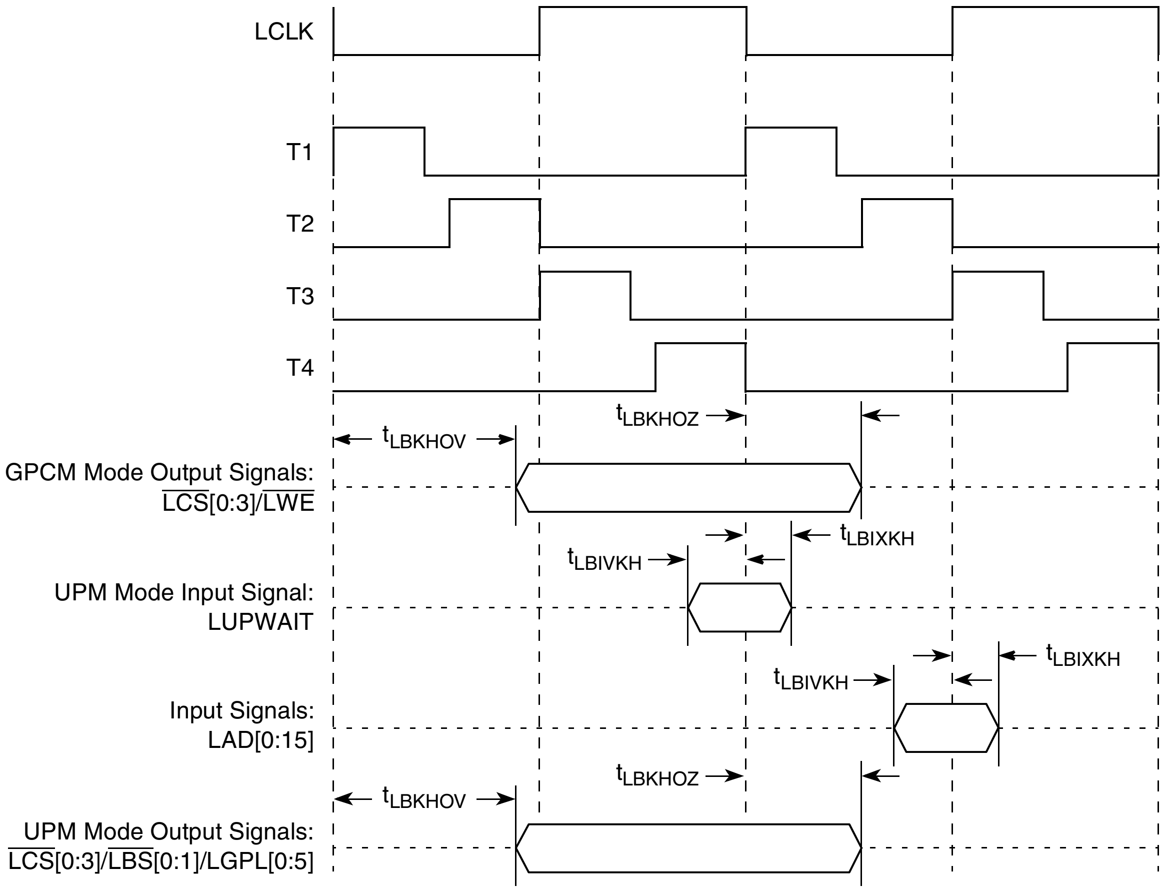


Figure 17. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8323E.

10.1 JTAG DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E.

Table 31. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.5	OV_{DD} + 0.3	V

Figure 27 shows the PCI output AC timing conditions.

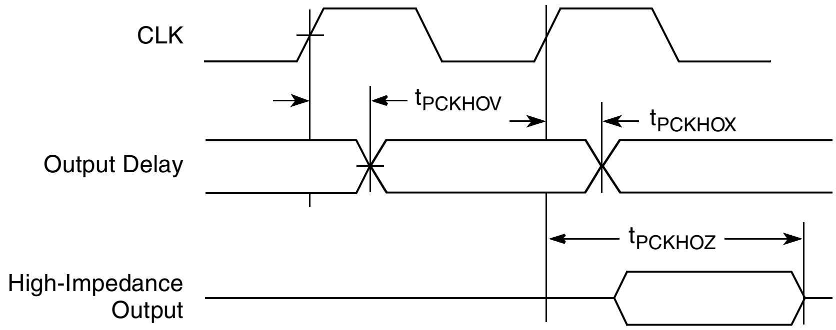


Figure 27. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8323E.

13.1 Timer DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the MPC8323E timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 38. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

13.2 Timer AC Timing Specifications

Table 39 provides the timer input and output AC timing specifications.

Table 39. Timer Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Figure 28 provides the AC test load for the timers.

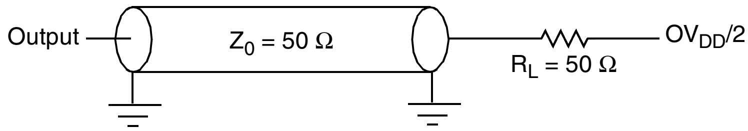


Figure 28. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8323E.

14.1 GPIO DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E GPIO.

Table 40. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

Table 41 provides the GPIO input and output AC timing specifications.

Table 41. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Table 46. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0\ V \le V_{IN} \le OV_{DD}$	—	±5	μA

17.2 TDM/SI AC Timing Specifications

Table 47 provides the TDM/SI input and output AC timing specifications.

Table 47. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	12	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 33 provides the AC test load for the TDM/SI.

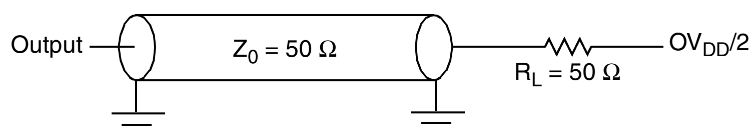
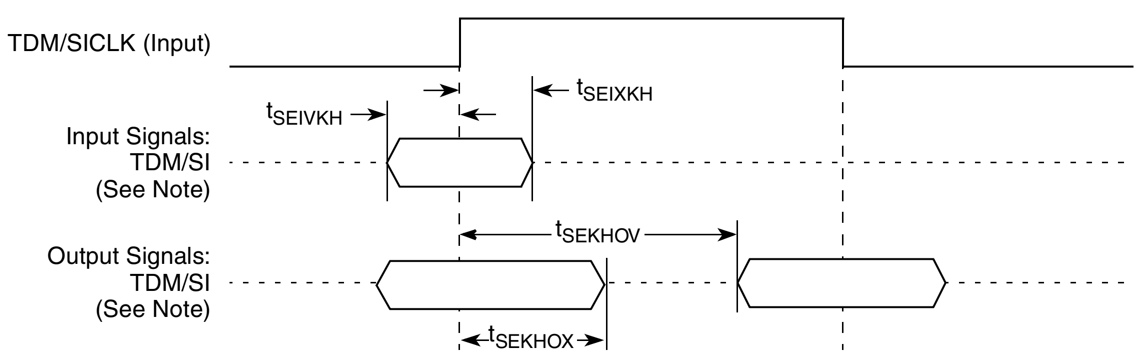


Figure 33. TDM/SI AC Test Load

Figure 34 represents the AC timing from Table 47. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on TDM/SI.

Figure 34. TDM/SI AC Timing (External Clock) Diagram

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 52. Synchronous UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	5.5	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	10	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	5.5	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	8	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	4	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	0	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{UAIKHOX}$ symbolizes the outputs internal timing (UAI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 38 provides the AC test load.

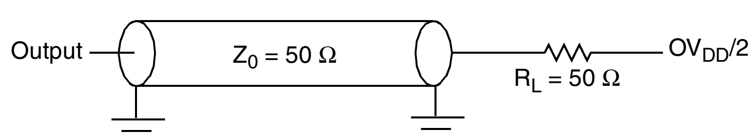
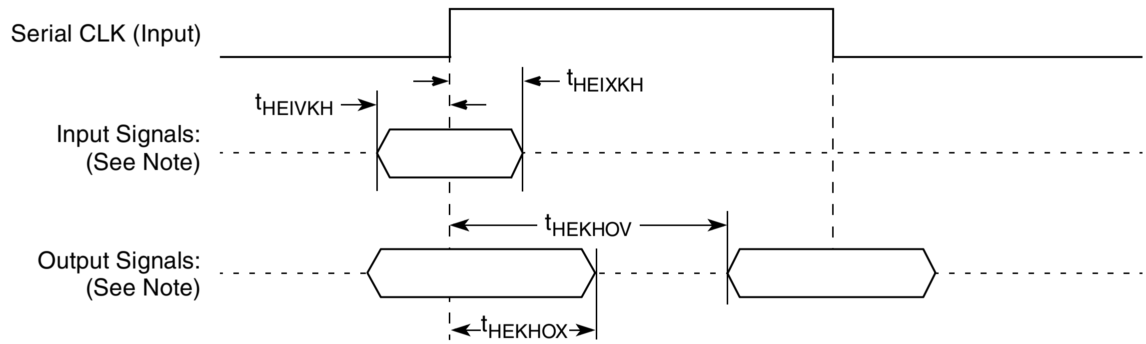


Figure 38. AC Test Load

Figure 39 and Figure 40 represent the AC timing from Table 51. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

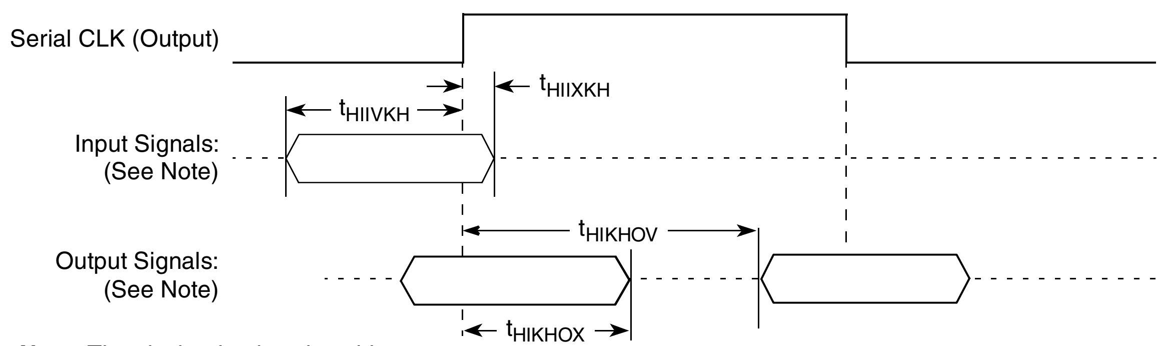
Figure 39 shows the timing with external clock.



Note: The clock edge is selectable.

Figure 39. AC Timing (External Clock) Diagram

Figure 40 shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 40. AC Timing (Internal Clock) Diagram

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE/GPIO				
GPIO_PA0/SER1_TXD[0]/TDMA_TXD[0]/USBTXN	G3	IO	OV_{DD}	—
GPIO_PA1/SER1_TXD[1]/TDMA_TXD[1]/USBTXP	F3	IO	OV_{DD}	—
GPIO_PA2/SER1_TXD[2]/TDMA_TXD[2]	F2	IO	OV_{DD}	—
GPIO_PA3/SER1_TXD[3]/TDMA_TXD[3]	E3	IO	OV_{DD}	—
GPIO_PA4/SER1_RXD[0]/TDMA_RXD[0]/USBRXP	E2	IO	OV_{DD}	—
GPIO_PA5/SER1_RXD[1]/TDMA_RXD[1]/USBRXN	E1	IO	OV_{DD}	—
GPIO_PA6/SER1_RXD[2]/TDMA_RXD[2]/USBRXD	D3	IO	OV_{DD}	—
GPIO_PA7/SER1_RXD[3]/TDMA_RXD[3]	D2	IO	OV_{DD}	—
GPIO_PA8/SER1_CD/TDMA_REQ/$\overline{\text{USBOE}}$	D1	IO	OV_{DD}	—
GPIO_PA9 TDMA_CLKO	C3	IO	OV_{DD}	—
GPIO_PA10/SER1_CTS/TDMA_RSYNC	C2	IO	OV_{DD}	—
GPIO_PA11/TDMA_STROBE	C1	IO	OV_{DD}	—
GPIO_PA12/SER1_RTS/TDMA_TSYNC	B1	IO	OV_{DD}	—
GPIO_PA13/CLK9/BRGO9	H4	IO	OV_{DD}	—
GPIO_PA14/CLK11/BRGO10	G4	IO	OV_{DD}	—
GPIO_PA15/BRGO7	J4	IO	OV_{DD}	—
GPIO_PA16/ LA0 (LBIU)	K24	IO	OV_{DD}	—
GPIO_PA17/ LA1 (LBIU)	K26	IO	OV_{DD}	—
GPIO_PA18/Enet2_TXD[0]/SER2_TXD[0]/ TDMB_TXD[0]/LA2 (LBIU)	G25	IO	OV_{DD}	—
GPIO_PA19/Enet2_TXD[1]/SER2_TXD[1]/ TDMB_TXD[1]/LA3 (LBIU)	G26	IO	OV_{DD}	—
GPIO_PA20/Enet2_TXD[2]/SER2_TXD[2]/ TDMB_TXD[2]/LA4 (LBIU)	H25	IO	OV_{DD}	—
GPIO_PA21/Enet2_TXD[3]/SER2_TXD[3]/ TDMB_TXD[3]/LA5 (LBIU)	H26	IO	OV_{DD}	—
GPIO_PA22/Enet2_RXD[0]/SER2_RXD[0]/ TDMB_RXD[0]/LA6 (LBIU)	C25	IO	OV_{DD}	—
GPIO_PA23/Enet2_RXD[1]/SER2_RXD[1]/ TDMB_RXD[1]/LA7 (LBIU)	C26	IO	OV_{DD}	—
GPIO_PA24/Enet2_RXD[2]/SER2_RXD[2]/ TDMB_RXD[2]/LA8 (LBIU)	D25	IO	OV_{DD}	—
GPIO_PA25/Enet2_RXD[3]/SER2_RXD[3]/ TDMB_RXD[3]/LA9 (LBIU)	D26	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PC10/UPC1_RxDATA[2]/SER5_RXD[2]	B21	IO	OV_{DD}	—
GPIO_PC11/UPC1_RxDATA[3]/SER5_RXD[3]	A20	IO	OV_{DD}	—
GPIO_PC12/UPC1_RxDATA[4]	D19	IO	OV_{DD}	—
GPIO_PC13/UPC1_RxDATA[5]/LSRCID0	C18	IO	OV_{DD}	—
GPIO_PC14/UPC1_RxDATA[6]/LSRCID1	D18	IO	OV_{DD}	—
GPIO_PC15/UPC1_RxDATA[7]/LSRCID2	A25	IO	OV_{DD}	—
GPIO_PC16/UPC1_TxADDR[0]	C21	IO	OV_{DD}	—
GPIO_PC17/UPC1_TxADDR[1]/LSRCID3	D22	IO	OV_{DD}	—
GPIO_PC18/UPC1_TxADDR[2]/LSRCID4	C23	IO	OV_{DD}	—
GPIO_PC19/UPC1_TxADDR[3]/LDVAL	D23	IO	OV_{DD}	—
GPIO_PC20/UPC1_RxADDR[0]	C17	IO	OV_{DD}	—
GPIO_PC21/UPC1_RxADDR[1]	D17	IO	OV_{DD}	—
GPIO_PC22/UPC1_RxADDR[2]	C16	IO	OV_{DD}	—
GPIO_PC23/UPC1_RxADDR[3]	D16	IO	OV_{DD}	—
GPIO_PC24/UPC1_RxSOC/SER5_CD	A16	IO	OV_{DD}	—
GPIO_PC25/UPC1_RxCLAV	D20	IO	OV_{DD}	—
GPIO_PC26/UPC1_RxPRTY/CE_EXT_REQ2	E23	IO	OV_{DD}	—
GPIO_PC27/UPC1_RxEN	B17	IO	OV_{DD}	—
GPIO_PC28/UPC1_TxSOC	B22	IO	OV_{DD}	—
GPIO_PC29/UPC1_TxCLAV/SER5_CTS	A17	IO	OV_{DD}	—
GPIO_PC30/UPC1_TxPRTY	A22	IO	OV_{DD}	—
GPIO_PC31/UPC1_TxEN/SER5_RTS	C20	IO	OV_{DD}	—
GPIO_PD0/SPIMOSI	A2	IO	OV_{DD}	—
GPIO_PD1/SPIMISO	B2	IO	OV_{DD}	—
GPIO_PD2/SPICLK	B3	IO	OV_{DD}	—
GPIO_PD3/SPISEL	A3	IO	OV_{DD}	—
GPIO_PD4/SPI_MDIO/CE_MUX_MDIO	A4	IO	OV_{DD}	—
GPIO_PD5/SPI_MDC/CE_MUX_MDC	B4	IO	OV_{DD}	—
GPIO_PD6/CLK8/BRGO16/CE_EXT_REQ3	F24	IO	OV_{DD}	—
GPIO_PD7/GTM1_TIN1/GTM2_TIN2/CLK5	G24	IO	OV_{DD}	—
GPIO_PD8/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$/CLK6	H24	IO	OV_{DD}	—
GPIO_PD9/$\overline{\text{GTM1\_TOUT1}}$	D24	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	K10, K11, K12, K13, K14, K15, K16, K17, L10, L17, M10, M17, N10, N17, P10, P17, R10, R17, T10, T17, U10, U11, U12, U13, U14, U15, U16, U17	V_{DD}	—	—
V_{SS}	B23, E7, E11, E13, E17, E21, F11, F13, F17, F21, F23, G5, H22, K5, K6, L11, L12, L13, L14, L15, L16, L21, M11, M12, M13, M14, M15, M16, N6, N11, N12, N13, N14, N15, N16, P5, P11, P12, P13, P14, P15, P16, P21, R11, R12, R13, R14, R15, R16, R22, T6, T11, T12, T13, T14, T15, T16, U5, U21, V23, W5, W6, W21, W23, W24, Y22, AA5, AA6, AA22, AA25, AB7, AB13, AB19, AB22, AC10, AC12, AC16, AC20	V_{SS}	—	—
No Connect				
NC	C22	—	—	—

Notes:
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG and local bus pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow the PCI specification’s recommendation.
6. This pin must always be tied to GND. 7.This pin has weak internal pull-down N-FET that is always enabled.8.Though this pin has weak internal pull-up yet it is recommended to apply an external pull-up.

22.1 Clocking in PCI Host Mode

When the MPC8323E is configured as a PCI host device (RCWH[PCIHOST] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexors. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

22.1.1 PCI Clock Outputs (PCI_CLK_OUT[0:2])

When the MPC8323E is configured as a PCI host, it provides three separate clock output signals, PCI_CLK_OUT[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOE*n*] bit. All output clocks are phase-aligned to each other.

22.2 Clocking in PCI Agent Mode

When the MPC8323E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND, and the clock output signals, PCI_CLK_OUT*n* and PCI_SYNC_OUT, are not used.

22.3 System Clock Domains

As shown in Figure 43, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*ce_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lb_clk*)

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = [\mathrm{PCI\_SYNC\_IN} \times (1 + \sim\overline{\mathrm{CFG\_CLKIN\_DIV}})] \times \mathrm{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\mathrm{CFG\_CLKIN\_DIV}}$) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300c2 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See the “Reset Configuration” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

Table 57. Operating Frequencies for PBGA (continued)

Characteristic[1]	Max Operating Frequency	Unit
DDR1/DDR2 memory bus frequency (MCLK)[2]	133	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz
PCI input frequency (CLKIN or PCI_CLK)	66	MHz

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2 The DDR1/DDR2 data rate is 2× the DDR1/DDR2 memory bus frequency.
3 The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

22.4 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 300–600 MHz.

Table 58. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

As described in Section 22, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG\_CLKIN\_DIV}}$ configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59

22.5 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 60 shows the encodings for RCWL[COREPLL]. COREPLL values not listed in Table 60 should be considered reserved.

Table 60. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷2
01	0001	1	1.5:1	÷4
10	0001	1	1.5:1	÷8
11	0001	1	1.5:1	÷8
00	0010	0	2:1	÷2
01	0010	0	2:1	÷4
10	0010	0	2:1	÷8
11	0010	0	2:1	÷8
00	0010	1	2.5:1	÷2
01	0010	1	2.5:1	÷4
10	0010	1	2.5:1	÷8
11	0010	1	2.5:1	÷8
00	0011	0	3:1	÷2
01	0011	0	3:1	÷4
10	0011	0	3:1	÷8
11	0011	0	3:1	÷8

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 500–800 MHz.