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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8321czqafdc

1 Overview

The MPC8323E incorporates the e300c2 (MPC603e-based) core built on Power Architecture® technology, which includes 16 Kbytes of L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The e300c2 core does not contain a floating point unit (FPU). The MPC8323E also includes a 32-bit PCI controller, four DMA channels, a security engine, and a 32-bit DDR1/DDR2 memory controller.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8323E. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). Note that the MPC8321 and MPC8321E do not support UTOPIA. A block diagram of the MPC8323E is shown in Figure 1.

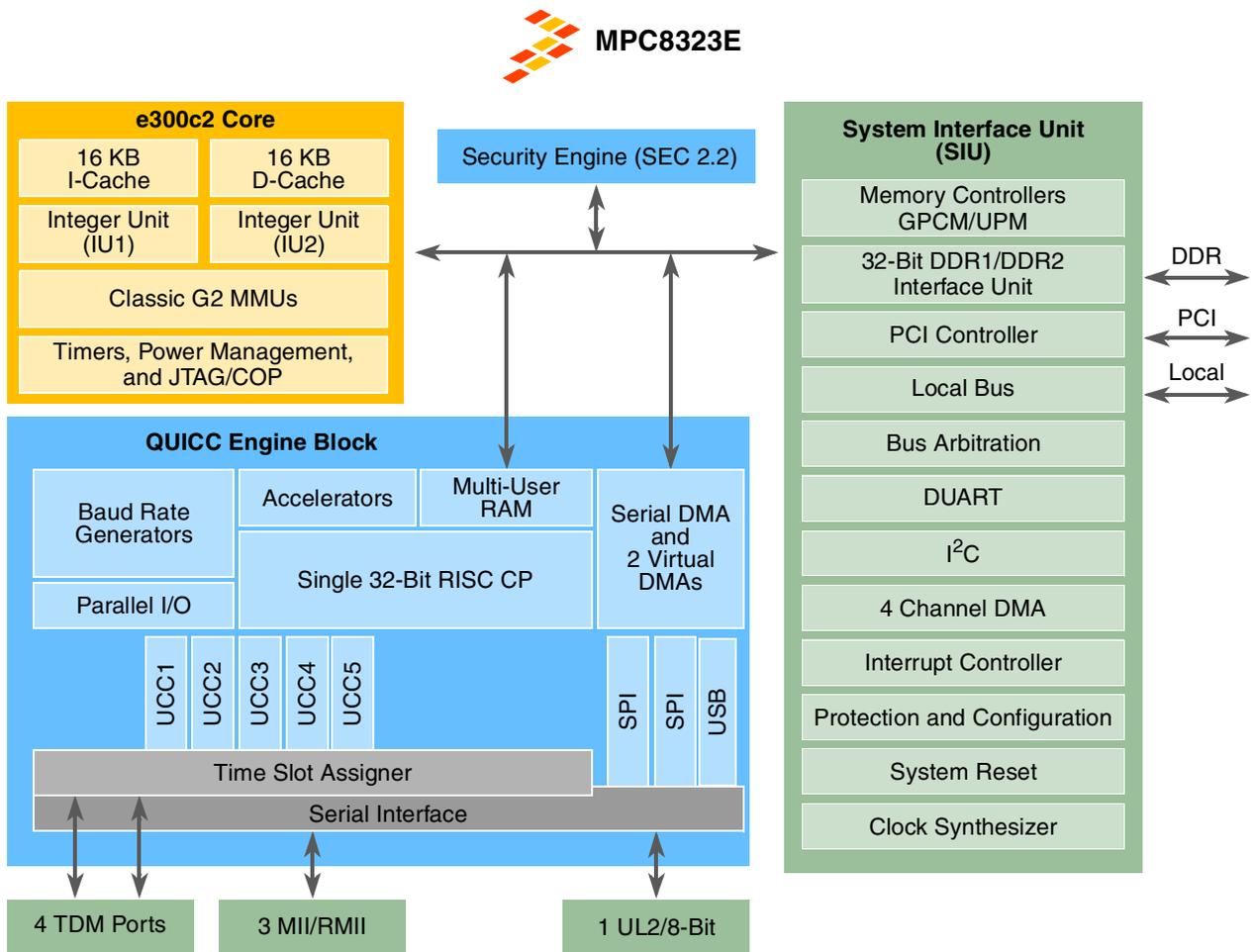


Figure 1. MPC8323E Block Diagram

Each of the five UCCs can support a variety of communication protocols: 10/100 Mbps Ethernet, serial ATM, HDLC, UART, and BISYNC—and, in the MPC8323E and MPC8323, multi-PHY ATM and ATM support for up to OC-3 speeds.

1.1.2 Serial Interfaces

The MPC8323E serial interfaces are as follows:

- Support for one UL2 interface with 31 multi-PHY addresses (MPC8323E and MPC8323 only)
- Support for up to three 10/100 Mbps Ethernet interfaces using MII or RMII
- Support for up to four T1/E1/J1/E3 or DS-3 serial interfaces (TDM)
- Support for dual UART and SPI interfaces and a single I²C interface

1.2 QUICC Engine Block

The QUICC Engine block is a versatile communications complex that integrates several communications peripheral controllers. It provides on-chip system design for a variety of applications, particularly in communications and networking systems. The QUICC Engine block has the following features:

- One 32-bit RISC controller for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
 - 10/100 Mbps Ethernet/IEEE 802.3® standard
 - IP support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
 - ATM protocol through UTOPIA interface (note that the MPC8321 and MPC8321E do not support the UTOPIA interface)
 - HDLC /transparent up to 70-Mbps full-duplex
 - HDLC bus up to 10 Mbps
 - Asynchronous HDLC
 - UART
 - BISYNC up to 2 Mbps
 - QUICC multi-channel controller (QMC) for 64 TDM channels
- One UTOPIA interface (UPC1) supporting 31 multi-PHYs (MPC8323E- and MPC8323-specific)
- Two serial peripheral interfaces (SPI). SPI2 is dedicated to Ethernet PHY management.
- Four TDM interfaces
- Thirteen independent baud rate generators and 19 input clock pins for supplying clocks to UCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

The UCCs are similar to the PowerQUICC II peripherals: SCC (BISYNC, UART, and HDLC bus) and FCC (fast Ethernet, HDLC, transparent, and ATM).

1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i™ standard, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8323E DDR1/DDR2 memory controller includes the following features:

- Single 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266-MHz data rate
- Support for two $\times 16$ devices
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O
- Support for 1 chip select only
- FCRAM, ECC, hardware/software calibration, bit deskew, QIN stage, or atomic logic are not supported.

1.5 PCI Controller

The MPC8323E PCI controller includes the following features:

- *PCI Specification Revision 2.3* compatible
- Single 32-bit data PCI interface operates up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

1.6 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 35 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

Figure 4 shows the input timing diagram for the DDR controller.

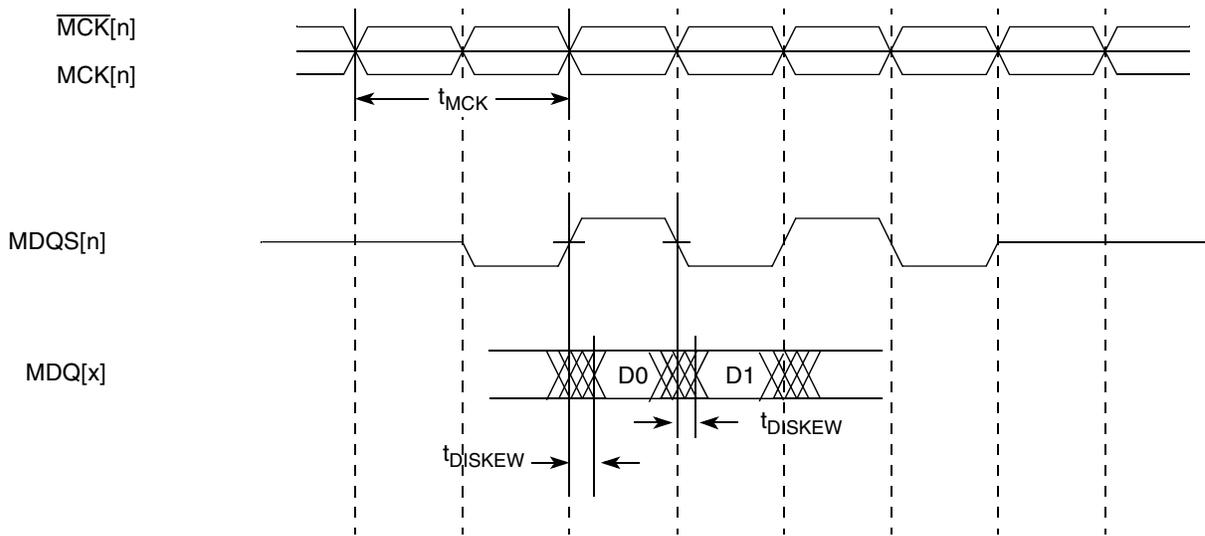


Figure 4. DDR Input Timing Diagram

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

Table 19 provides the output AC timing specifications for the DDR1 and DDR2 SDRAM interfaces.

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with $D_n_GV_{DD}$ of $(1.8 \text{ or } 2.5 \text{ V}) \pm 5\%$.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK cycle time, (MCK/MCK crossing)	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}	2.5 3.5	— —	ns	3
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}	2.5 3.5	— —	ns	3
MCS output setup with respect to MCK	t_{DDKHCS}	2.5 3.5	— —	ns	3
MCS output hold with respect to MCK	t_{DDKHCS}	2.5 3.5	— —	ns	3
MCK to MDQS Skew	t_{DDKMHM}	-0.6	0.6	ns	4

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)

 At recommended operating conditions with $D_n_GV_{DD}$ of (1.8 or 2.5 V) \pm 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MDQ/MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	0.9 1.0	— —	ns	5
MDQ/MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX} , t_{DDKLDX}	1100 1200	— —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	-0.6	0.6	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/\overline{MCK} referenced measurements are made from the crossing of the two signals ± 0.1 V.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/\overline{MCK} , \overline{MCS} , and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
- Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
RX_CLK clock fall time	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

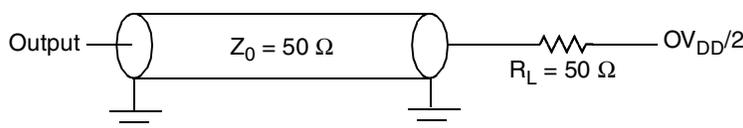


Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

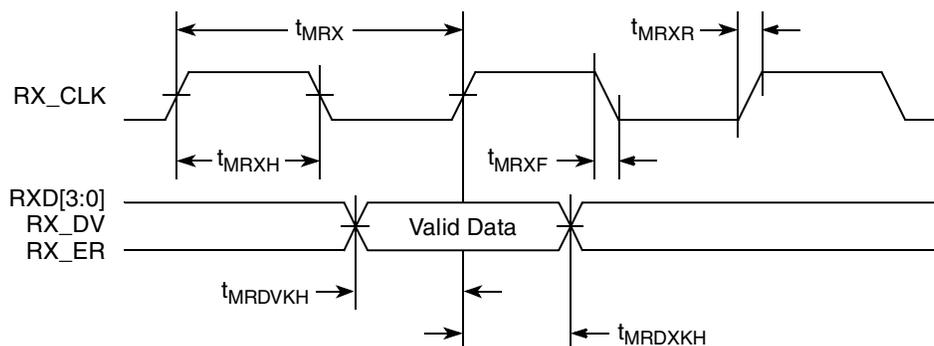


Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 27](#).

Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—	2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$ $OV_{DD} = \text{Min}$	2.10	$OV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$ $OV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	2.00	—	V
Input low voltage	V_{IL}	—	—	0.80	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

8.3.2 MII Management AC Electrical Specifications

[Table 28](#) provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is $3.3 \text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 13 shows the MII management AC timing diagram.

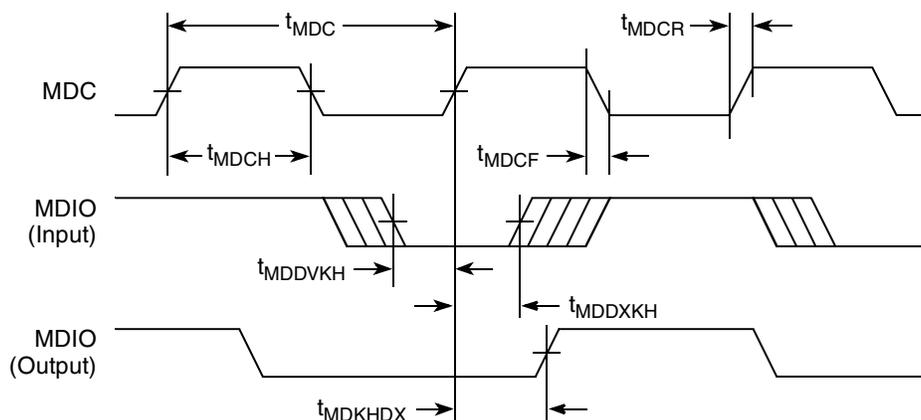


Figure 13. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8323E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V
Input current	I_{IN}	—	± 5	μA

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8323E.

Table 30. Local Bus General Timing Parameters

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK n)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK n)	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5

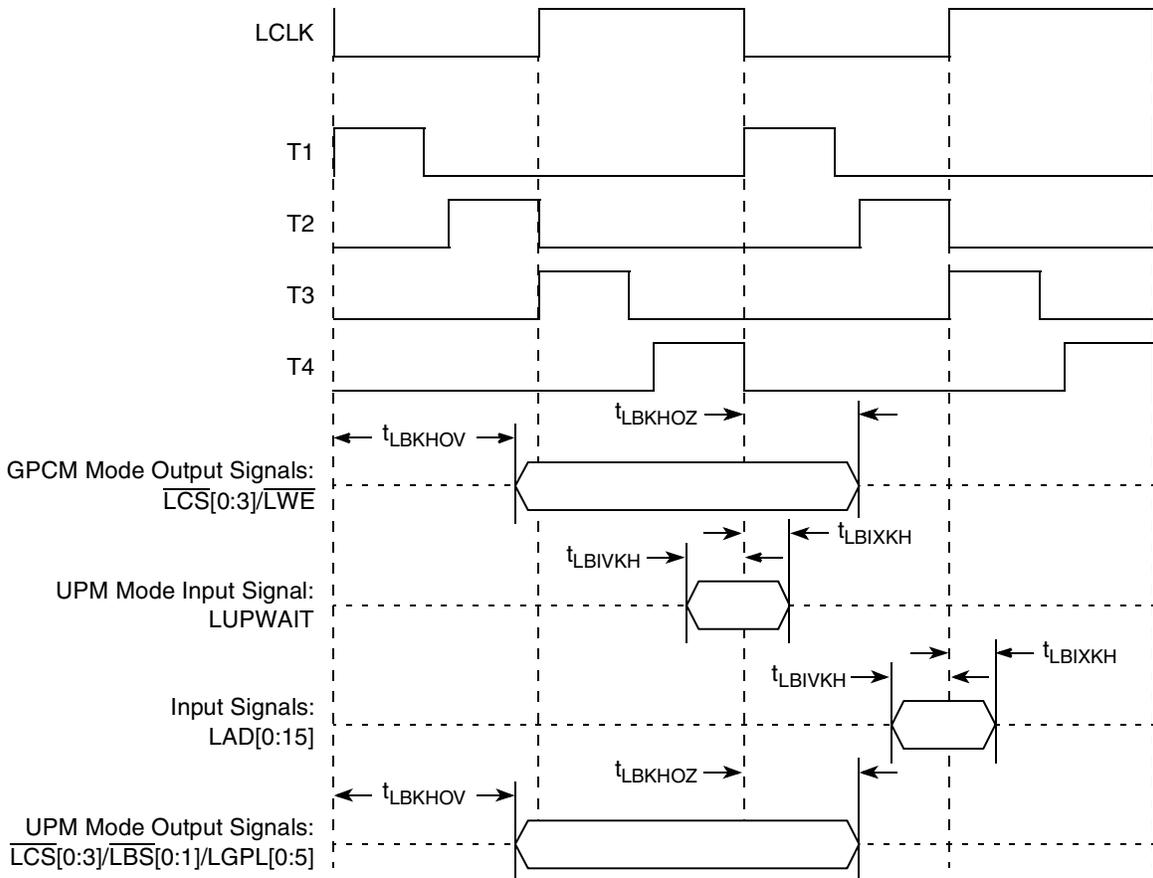


Figure 17. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8323E.

10.1 JTAG DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E.

Table 31. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.5	$OV_{DD} + 0.3$	V

Table 31. JTAG Interface DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E. [Table 32](#) provides the JTAG AC timing specifications as defined in [Figure 19](#) through [Figure 22](#).

Table 32. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see [Table 2](#)).

Parameter	Symbol ²	Min	Max	Unit	Notes	
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—	
JTAG external clock cycle time	t_{JTG}	30	—	ns	—	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	11	—	ns	—	
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3	
Input setup times:	Boundary-scan data TMS, TDI	t_{JTDVKH}	4	—	ns	4
		t_{JTIVKH}	4	—		
Input hold times:	Boundary-scan data TMS, TDI	t_{JTDXKH}	10	—	ns	4
		t_{JTIXKH}	10	—		
Valid times:	Boundary-scan data TDO	t_{JTKLDV}	2	15	ns	5
		t_{JTKLOV}	2	15		
Output hold times:	Boundary-scan data TDO	t_{JTKLDX}	2	—	ns	5
		t_{JTKLOX}	2	—		

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

Table 33. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t_{I2KLV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0\text{ V} \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 5	μA	4

Notes:

- Output voltage (open drain or open collector) condition = 3 mA sink current.
- C_B = capacitance of one bus line in pF.
- Refer to the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for information on the digital filter used.
- I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I²C interface of the MPC8323E.

Table 34. I²C AC Electrical Specifications

All values refer to $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ levels (see Table 33).

Parameter	Symbol ¹	Min	Max	Unit	
SCL clock frequency	f_{I2C}	0	400	kHz	
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	
High period of the SCL clock	t_{I2CH}	0.6	—	μs	
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	
Data setup time	t_{I2DVKH}	100	—	ns	
Data hold time:	CBUS compatible masters I ² C bus devices	t_{I2DXKL}	— 0^2	— 0.9^3	μs

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Table 44. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 30 provides the AC test load for the SPI.

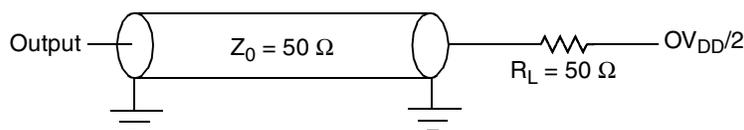


Figure 30. SPI AC Test Load

Figure 31 and Figure 32 represent the AC timing from Table 45. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 31 shows the SPI timing in slave mode (external clock).

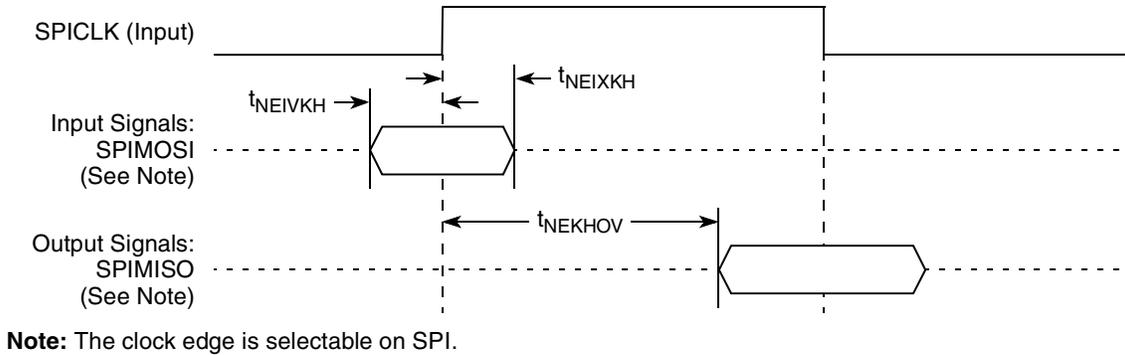


Figure 31. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 32 shows the SPI timing in master mode (internal clock).

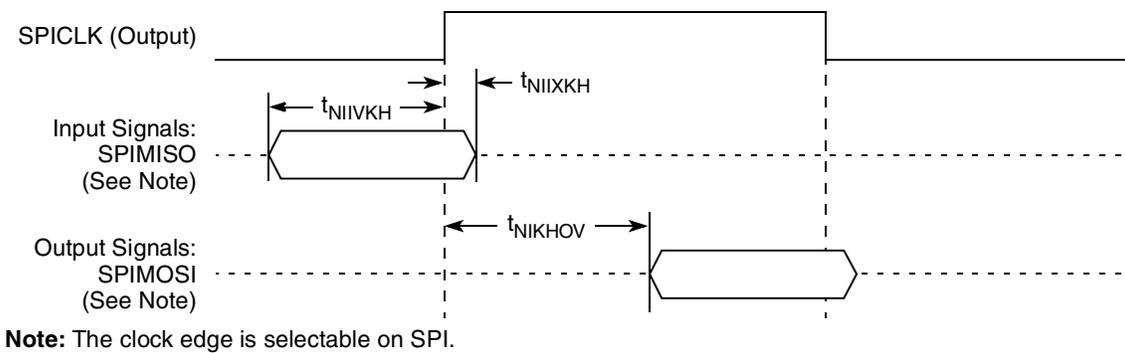


Figure 32. SPI AC Timing in Master Mode (Internal Clock) Diagram

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8323E.

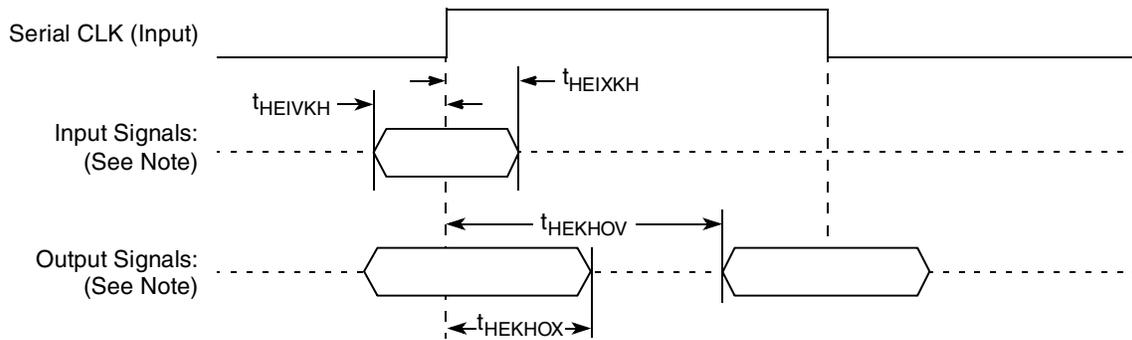
17.1 TDM/SI DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the MPC8323E TDM/SI.

Table 46. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -2.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.5	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V

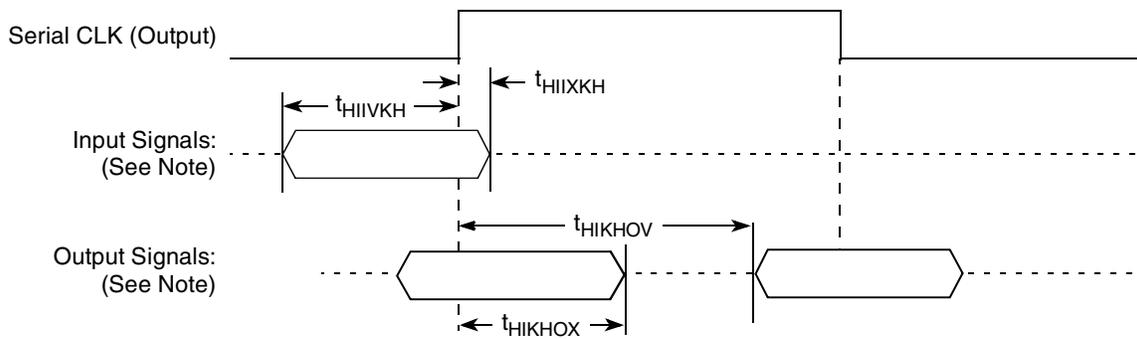
Figure 39 shows the timing with external clock.



Note: The clock edge is selectable.

Figure 39. AC Timing (External Clock) Diagram

Figure 40 shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 40. AC Timing (Internal Clock) Diagram

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	O	GV _{DD}	3
MEMC_MCK	AF14	O	GV _{DD}	—
$\overline{\text{MEMC_MCK}}$	AE14	O	GV _{DD}	—
MEMC_MODT	AF11	O	GV _{DD}	—
Local Bus Controller Interface				
LAD0	N25	IO	OV _{DD}	7
LAD1	P26	IO	OV _{DD}	7
LAD2	P25	IO	OV _{DD}	7
LAD3	R26	IO	OV _{DD}	7
LAD4	R25	IO	OV _{DD}	7
LAD5	T26	IO	OV _{DD}	7
LAD6	T25	IO	OV _{DD}	7
LAD7	U25	IO	OV _{DD}	7
LAD8	M24	IO	OV _{DD}	7
LAD9	N24	IO	OV _{DD}	7
LAD10	P24	IO	OV _{DD}	7
LAD11	R24	IO	OV _{DD}	7
LAD12	T24	IO	OV _{DD}	7
LAD13	U24	IO	OV _{DD}	7
LAD14	U26	IO	OV _{DD}	7
LAD15	V26	IO	OV _{DD}	7
LA16	K25	O	OV _{DD}	7
LA17	L25	O	OV _{DD}	7
LA18	L26	O	OV _{DD}	7
LA19	L24	O	OV _{DD}	7
LA20	M26	O	OV _{DD}	7
LA21	M25	O	OV _{DD}	7
LA22	N26	O	OV _{DD}	7
LA23	AC24	O	OV _{DD}	7
LA24	AC25	O	OV _{DD}	7
LA25	AB23	O	OV _{DD}	7
$\overline{\text{LCS0}}$	AB24	O	OV _{DD}	4

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_AD20	AB2	IO	OV _{DD}	—
PCI_AD21	Y4	IO	OV _{DD}	—
PCI_AD22	AC1	IO	OV _{DD}	—
PCI_AD23	AA3	IO	OV _{DD}	—
PCI_AD24	AA4	IO	OV _{DD}	—
PCI_AD25	AD1	IO	OV _{DD}	—
PCI_AD26	AD2	IO	OV _{DD}	—
PCI_AD27	AB3	IO	OV _{DD}	—
PCI_AD28	AB4	IO	OV _{DD}	—
PCI_AD29	AE1	IO	OV _{DD}	—
PCI_AD30	AC3	IO	OV _{DD}	—
PCI_AD31	AC4	IO	OV _{DD}	—
PCI_C_BE0	M4	IO	OV _{DD}	—
PCI_C_BE1	T4	IO	OV _{DD}	—
PCI_C_BE2	Y3	IO	OV _{DD}	—
PCI_C_BE3	AC2	IO	OV _{DD}	—
PCI_PAR	U3	IO	OV _{DD}	—
PCI_FRAME	W1	IO	OV _{DD}	5
PCI_TRDY	W4	IO	OV _{DD}	5
PCI_IRDY	W2	IO	OV _{DD}	5
PCI_STOP	V4	IO	OV _{DD}	5
PCI_DEVSEL	W3	IO	OV _{DD}	5
PCI_IDSEL	P2	I	OV _{DD}	—
PCI_SERR	U4	IO	OV _{DD}	5
PCI_PERR	V3	IO	OV _{DD}	5
PCI_REQ0	AD4	IO	OV _{DD}	—
PCI_REQ1/CPCI_HS_ES	AE3	I	OV _{DD}	—
PCI_REQ2	AF3	I	OV _{DD}	—
PCI_GNT0	AD3	IO	OV _{DD}	—
PCI_GNT1/CPCI_HS_LED	AE4	O	OV _{DD}	—
PCI_GNT2/CPCI_HS_ENUM	AF4	O	OV _{DD}	—
M66EN	L4	I	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PA26/Enet2_RX_ER/SER2_CD/TDMB_REQ/LA10 (LBIU)	E26	IO	OV _{DD}	—
GPIO_PA27/Enet2_TX_ER/TDMB_CLKO/LA11 (LBIU)	F25	IO	OV _{DD}	—
GPIO_PA28/Enet2_RX_DV/SER2_CTS/TDMB_RSYNC/LA12 (LBIU)	E25	IO	OV _{DD}	—
GPIO_PA29/Enet2_COL/RXD[4]/SER2_RXD[4]/TDMB_STROBE/LA13 (LBIU)	J25	IO	OV _{DD}	—
GPIO_PA30/Enet2_TX_EN/SER2_RTS/TDMB_TSYNC/LA14 (LBIU)	F26	IO	OV _{DD}	—
GPIO_PA31/Enet2_CRS/SDET LA15 (LBIU)	J26	IO	OV _{DD}	—
GPIO_PB0/Enet3_TXD[0]/SER3_TXD[0]/TDMC_TXD[0]	A13	IO	OV _{DD}	—
GPIO_PB1/Enet3_TXD[1]/SER3_TXD[1]/TDMC_TXD[1]	B13	IO	OV _{DD}	—
GPIO_PB2/Enet3_TXD[2]/SER3_TXD[2]/TDMC_TXD[2]	A14	IO	OV _{DD}	—
GPIO_PB3/Enet3_TXD[3]/SER3_TXD[3]/TDMC_TXD[3]	B14	IO	OV _{DD}	—
GPIO_PB4/Enet3_RXD[0]/SER3_RXD[0]/TDMC_RXD[0]	B8	IO	OV _{DD}	—
GPIO_PB5/Enet3_RXD[1]/SER3_RXD[1]/TDMC_RXD[1]	A8	IO	OV _{DD}	—
GPIO_PB6/Enet3_RXD[2]/SER3_RXD[2]/TDMC_RXD[2]	A9	IO	OV _{DD}	—
GPIO_PB7/Enet3_RXD[3]/SER3_RXD[3]/TDMC_RXD[3]	B9	IO	OV _{DD}	—
GPIO_PB8/Enet3_RX_ER/SER3_CD/TDMC_REQ	A11	IO	OV _{DD}	—
GPIO_PB9/Enet3_TX_ER/TDMC_CLKO	B11	IO	OV _{DD}	—
GPIO_PB10/Enet3_RX_DV/SER3_CTS/TDMC_RSYNC	A10	IO	OV _{DD}	—
GPIO_PB11/Enet3_COL/RXD[4]/SER3_RXD[4]/TDMC_STROBE	A15	IO	OV _{DD}	—
GPIO_PB12/Enet3_TX_EN/SER3_RTS/TDMC_TSYNC	B12	IO	OV _{DD}	—
GPIO_PB13/Enet3_CRS/SDET	B15	IO	OV _{DD}	—
GPIO_PB14/CLK12	D9	IO	OV _{DD}	—
GPIO_PB15 UPC1_TxADDR[4]	D14	IO	OV _{DD}	—
GPIO_PB16 UPC1_RxADDR[4]	B16	IO	OV _{DD}	—

shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 59. CSB Frequency Options

CFG_CLKIN_DIV_B at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	Input Clock Frequency (MHz) ²		
			25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)		
High	0010	2 : 1			133
High	0011	3 : 1		100	
High	0100	4 : 1	100	133	
High	0101	5 : 1	125		
High	0110	6 : 1			
High	0111	7 : 1			
High	1000	8 : 1			
High	1001	9 : 1			
High	1010	10 : 1			
High	1011	11 : 1			
High	1100	12 : 1			
High	1101	13 : 1			
High	1110	14 : 1			
High	1111	15 : 1			
High	0000	16 : 1			
Low	0010	2 : 1			133
Low	0011	3 : 1		100	
Low	0100	4 : 1		133	
Low	0101	5 : 1			
Low	0110	6 : 1			
Low	0111	7 : 1			
Low	1000	8 : 1			
Low	1001	9 : 1			
Low	1010	10 : 1			
Low	1011	11 : 1			
Low	1100	12 : 1			
Low	1101	13 : 1			
Low	1110	14 : 1			
Low	1111	15 : 1			
Low	0000	16 : 1			

¹ CFG_CLKIN_DIV_B is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV_B must be pulled up (high) in agent mode.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

P_D = power dissipation (W)

24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8323E.

24.1 System Clocking

The MPC8323E includes three PLLs.

- The system PLL (AV_{DD2}) generates the system clock from the externally supplied CLKIN input. The frequency ratio between the system and CLKIN is selected using the system PLL ratio configuration bits as described in [Section 22.4, “System PLL Configuration.”](#)
- The e300 core PLL (AV_{DD3}) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in [Section 22.5, “Core PLL Configuration.”](#)
- The QUICC Engine PLL (AV_{DD1}) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each AV_{DDⁿ} pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in [Figure 44](#), one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 44 shows the PLL power supply filter circuit.

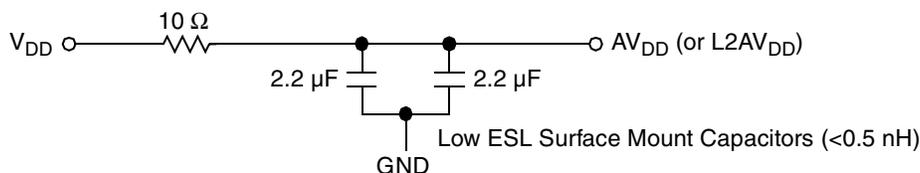


Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8323E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8323E system, and the MPC8323E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , and GV_{DD} pins of the MPC8323E. These decoupling capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , OV_{DD} , and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , or GV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , OV_{DD} , and GND pins of the MPC8323E.

24.5 Output Buffer DC Impedance

The MPC8323E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The