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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8321ecvrafdc

NOTE

The QUICC Engine block can also support a UTOPIA level 2 capable of supporting 31 multi-PHY (MPC8323E- and MPC8323-specific).

The MPC8323E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In summary, the MPC8323E family provides users with a highly integrated, fully programmable communications processor. This helps ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

1.1 MPC8323E Features

Major features of the MPC8323E are as follows:

- High-performance, low-power, and cost-effective single-chip data-plane/control-plane solution for ATM or IP/Ethernet packet processing (or both).
- MPC8323E QUICC Engine block offers a future-proof solution for next generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards.
- Single platform architecture supports the convergence of IP packet networks and ATM networks.
- DDR1/DDR2 memory controller—one 32-bit interface at up to 266 MHz supporting both DDR1 and DDR2.
- An e300c2 core built on Power Architecture technology with 16-Kbyte instruction and data caches, and dual integer units.
- Peripheral interfaces such as 32-bit PCI (2.2) interface up to 66-MHz operation, 16-bit local bus interface up to 66-MHz operation, and USB 2.0 (full-/low-speed).
- Security engine provides acceleration for control and data plane security protocols.
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration.

1.1.1 Protocols

The protocols are as follows:

- ATM SAR up to 155 Mbps (OC-3) full duplex, with ATM traffic shaping (ATF TM4.1)
- Support for ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- Support for IMA and ATM transmission convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- Support for 64 channels of HDLC/transparent

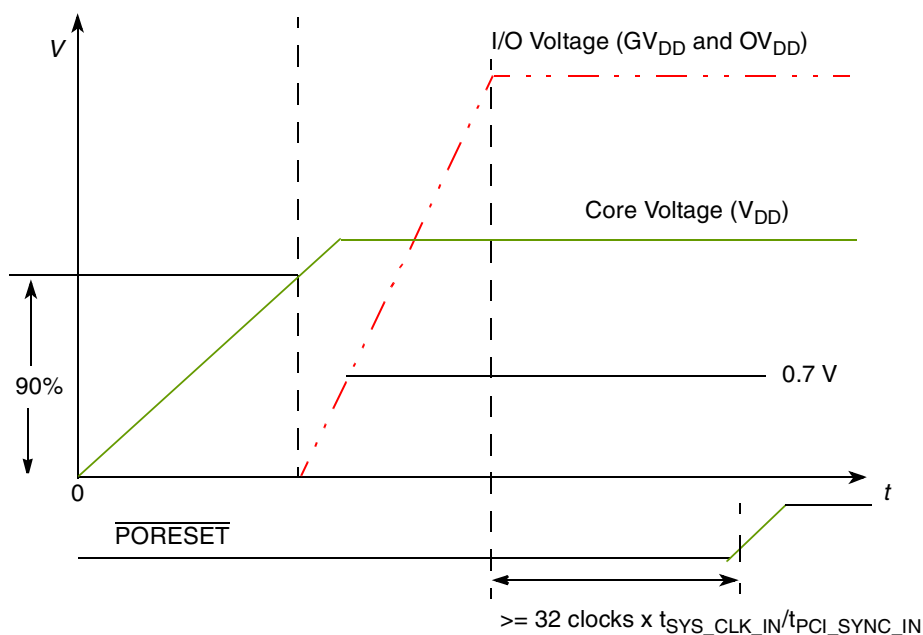


Figure 3. MPC8323E Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation for this family of MPC8323E devices is shown in [Table 5](#).

Table 5. MPC8323E Power Dissipation

CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Core Frequency (MHz)	Typical	Maximum	Unit	Notes
133	200	266	0.74	1.48	W	1, 2, 3
133	200	333	0.78	1.62	W	1, 2, 3

Notes:

1. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or AV_{DD} . For I/O power values, see [Table 6](#).
2. Typical power is based on a nominal voltage of $V_{DD} = 1.0$ V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the MPC8323MDS evaluation board using WC process silicon.
3. Maximum power is based on a voltage of $V_{DD} = 1.07$ V, WC process, a junction $T_J = 110^{\circ}\text{C}$, and an artificial smoke test.

[Table 6](#) shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V $R_s = 20\ \Omega$ $R_t = 50\ \Omega$ 1 pair of clocks	266 MHz, 1×32 bits	0.212	0.367	—	W	—

Table 6. Estimated Typical I/O Power Dissipation (continued)

Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 32 bits	—	—	0.12	W	—
PCI I/O load = 30 pF	66 MHz, 32 bits	—	—	0.057	W	—
QUICC Engine block and other I/Os	UTOPIA 8-bit 31 PHYs	—	—	0.041	W	Multiply by number of interfaces used.
	TDM serial	—	—	0.001	W	
	TDM nibble	—	—	0.004	W	
	HDLC/TRAN serial	—	—	0.003	W	
	HDLC/TRAN nibble	—	—	0.025	W	
	DUART	—	—	0.017	W	
	MIIs	—	—	0.009	W	
	RMII	—	—	0.009	W	
	Ethernet management	—	—	0.002	W	
	USB	—	—	0.001	W	
	SPI	—	—	0.001	W	
	Timer output	—	—	0.002	W	

NOTE

AV_{DDn} (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	$OV_{DD} + 0.3$	V
Input low voltage	—	V_{IL}	−0.3	0.4	V

Table 11. Reset Signals DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA	—

Note:

1. This specification applies when operating from 3.3 V supply.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR1 and DDR2 SDRAM interface of the MPC8323E. Note that DDR1 SDRAM is $Dn_GV_{DD}(\text{typ}) = 2.5\text{ V}$ and DDR2 SDRAM is $Dn_GV_{DD}(\text{typ}) = 1.8\text{ V}$. The AC electrical specifications are the same for DDR1 and DDR2 SDRAM.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8323E when $Dn_GV_{DD}(\text{typ}) = 1.8\text{ V}$.

Table 12. DDR2 SDRAM DC Electrical Characteristics for $Dn_GV_{DD}(\text{typ}) = 1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	Dn_GV_{DD}	1.71	1.89	V	1
I/O reference voltage	$MVREF_{REF}$	$0.49 \times Dn_GV_{DD}$	$0.51 \times Dn_GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MVREF_{REF} - 0.04$	$MVREF_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MVREF_{REF} + 0.125$	$Dn_GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	−0.3	$MVREF_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	−9.9	9.9	μA	4
Output high current ($V_{OUT} = 1.35\text{ V}$)	I_{OH}	−13.4	—	mA	—
Output low current ($V_{OUT} = 0.280\text{ V}$)	I_{OL}	13.4	—	mA	—

Notes:

1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.
2. $MVREF_{REF}$ is expected to be equal to $0.5 \times Dn_GV_{DD}$, and to track Dn_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MVREF_{REF}$ may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to $MVREF_{REF}$. This rail should track variations in the DC level of $MVREF_{REF}$.
4. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq Dn_GV_{DD}$.

Table 13 provides the DDR2 capacitance when $Dn_GV_{DD}(\text{typ}) = 1.8\text{ V}$.

Table 13. DDR2 SDRAM Capacitance for $Dn_GV_{DD}(\text{typ}) = 1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR1 and DDR2 SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM ($Dn_GV_{DD}(typ) = 1.8\text{ V}$).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with Dn_GV_{DD} of $1.8 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MVREFn_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MVREFn_{REF} + 0.25$	—	V	—

Table 17 provides the input AC timing specifications for the DDR1 SDRAM ($Dn_GV_{DD}(typ) = 2.5\text{ V}$).

Table 17. DDR1 SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with Dn_GV_{DD} of $2.5 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MVREFn_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MVREFn_{REF} + 0.31$	—	V	—

Table 18 provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 18. DDR1 and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with Dn_GV_{DD} of $(1.8\text{ or }2.5\text{ V}) \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
266 MHz		–750	750		
200 MHz		–1250	1250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
RX_CLK clock fall time	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

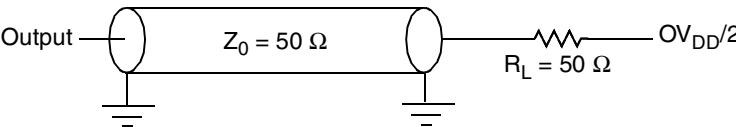


Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

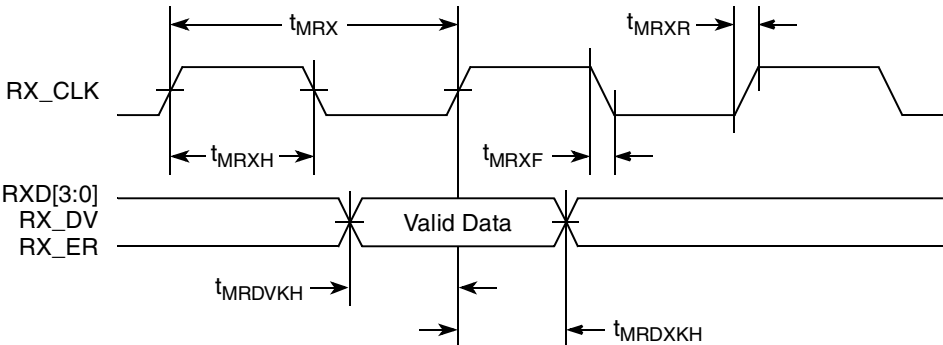


Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

Table 31. JTAG Interface DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	—	±5	μA

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E. [Table 32](#) provides the JTAG AC timing specifications as defined in [Figure 19](#) through [Figure 22](#).

Table 32. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see [Table 2](#)).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	11	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
\overline{TRST} assert time	t_{TRST}	25	—	ns	3
Input setup times:				ns	
Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 4	— —		4
Input hold times:				ns	
Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	10 10	— —		4
Valid times:				ns	
Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	2 2	15 15		5
Output hold times:				ns	
Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	2 2	— —		5

Table 32. JTAG AC Timing Specifications (Independent of CLKIN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	2	19		5, 6
TDO	t_{JTKLOZ}	2	9		6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVXH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDVXH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. \overline{TRST} is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK} .
5. Non-JTAG signal output timing with respect to t_{TCLK} .
6. Guaranteed by design and characterization.

Figure 18 provides the AC test load for TDO and the boundary-scan outputs of the MPC8323E.

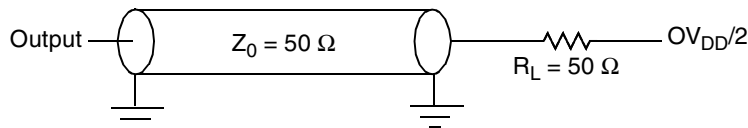

Figure 18. AC Test Load for the JTAG Interface

Figure 19 provides the JTAG clock input timing diagram.

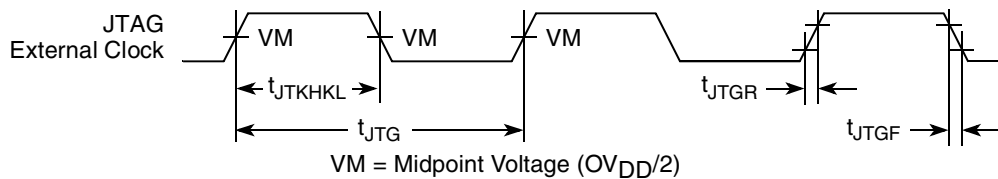

Figure 19. JTAG Clock Input Timing Diagram

Figure 20 provides the \overline{TRST} timing diagram.

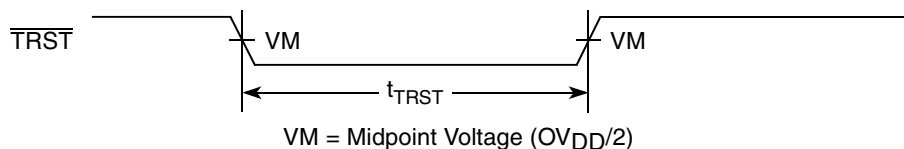

Figure 20. \overline{TRST} Timing Diagram

Table 37 shows the PCI AC timing specifications at 33 MHz.

Table 37. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 25 provides the AC test load for PCI.

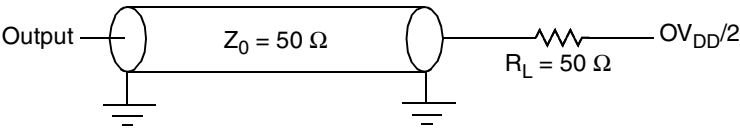


Figure 25. PCI AC Test Load

Figure 26 shows the PCI input AC timing conditions.

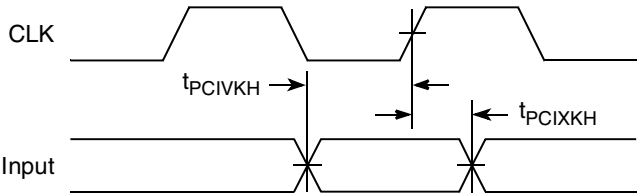


Figure 26. PCI Input AC Timing Measurement Conditions

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Table 44. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	$t_{NIKH OV}$	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	$t_{NEKH OV}$	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{NIKH OV}$ symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 30 provides the AC test load for the SPI.

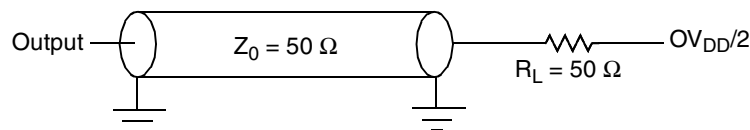


Figure 30. SPI AC Test Load

Table 46. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	—	±5	μA

17.2 TDM/SI AC Timing Specifications

Table 47 provides the TDM/SI input and output AC timing specifications.

Table 47. TDM/SI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	12	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 33 provides the AC test load for the TDM/SI.

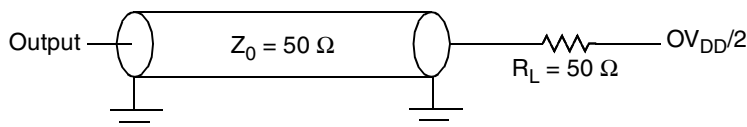
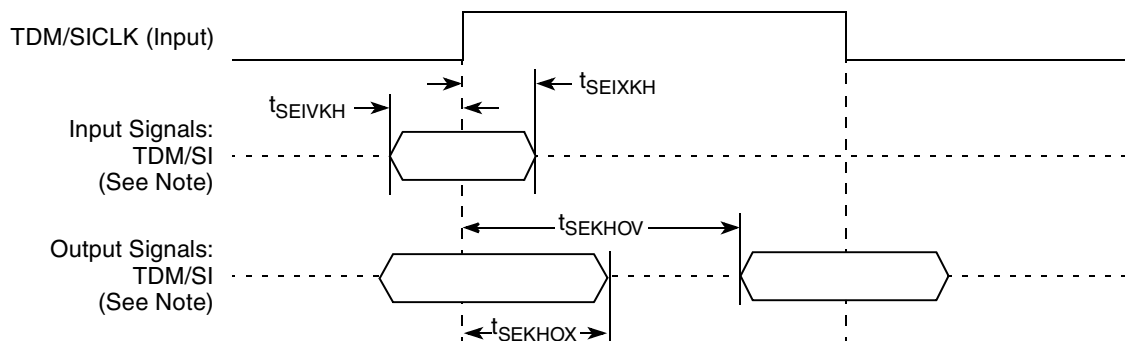

Figure 33. TDM/SI AC Test Load

Figure 34 represents the AC timing from Table 47. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on TDM/SI.

Figure 34. TDM/SI AC Timing (External Clock) Diagram

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications¹ (continued)

Characteristic	Symbol ²	Min	Max	Unit
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 52. Synchronous UART AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	5.5	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	10	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	5.5	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	8	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	4	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	0	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{UAIKHOX}$ symbolizes the outputs internal timing (UAI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 38 provides the AC test load.

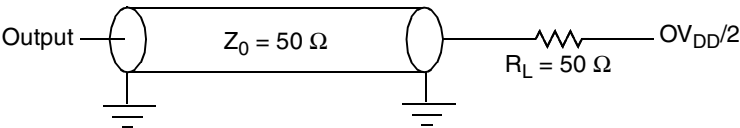
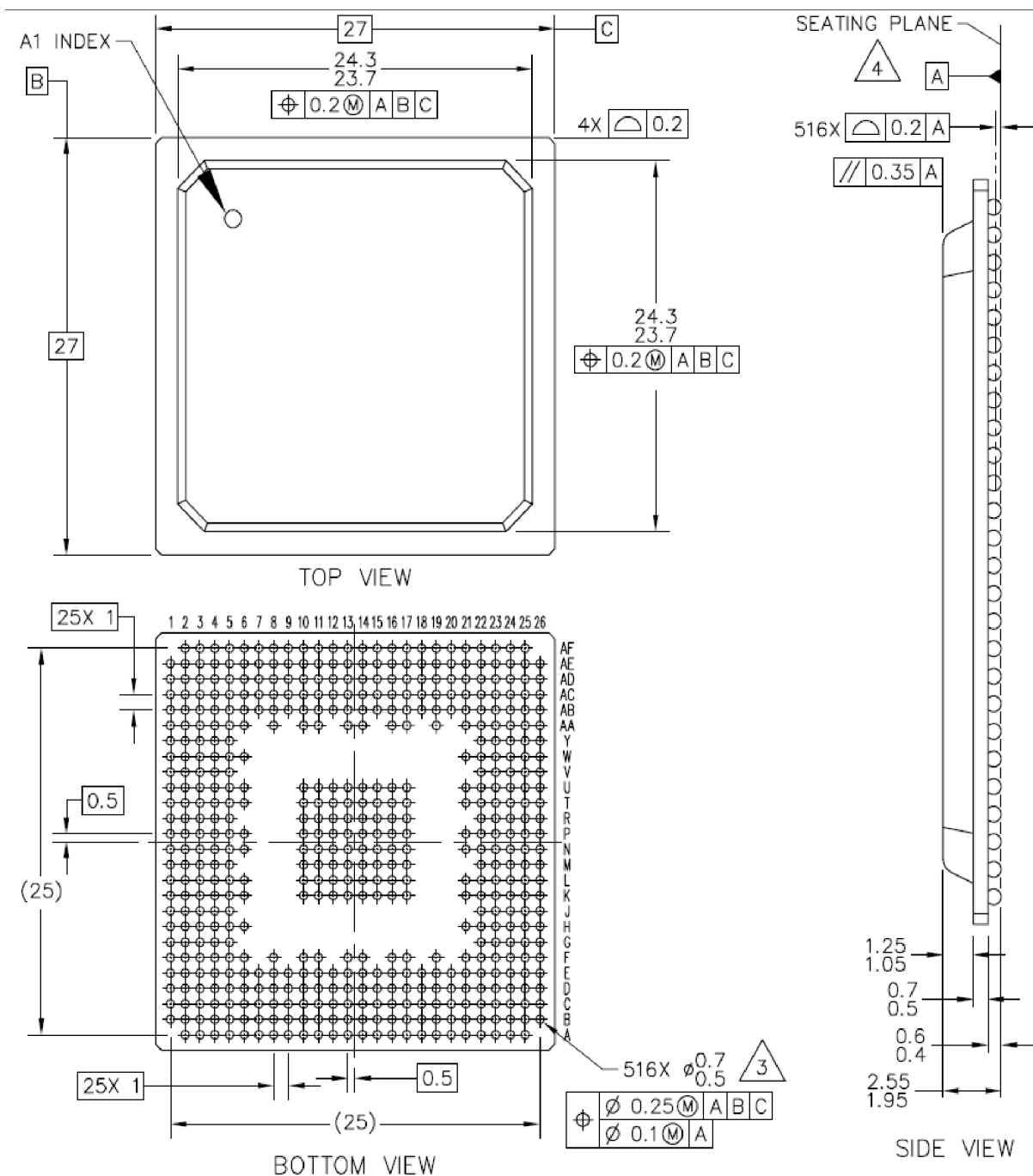


Figure 38. AC Test Load

Figure 39 and Figure 40 represent the AC timing from Table 51. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 42. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8323E PBGA

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	O	GV _{DD}	3
MEMC_MCK	AF14	O	GV _{DD}	—
MEMC_MCK	AE14	O	GV _{DD}	—
MEMC_MODT	AF11	O	GV _{DD}	—
Local Bus Controller Interface				
LAD0	N25	IO	OV _{DD}	7
LAD1	P26	IO	OV _{DD}	7
LAD2	P25	IO	OV _{DD}	7
LAD3	R26	IO	OV _{DD}	7
LAD4	R25	IO	OV _{DD}	7
LAD5	T26	IO	OV _{DD}	7
LAD6	T25	IO	OV _{DD}	7
LAD7	U25	IO	OV _{DD}	7
LAD8	M24	IO	OV _{DD}	7
LAD9	N24	IO	OV _{DD}	7
LAD10	P24	IO	OV _{DD}	7
LAD11	R24	IO	OV _{DD}	7
LAD12	T24	IO	OV _{DD}	7
LAD13	U24	IO	OV _{DD}	7
LAD14	U26	IO	OV _{DD}	7
LAD15	V26	IO	OV _{DD}	7
LA16	K25	O	OV _{DD}	7
LA17	L25	O	OV _{DD}	7
LA18	L26	O	OV _{DD}	7
LA19	L24	O	OV _{DD}	7
LA20	M26	O	OV _{DD}	7
LA21	M25	O	OV _{DD}	7
LA22	N26	O	OV _{DD}	7
LA23	AC24	O	OV _{DD}	7
LA24	AC25	O	OV _{DD}	7
LA25	AB23	O	OV _{DD}	7
LCS0	AB24	O	OV _{DD}	4

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PA26/Enet2_RX_ER/SER2_CD/TDMB_REQ/LA10 (LBIU)	E26	IO	OV _{DD}	—
GPIO_PA27/Enet2_TX_ER/TDMB_CLKO/LA11 (LBIU)	F25	IO	OV _{DD}	—
GPIO_PA28/Enet2_RX_DV/SER2_CTS/TDMB_RSYNC/LA12 (LBIU)	E25	IO	OV _{DD}	—
GPIO_PA29/Enet2_COL/RXD[4]/SER2_RXD[4]/TDMB_STROBE/LA13 (LBIU)	J25	IO	OV _{DD}	—
GPIO_PA30/Enet2_TX_EN/SER2_RTS/TDMB_TSYNC/LA14 (LBIU)	F26	IO	OV _{DD}	—
GPIO_PA31/Enet2_CRS/SDET LA15 (LBIU)	J26	IO	OV _{DD}	—
GPIO_PB0/Enet3_TXD[0]/SER3_TXD[0]/TDMC_TXD[0]	A13	IO	OV _{DD}	—
GPIO_PB1/Enet3_TXD[1]/SER3_TXD[1]/TDMC_TXD[1]	B13	IO	OV _{DD}	—
GPIO_PB2/Enet3_TXD[2]/SER3_TXD[2]/TDMC_TXD[2]	A14	IO	OV _{DD}	—
GPIO_PB3/Enet3_TXD[3]/SER3_TXD[3]/TDMC_TXD[3]	B14	IO	OV _{DD}	—
GPIO_PB4/Enet3_RXD[0]/SER3_RXD[0]/TDMC_RXD[0]	B8	IO	OV _{DD}	—
GPIO_PB5/Enet3_RXD[1]/SER3_RXD[1]/TDMC_RXD[1]	A8	IO	OV _{DD}	—
GPIO_PB6/Enet3_RXD[2]/SER3_RXD[2]/TDMC_RXD[2]	A9	IO	OV _{DD}	—
GPIO_PB7/Enet3_RXD[3]/SER3_RXD[3]/TDMC_RXD[3]	B9	IO	OV _{DD}	—
GPIO_PB8/Enet3_RX_ER/SER3_CD/TDMC_REQ	A11	IO	OV _{DD}	—
GPIO_PB9/Enet3_TX_ER/TDMC_CLKO	B11	IO	OV _{DD}	—
GPIO_PB10/Enet3_RX_DV/SER3_CTS/TDMC_RSYNC	A10	IO	OV _{DD}	—
GPIO_PB11/Enet3_COL/RXD[4]/SER3_RXD[4]/TDMC_STROBE	A15	IO	OV _{DD}	—
GPIO_PB12/Enet3_TX_EN/SER3_RTS/TDMC_TSYNC	B12	IO	OV _{DD}	—
GPIO_PB13/Enet3_CRS/SDET	B15	IO	OV _{DD}	—
GPIO_PB14/CLK12	D9	IO	OV _{DD}	—
GPIO_PB15 UPC1_TxADDR[4]	D14	IO	OV _{DD}	—
GPIO_PB16 UPC1_RxADDR[4]	B16	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PB17/BRGO1/CE_EXT_REQ1	D10	IO	OV _{DD}	—
GPIO_PB18/Enet4_TXD[0]/SER4_TXD[0]/TDMD_TXD[0]	C10	IO	OV _{DD}	—
GPIO_PB19/Enet4_TXD[1]/SER4_TXD[1]/TDMD_TXD[1]	C9	IO	OV _{DD}	—
GPIO_PB20/Enet4_TXD[2]/SER4_TXD[2]/TDMD_TXD[2]	D8	IO	OV _{DD}	—
GPIO_PB21/Enet4_TXD[3]/SER4_TXD[3]/TDMD_TXD[3]	C8	IO	OV _{DD}	—
GPIO_PB22/Enet4_RXD[0]/SER4_RXD[0]/TDMD_RXD[0]	C15	IO	OV _{DD}	—
GPIO_PB23/Enet4_RXD[1]/SER4_RXD[1]/TDMD_RXD[1]	C14	IO	OV _{DD}	—
GPIO_PB24/Enet4_RXD[2]/SER4_RXD[2]/TDMD_RXD[2]	D13	IO	OV _{DD}	—
GPIO_PB25/Enet4_RXD[3]/SER4_RXD[3]/TDMD_RXD[3]	C13	IO	OV _{DD}	—
GPIO_PB26/Enet4_RX_ER/SER4_CD/TDMD_REQ	C12	IO	OV _{DD}	—
GPIO_PB27/Enet4_TX_ER/TDMD_CLKO	D11	IO	OV _{DD}	—
GPIO_PB28/Enet4_RX_DV/SER4_CTS/TDMD_RSYNC	D12	IO	OV _{DD}	—
GPIO_PB29/Enet4_COL/RXD[4]/SER4_RXD[4]/TDMD_STROBE	D7	IO	OV _{DD}	—
GPIO_PB30/Enet4_TX_EN/SER4_RTS/TDMD_TSYNC	C11	IO	OV _{DD}	—
GPIO_PB31/Enet4_CRS/SDET	C7	IO	OV _{DD}	—
GPIO_PC0/UPC1_TxDATA[0]/SER5_TXD[0]	A18	IO	OV _{DD}	—
GPIO_PC1/UPC1_TxDATA[1]/SER5_TXD[1]	A19	IO	OV _{DD}	—
GPIO_PC2/UPC1_TxDATA[2]/SER5_TXD[2]	B18	IO	OV _{DD}	—
GPIO_PC3/UPC1_TxDATA[3]/SER5_TXD[3]	B19	IO	OV _{DD}	—
GPIO_PC4/UPC1_TxDATA[4]	A24	IO	OV _{DD}	—
GPIO_PC5/UPC1_TxDATA[5]	B24	IO	OV _{DD}	—
GPIO_PC6/UPC1_TxDATA[6]	A23	IO	OV _{DD}	—
GPIO_PC7/UPC1_TxDATA[7]	B26	IO	OV _{DD}	—
GPIO_PC8/UPC1_RxDATA[0]/SER5_RXD[0]	A21	IO	OV _{DD}	—
GPIO_PC9/UPC1_RxDATA[1]/SER5_RXD[1]	B20	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PD10/GTM1_TIN2/GTM2_TIN1/CLK17	J24	IO	OV _{DD}	—
GPIO_PD11/GTM1_TGATE2/GTM2_TGATE1	B25	IO	OV _{DD}	—
GPIO_PD12/GTM1_TOUT2/GTM2_TOUT1	C4	IO	OV _{DD}	—
GPIO_PD13/GTM1_TIN3/GTM2_TIN4/BRGO8	D4	IO	OV _{DD}	—
GPIO_PD14/GTM1_TGATE3/GTM2_TGATE4	D5	IO	OV _{DD}	—
GPIO_PD15/GTM1_TOUT3	A5	IO	OV _{DD}	—
GPIO_PD16/GTM1_TIN4/GTM2_TIN3	B5	IO	OV _{DD}	—
GPIO_PD17/GTM1_TGATE4/GTM2_TGATE3	C5	IO	OV _{DD}	—
GPIO_PD18/GTM1_TOUT4/GTM2_TOUT3	A6	IO	OV _{DD}	—
GPIO_PD19/CE_RISC1_INT/CE_EXT_REQ4	B6	IO	OV _{DD}	—
GPIO_PD20/CLK18/BRGO6	D21	IO	OV _{DD}	—
GPIO_PD21/CLK16/BRGO5/UPC1_CLKO	C19	IO	OV _{DD}	—
GPIO_PD22/CLK4/BRGO9/UCC2_CLKO	A7	IO	OV _{DD}	—
GPIO_PD23/CLK3/BRGO10/UCC3_CLKO	B7	IO	OV _{DD}	—
GPIO_PD24/CLK10/BRGO2/UCC4_CLKO	A12	IO	OV _{DD}	—
GPIO_PD25/CLK13/BRGO16/UCC5_CLKO	B10	IO	OV _{DD}	—
GPIO_PD26/CLK2/BRGO4/UCC1_CLKO	E4	IO	OV _{DD}	—
GPIO_PD27/CLK1/BRGO3	F4	IO	OV _{DD}	—
GPIO_PD28/CLK19/BRGO11	D15	IO	OV _{DD}	—
GPIO_PD29/CLK15/BRGO8	C6	IO	OV _{DD}	—
GPIO_PD30/CLK14	D6	IO	OV _{DD}	—
GPIO_PD31/CLK7/BRGO15	E24	IO	OV _{DD}	—
Power and Ground Supplies				
GV _{DD}	AA8, AA10, AA11, AA13, AA14, AA16, AA17, AA19, AA21, AB9, AB10, AB11, AB12, AB14, AB18, AB20, AB21, AC6, AC8, AC14, AC18	GV _{DD}	—	—
OV _{DD}	E5, E6, E8, E9, E10, E12, E14, E15, E16, E18, E19, E20, E22, F5, F6, F8, F10, F14, F16, F19, F22, G22, H5, H6, H21, J5, J22, K21, K22, L5, L6, L22, M5, M22, N5, N21, N22, P6, P22, P23, R5, R23, T5, T21, T22, U6, U22, V5, V22, W22, Y5, AB5, AB6, AC5	OV _{DD}	—	—

shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 59. CSB Frequency Options

CFG_CLKIN_DIV_B at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	Input Clock Frequency (MHz) ²		
			25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)		
High	0010	2 : 1			133
High	0011	3 : 1		100	
High	0100	4 : 1	100	133	
High	0101	5 : 1	125		
High	0110	6 : 1			
High	0111	7 : 1			
High	1000	8 : 1			
High	1001	9 : 1			
High	1010	10 : 1			
High	1011	11 : 1			
High	1100	12 : 1			
High	1101	13 : 1			
High	1110	14 : 1			
High	1111	15 : 1			
High	0000	16 : 1			
Low	0010	2 : 1			133
Low	0011	3 : 1		100	
Low	0100	4 : 1		133	
Low	0101	5 : 1			
Low	0110	6 : 1			
Low	0111	7 : 1			
Low	1000	8 : 1			
Low	1001	9 : 1			
Low	1010	10 : 1			
Low	1011	11 : 1			
Low	1100	12 : 1			
Low	1101	13 : 1			
Low	1110	14 : 1			
Low	1111	15 : 1			
Low	0000	16 : 1			

¹ CFG_CLKIN_DIV_B is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV_B must be pulled up (high) in agent mode.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

24.7 Pull-Up Resistor Requirements

The MPC8323E requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins including I²C pins, Ethernet Management MDIO pin, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see AN3361, “MPC8321E/MPC8323E PowerQUICC Design Checklist,” Rev. 1.

25 Ordering Information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in [Section 25.1, “Part Numbers Fully Addressed by This Document.”](#)

25.1 Part Numbers Fully Addressed by This Document

[Table 66](#) provides the Freescale part numbering nomenclature for the MPC8323E family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

Table 66. Part Numbering Nomenclature

MPC	nnnn	E	C	VR	AF	D	C	A
Product Code	Part Identifier	Encryption Acceleration	Temperature Range ¹	Package ²	e300 Core Frequency ³	DDR Frequency	QUICC Engine Frequency	Revision Level
MPC	8323	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	VR = Pb-free PBGA ZQ = Pb PBGA	AD = 266 MHz AF = 333 MHz	D = 266 MHz	C = 200 MHz	Contact local Freescale sales office

Notes:

1. Contact local Freescale office on availability of parts with C temperature range.
2. See [Section 21, “Package and Pin Listings,”](#) for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

25.2 Part Marking

Parts are marked as in the example shown in [Figure 46](#).

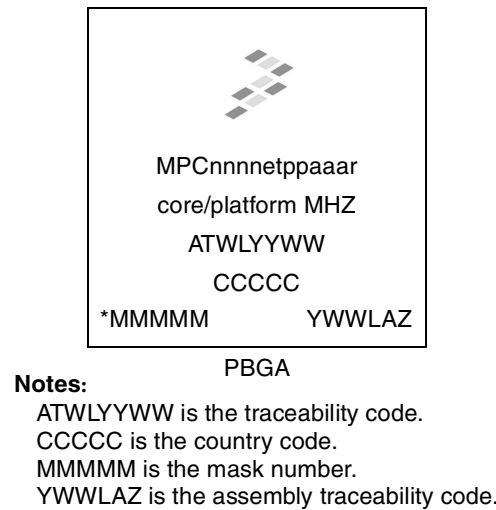


Figure 46. Freescale Part Marking for PBGA Devices

26 Document Revision History

[Table 67](#) provides a revision history for this hardware specification.

Table 67. Document Revision History

Rev. No.	Date	Substantive Change(s)
4	09/2010	<ul style="list-style-type: none"> Replaced all instances of "LCCR" with "LCRR" throughout. Added footnotes 3 and 4 in Table 2, "Recommended Operating Conditions³." Modified Section 8.1.1, "DC Electrical Characteristics." Modified Table 23, "MII Transmit AC Timing Specifications." Modified Table 24, "MII Receive AC Timing Specifications." Added footnote 7 and 8, and modified some signal names in Table 55, "MPC8323E PBGA Pinout Listing."
3	12/2009	<ul style="list-style-type: none"> Removed references for note 4 from Table 1. Added Figure 2 in Section 2.1.2, "Power Supply Voltage Specification." Added symbol T_A in Table 2. Added footnote 2 in Table 2. Added a note in Section 4, "Clock Input Timing" for rise/fall time of QE input pins. Modified CLKIN, PCI_CLK rise/fall time parameters in Table 8. Modified min value of t_{MCK} in Table 19. Modified Figure 43. Modified formula for ce_clk calculation in Section 22.3, "System Clock Domains." Added a note in Section 22.4, "System PLL Configuration." Removed the signal ECID_TMODE_IN from Table 55. Removed all references of RST signals from Table 55.