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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8321evrafdc

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8323E. The MPC8323E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DDn}	–0.3 to 1.26	V	—
DDR1 and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
PCI, local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.6	V	—
Input voltage	DDR1/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2
	DDR1/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2
	Local bus, DUART, CLKIN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	5
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV_{DD} = 3.3 V
PCI signals	25	
DDR1 signal	18	GV_{DD} = 2.5 V
DDR2 signal	18	GV_{DD} = 1.8 V
DUART, system control, I2C, SPI, JTAG	42	OV_{DD} = 3.3 V
GPIO signals	42	OV_{DD} = 3.3 V

2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input capacitance for all pins except CLKIN	C_I	6	8	pF	—
Input capacitance for CLKIN	C_{ICLKIN}	10	—	pF	1

Note:
1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and IO supply voltages (GV_{DD} and OV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD} and OV_{DD}) do not have any ordering requirements with respect to one another.

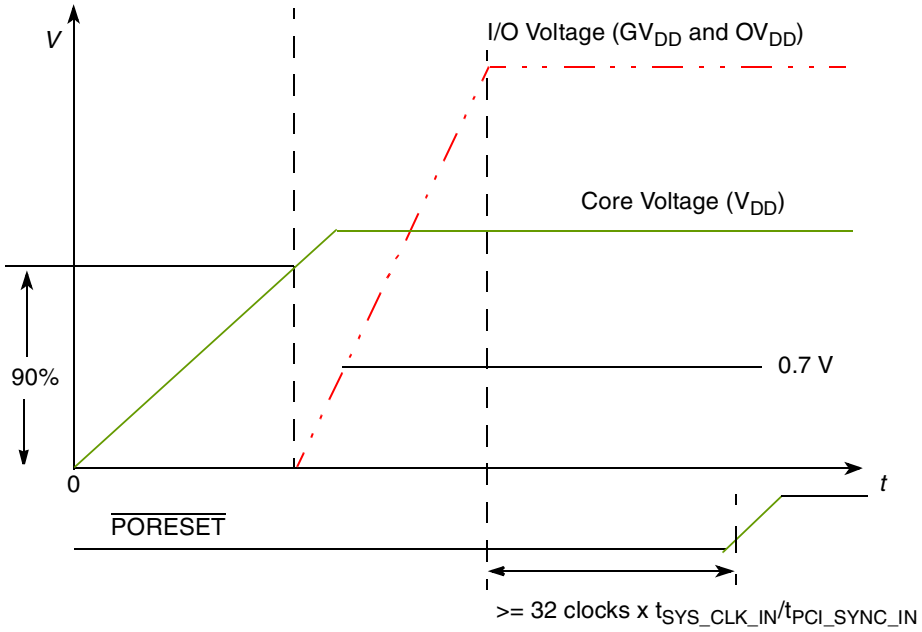

Figure 3. MPC8323E Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation for this family of MPC8323E devices is shown in Table 5.

Table 5. MPC8323E Power Dissipation

CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Core Frequency (MHz)	Typical	Maximum	Unit	Notes
133	200	266	0.74	1.48	W	1, 2, 3
133	200	333	0.78	1.62	W	1, 2, 3

Notes:
1. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a nominal voltage of V_{DD} = 1.0 V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the MPC8323MDS evaluation board using WC process silicon.
3. Maximum power is based on a voltage of V_{DD} = 1.07 V, WC process, a junction T_J = 110°C, and an artificial smoke test.

Table 6 shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V R_s = 20 Ω R_t = 50 Ω 1 pair of clocks	266 MHz, 1 × 32 bits	0.212	0.367	—	W	—

Table 23. MII Transmit AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK data clock fall time	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 7 shows the MII transmit AC timing diagram.

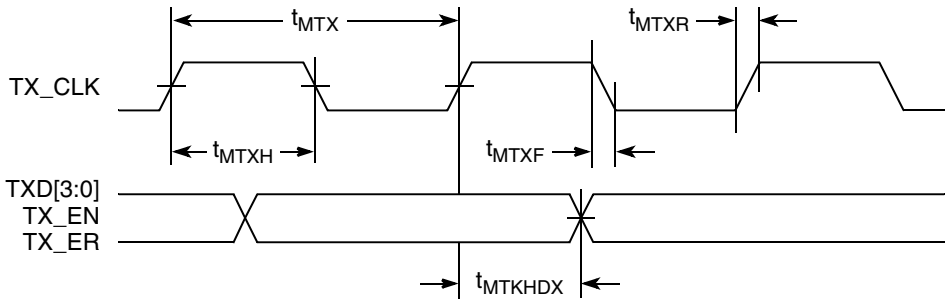

Figure 7. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time	t_{MRXR}	1.0	—	4.0	ns

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock fall time	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

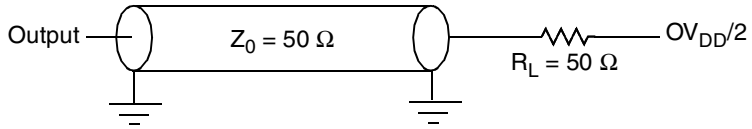

Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

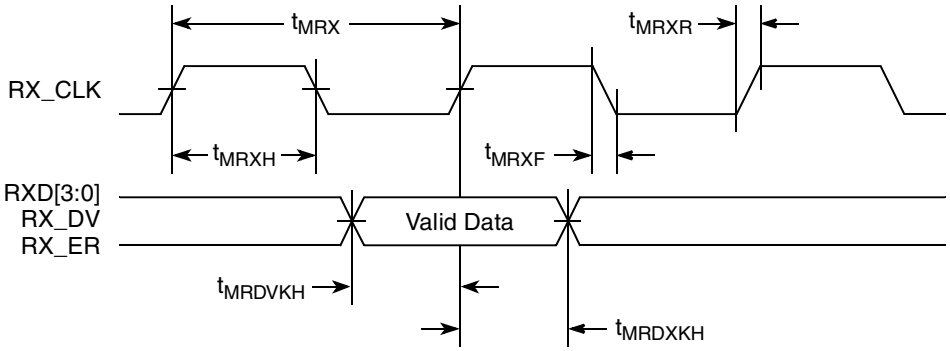

Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

Table 32. JTAG AC Timing Specifications (Independent of CLKIN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	 5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 18 provides the AC test load for TDO and the boundary-scan outputs of the MPC8323E.

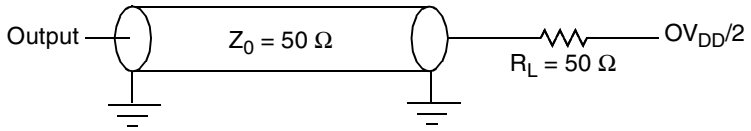

Figure 18. AC Test Load for the JTAG Interface

Figure 19 provides the JTAG clock input timing diagram.

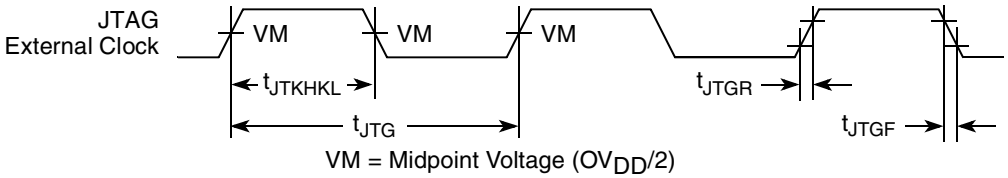

Figure 19. JTAG Clock Input Timing Diagram

Figure 20 provides the $\overline{\text{TRST}}$ timing diagram.

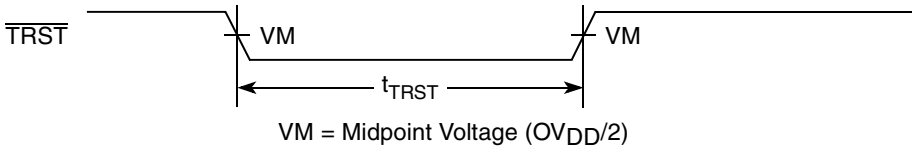

Figure 20. $\overline{\text{TRST}}$ Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

Table 33. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I²C interface of the MPC8323E.

Table 34. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0[2]	— 0.9[3]	μs

Table 34. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol[1]	Min	Max	Unit
Rise time of both SDA and SCL signals	t_{I2CR}	20 + 0.1 C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_b[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8323E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

Figure 23 provides the AC test load for the I²C.

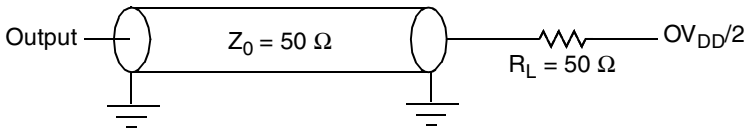

Figure 23. I²C AC Test Load

Figure 24 shows the AC timing diagram for the I²C bus.

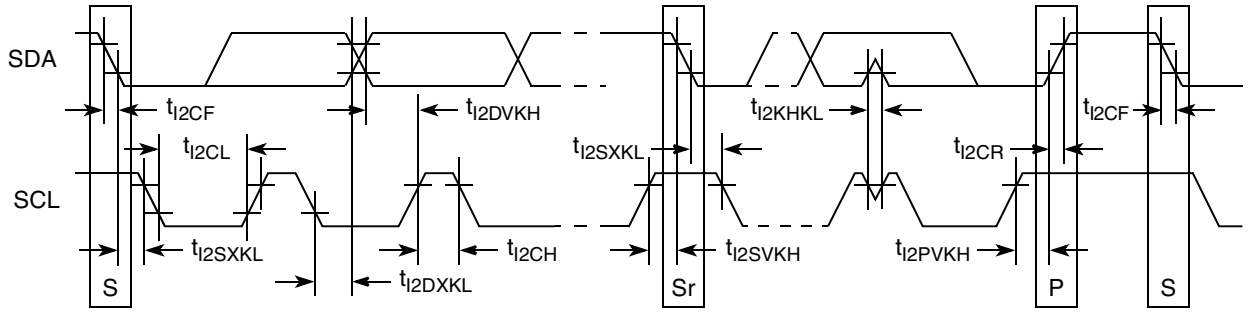

Figure 24. I²C Bus AC Timing Diagram

Figure 29 provides the AC test load for the GPIO.

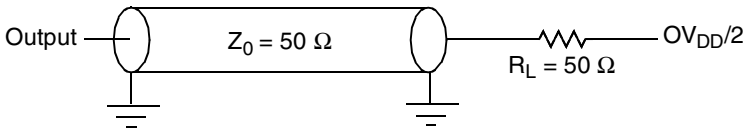

Figure 29. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8323E.

15.1 IPIC DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the external interrupt pins of the MPC8323E.

Table 42. IPIC DC Electrical Characteristics[1,2]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

15.2 IPIC AC Timing Specifications

Table 43 provides the IPIC input and output AC timing specifications.

Table 43. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Table 44. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 30 provides the AC test load for the SPI.

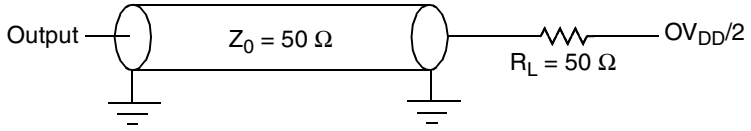

Figure 30. SPI AC Test Load

19 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART of the MPC8323E.

19.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Table 50 provides the DC electrical characteristics for the MPC8323E HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 50. HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

19.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Table 51 provides the input and output AC timing specifications for HDLC, BISYNC, and transparent UART protocols.

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	5.5	ns
Outputs—External clock delay	t_{HEKHOV}	1	10	ns
Outputs—Internal clock high impedance	t_{HIKHOX}	0	5.5	ns
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 52. Synchronous UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	5.5	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	10	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	5.5	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	8	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	4	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	0	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{UAIKHOX}$ symbolizes the outputs internal timing (UAI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 38 provides the AC test load.

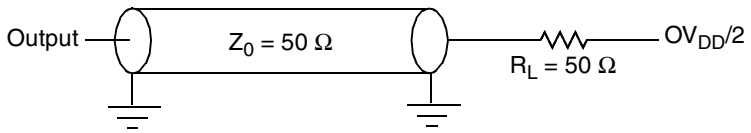

Figure 38. AC Test Load

Figure 39 and Figure 40 represent the AC timing from Table 51. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

Table 55. MPC8323E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	AE9	IO	GV_{DD}	—
MEMC_MDQ1	AD10	IO	GV_{DD}	—
MEMC_MDQ2	AF10	IO	GV_{DD}	—
MEMC_MDQ3	AF9	IO	GV_{DD}	—
MEMC_MDQ4	AF7	IO	GV_{DD}	—
MEMC_MDQ5	AE10	IO	GV_{DD}	—
MEMC_MDQ6	AD9	IO	GV_{DD}	—
MEMC_MDQ7	AF8	IO	GV_{DD}	—
MEMC_MDQ8	AE6	IO	GV_{DD}	—
MEMC_MDQ9	AD7	IO	GV_{DD}	—
MEMC_MDQ10	AF6	IO	GV_{DD}	—
MEMC_MDQ11	AC7	IO	GV_{DD}	—
MEMC_MDQ12	AD8	IO	GV_{DD}	—
MEMC_MDQ13	AE7	IO	GV_{DD}	—
MEMC_MDQ14	AD6	IO	GV_{DD}	—
MEMC_MDQ15	AF5	IO	GV_{DD}	—
MEMC_MDQ16	AD18	IO	GV_{DD}	—
MEMC_MDQ17	AE19	IO	GV_{DD}	—
MEMC_MDQ18	AF17	IO	GV_{DD}	—
MEMC_MDQ19	AF19	IO	GV_{DD}	—
MEMC_MDQ20	AF18	IO	GV_{DD}	—
MEMC_MDQ21	AE18	IO	GV_{DD}	—
MEMC_MDQ22	AF20	IO	GV_{DD}	—
MEMC_MDQ23	AD19	IO	GV_{DD}	—
MEMC_MDQ24	AD21	IO	GV_{DD}	—
MEMC_MDQ25	AF22	IO	GV_{DD}	—
MEMC_MDQ26	AC21	IO	GV_{DD}	—
MEMC_MDQ27	AF21	IO	GV_{DD}	—
MEMC_MDQ28	AE21	IO	GV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MDQ29	AD20	IO	GV_{DD}	—
MEMC_MDQ30	AF23	IO	GV_{DD}	—
MEMC_MDQ31	AD22	IO	GV_{DD}	—
MEMC_MDM0	AC9	O	GV_{DD}	—
MEMC_MDM1	AD5	O	GV_{DD}	—
MEMC_MDM2	AE20	O	GV_{DD}	—
MEMC_MDM3	AE22	O	GV_{DD}	—
MEMC_MDQS0	AE8	IO	GV_{DD}	—
MEMC_MDQS1	AE5	IO	GV_{DD}	—
MEMC_MDQS2	AC19	IO	GV_{DD}	—
MEMC_MDQS3	AE23	IO	GV_{DD}	—
MEMC_MBA0	AD16	O	GV_{DD}	—
MEMC_MBA1	AD17	O	GV_{DD}	—
MEMC_MBA2	AE17	O	GV_{DD}	—
MEMC_MA0	AD12	O	GV_{DD}	—
MEMC_MA1	AE12	O	GV_{DD}	—
MEMC_MA2	AF12	O	GV_{DD}	—
MEMC_MA3	AC13	O	GV_{DD}	—
MEMC_MA4	AD13	O	GV_{DD}	—
MEMC_MA5	AE13	O	GV_{DD}	—
MEMC_MA6	AF13	O	GV_{DD}	—
MEMC_MA7	AC15	O	GV_{DD}	—
MEMC_MA8	AD15	O	GV_{DD}	—
MEMC_MA9	AE15	O	GV_{DD}	—
MEMC_MA10	AF15	O	GV_{DD}	—
MEMC_MA11	AE16	O	GV_{DD}	—
MEMC_MA12	AF16	O	GV_{DD}	—
MEMC_MA13	AB16	O	GV_{DD}	—
$\overline{\text{MEMC\_MWE}}$	AC17	O	GV_{DD}	—
$\overline{\text{MEMC\_MRAS}}$	AE11	O	GV_{DD}	—
$\overline{\text{MEMC\_MCAS}}$	AD11	O	GV_{DD}	—
$\overline{\text{MEMC\_MCS}}$	AC11	O	GV_{DD}	—

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

When CLKIN is the primary input clock,

ce_clk = (primary clock input × CEPMF) ÷ (1 + CEPDF)

When PCI_CLK is the primary input clock,

ce_clk = [primary clock input × CEPMF × (1 + ~CFG_CLKIN_DIV)] ÷ (1 + CEPDF)

See the "QUICC Engine PLL Multiplication Factor" section and the "QUICC Engine PLL Division Factor" section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

The DDR SDRAM memory controller operates with a frequency equal to twice the frequency of *csb_clk*. Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The local bus memory controller operates with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBC clock divider ratio is controlled by LCRR[CLKDIV]. See the "LBC Bus Clock and Clock Ratios" section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 56 specifies which units have a configurable clock frequency. Refer to the "System Clock Control Register (SCCR)" section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for a detailed description.

Table 56. Configurable Clock Units

Unit	Default Frequency	Options
Security core, I2C, SAP, TPR	*csb_clk*	Off, *csb_clk*/2, *csb_clk*/3
PCI and DMA complex	*csb_clk*	Off, *csb_clk*

NOTE

Setting the clock ratio of these units must be performed prior to any access to them.

Table 57 provides the operating frequencies for the 8323E PBGA under recommended operating conditions (see Table 2).

Table 57. Operating Frequencies for PBGA

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	333	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
QUICC Engine frequency (*ce_clk*)	200	MHz

22.7 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8323E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 63 shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

Table 63. Suggested PLL Configurations

Conf No.	SPMF	Core PLL	CEMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0110	0	33.33	133.33	266.66	200
2	0100	0000101	1000	0	25	100	250	200
3	0010	0000100	0011	0	66.67	133.33	266.66	200
4	0100	0000101	0110	0	33.33	133.33	333.33	200
5	0101	0000101	1000	0	25	125	312.5	200
6	0010	0000101	0011	0	66.67	133.33	333.33	200

23 Thermal

This section describes the thermal specifications of the MPC8323E.

23.1 Thermal Characteristics

Table 64 provides the package thermal characteristics for the 516 27×27 mm PBGA of the MPC8323E.

Table 64. Package Thermal Characteristics for PBGA

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	21	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	23	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	13	°C/W	4
Junction-to-case	—	$R_{\theta JC}$	9	°C/W	5

interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_C = case temperature of the package (°C)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
P_D = power dissipation (W)

24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8323E.

24.1 System Clocking

The MPC8323E includes three PLLs.

- The system PLL ($AV_{DD}2$) generates the system clock from the externally supplied CLKIN input. The frequency ratio between the system and CLKIN is selected using the system PLL ratio configuration bits as described in Section 22.4, “System PLL Configuration.”
- The e300 core PLL ($AV_{DD}3$) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in Section 22.5, “Core PLL Configuration.”
- The QUICC Engine PLL ($AV_{DD}1$) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each $AV_{DD}n$ pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 44, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 44 shows the PLL power supply filter circuit.

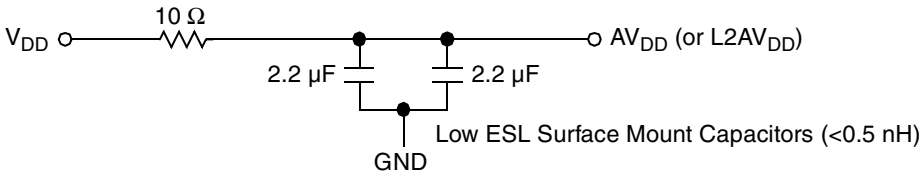

Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8323E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8323E system, and the MPC8323E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pins of the MPC8323E. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, or GV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, OV_{DD}, and GND pins of the MPC8323E.

24.5 Output Buffer DC Impedance

The MPC8323E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The

output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

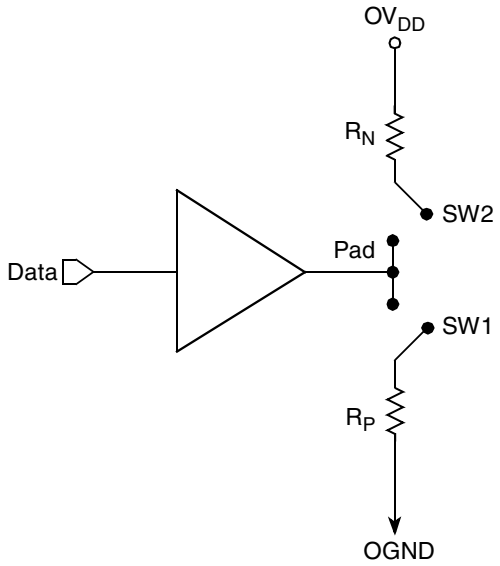

Figure 45. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 65 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 65. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

24.6 Configuration Pin Multiplexing

The MPC8323E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

24.7 Pull-Up Resistor Requirements

The MPC8323E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins, Ethernet Management MDIO pin, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see AN3361, “MPC8321E/MPC8323E PowerQUICC Design Checklist,” Rev. 1.

25 Ordering Information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 25.1, “Part Numbers Fully Addressed by This Document.”

25.1 Part Numbers Fully Addressed by This Document

Table 66 provides the Freescale part numbering nomenclature for the MPC8323E family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

Table 66. Part Numbering Nomenclature

MPC	*nnnn*	*E*	*C*	*VR*	*AF*	*D*	*C*	*A*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range[1]**	**Package[2]**	**e300 Core Frequency[3]**	**DDR Frequency**	**QUICC Engine Frequency**	**Revision Level**
MPC	8323	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	VR = Pb-free PBGA ZQ = Pb PBGA	AD = 266 MHz AF = 333 MHz	D = 266 MHz	C = 200 MHz	Contact local Freescale sales office

Notes:
1. Contact local Freescale office on availability of parts with C temperature range.
2. See Section 21, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.