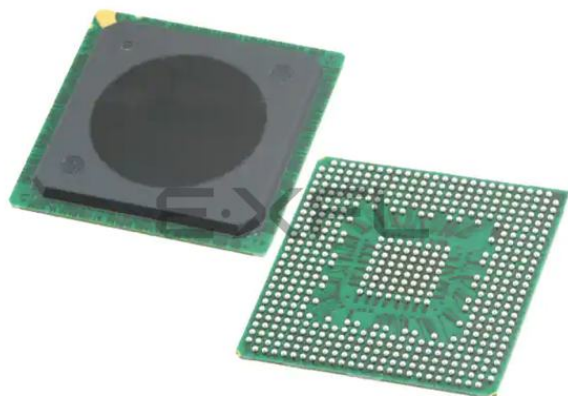




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8321vrafdc

NOTE

The QUICC Engine block can also support a UTOPIA level 2 capable of supporting 31 multi-PHY (MPC8323E- and MPC8323-specific).

The MPC8323E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In summary, the MPC8323E family provides users with a highly integrated, fully programmable communications processor. This helps ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

1.1 MPC8323E Features

Major features of the MPC8323E are as follows:

- High-performance, low-power, and cost-effective single-chip data-plane/control-plane solution for ATM or IP/Ethernet packet processing (or both).
- MPC8323E QUICC Engine block offers a future-proof solution for next generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards.
- Single platform architecture supports the convergence of IP packet networks and ATM networks.
- DDR1/DDR2 memory controller—one 32-bit interface at up to 266 MHz supporting both DDR1 and DDR2.
- An e300c2 core built on Power Architecture technology with 16-Kbyte instruction and data caches, and dual integer units.
- Peripheral interfaces such as 32-bit PCI (2.2) interface up to 66-MHz operation, 16-bit local bus interface up to 66-MHz operation, and USB 2.0 (full-/low-speed).
- Security engine provides acceleration for control and data plane security protocols.
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration.

1.1.1 Protocols

The protocols are as follows:

- ATM SAR up to 155 Mbps (OC-3) full duplex, with ATM traffic shaping (ATF TM4.1)
- Support for ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- Support for IMA and ATM transmission convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- Support for 64 channels of HDLC/transparent

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	$OV_{DD} = 3.3\text{ V}$
PCI signals	25	
DDR1 signal	18	$GV_{DD} = 2.5\text{ V}$
DDR2 signal	18	$GV_{DD} = 1.8\text{ V}$
DUART, system control, I2C, SPI, JTAG	42	$OV_{DD} = 3.3\text{ V}$
GPIO signals	42	$OV_{DD} = 3.3\text{ V}$

2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input capacitance for all pins except CLKIN	C_I	6	8	pF	—
Input capacitance for CLKIN	$C_{I\text{CLKIN}}$	10	—	pF	1

Note:

1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and IO supply voltages (GV_{DD} and OV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD} and OV_{DD}) do not have any ordering requirements with respect to one another.

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
$\overline{\text{HRESET}}/\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

1. $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is in PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{\text{OH}} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$\text{OV}_{\text{DD}} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—

Table 13. DDR2 SDRAM Capacitance for $Dn_GV_{DD}(typ) = 1.8\text{ V}$

Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1
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Note:

1. This parameter is sampled. $Dn_GV_{DD} = 1.8\text{ V} \pm 0.090\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$, $V_{OUT} = Dn_GV_{DD} \div 2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR1 SDRAM component(s) of the MPC8323E when $Dn_GV_{DD}(typ) = 2.5\text{ V}$.

Table 14. DDR1 SDRAM DC Electrical Characteristics for $Dn_GV_{DD}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	Dn_GV_{DD}	2.375	2.625	V	1
I/O reference voltage	$MVREFn_{REF}$	$0.49 \times Dn_GV_{DD}$	$0.51 \times Dn_GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MVREFn_{REF} - 0.04$	$MVREFn_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MVREFn_{REF} + 0.15$	$Dn_GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MVREFn_{REF} - 0.15$	V	—
Output leakage current	I_{OZ}	-9.9	-9.9	μA	4
Output high current ($V_{OUT} = 1.95\text{ V}$)	I_{OH}	-16.2	—	mA	—
Output low current ($V_{OUT} = 0.35\text{ V}$)	I_{OL}	16.2	—	mA	—

Notes:

1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.
2. $MVREFn_{REF}$ is expected to be equal to $0.5 \times Dn_GV_{DD}$, and to track Dn_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MVREFn_{REF}$ may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to $MVREFn_{REF}$. This rail should track variations in the DC level of $MVREFn_{REF}$.
4. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq Dn_GV_{DD}$.

Table 15 provides the DDR1 capacitance $Dn_GV_{DD}(typ) = 2.5\text{ V}$.

Table 15. DDR1 SDRAM Capacitance for $Dn_GV_{DD}(typ) = 2.5\text{ V}$ Interface

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ,DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 2.5\text{ V} \pm 0.125\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$, $V_{OUT} = Dn_GV_{DD} \div 2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
RX_CLK clock fall time	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

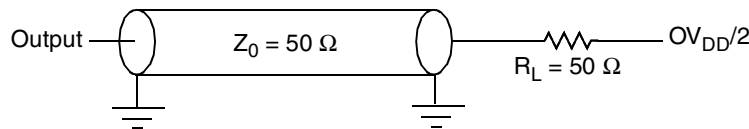


Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

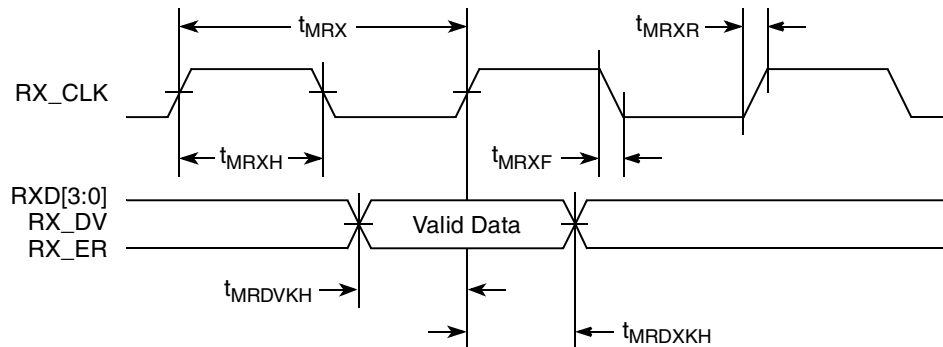


Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

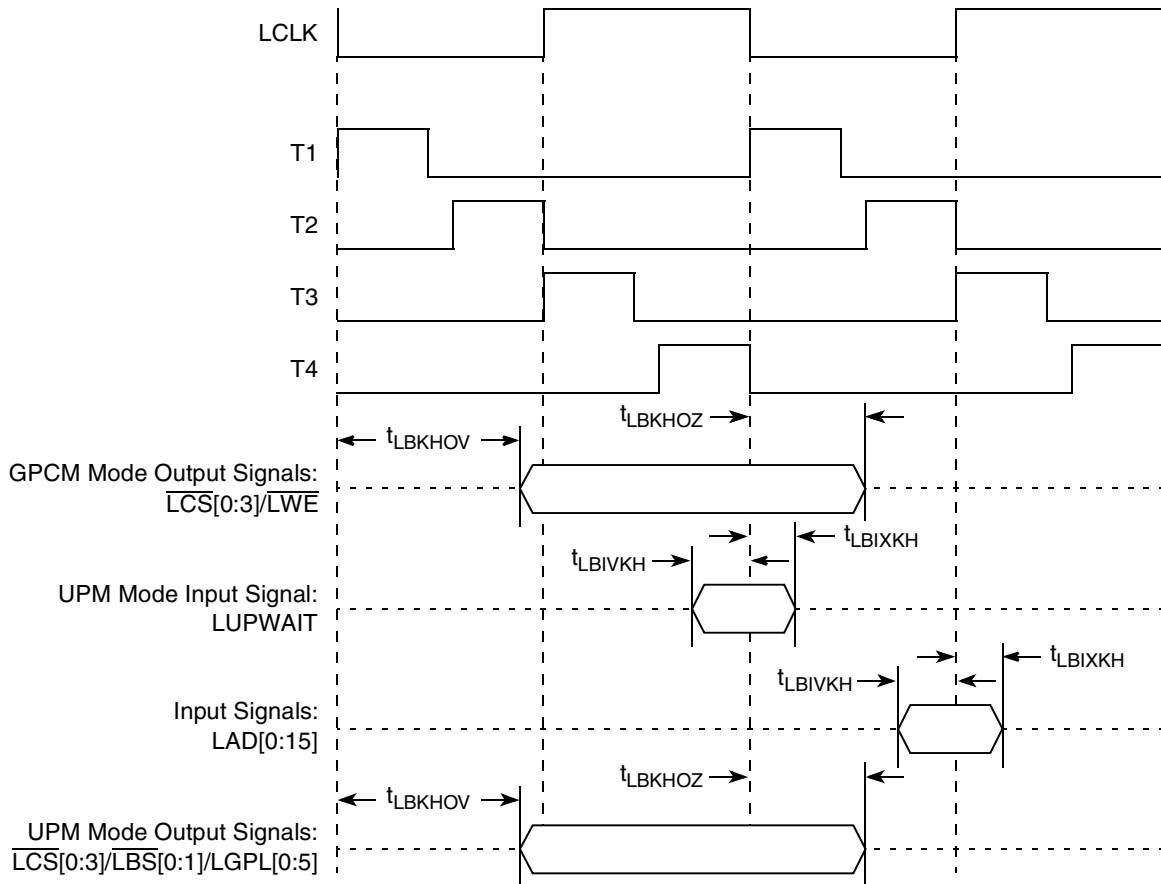


Figure 17. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8323E.

10.1 JTAG DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E.

Table 31. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.5	$OV_{DD} + 0.3$	V

Table 32. JTAG AC Timing Specifications (Independent of CLKIN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	2	19		5, 6
TDO	t_{JTKLOZ}	2	9		6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVXH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDVXH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK} .
5. Non-JTAG signal output timing with respect to t_{TCLK} .
6. Guaranteed by design and characterization.

Figure 18 provides the AC test load for TDO and the boundary-scan outputs of the MPC8323E.

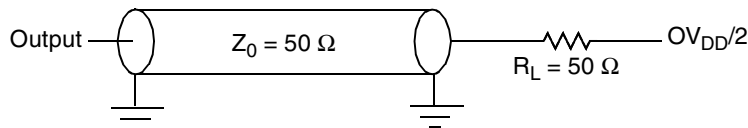

Figure 18. AC Test Load for the JTAG Interface

Figure 19 provides the JTAG clock input timing diagram.

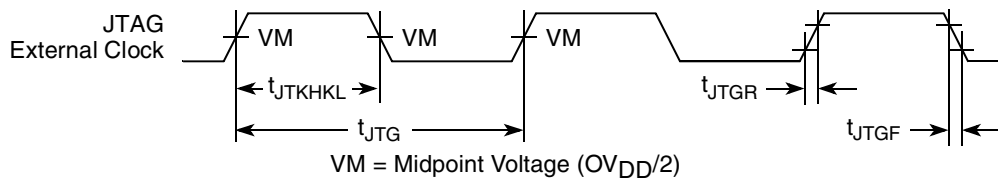

Figure 19. JTAG Clock Input Timing Diagram

Figure 20 provides the $\overline{TRST}$ timing diagram.

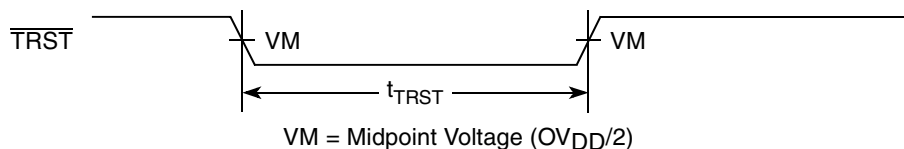

Figure 20. $\overline{TRST}$ Timing Diagram

Figure 27 shows the PCI output AC timing conditions.

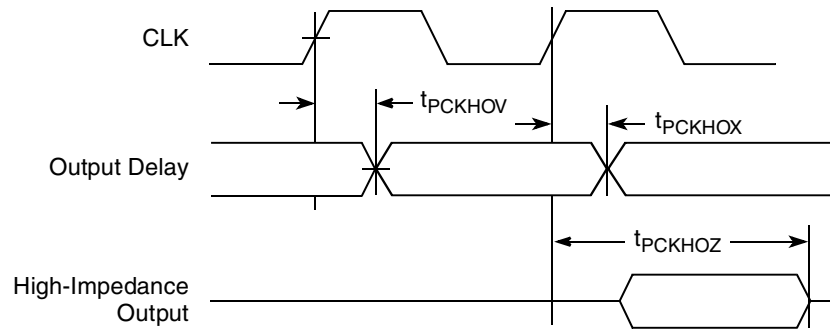


Figure 27. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8323E.

13.1 Timer DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the MPC8323E timer pins, including TIN, $\overline{\text{TOUT}}$, TGATE, and RTC_CLK.

Table 38. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

13.2 Timer AC Timing Specifications

Table 39 provides the timer input and output AC timing specifications.

Table 39. Timer Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Table 46. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	—	±5	μA

17.2 TDM/SI AC Timing Specifications

Table 47 provides the TDM/SI input and output AC timing specifications.

Table 47. TDM/SI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	12	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 33 provides the AC test load for the TDM/SI.

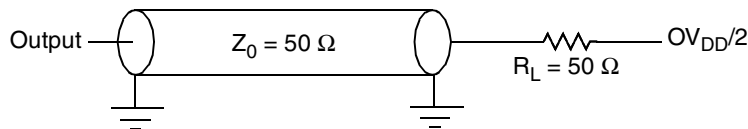
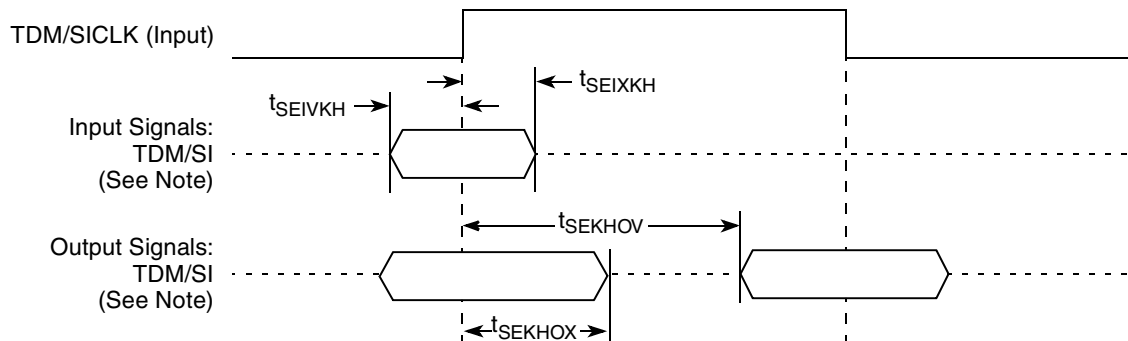

Figure 33. TDM/SI AC Test Load

Figure 34 represents the AC timing from Table 47. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on TDM/SI.

Figure 34. TDM/SI AC Timing (External Clock) Diagram

20 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8323E.

20.1 USB DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the USB interface.

Table 53. USB DC Electrical Characteristics¹

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V
Input current	I_{IN}	—	± 5	μA

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

20.2 USB AC Electrical Specifications

Table 54 describes the general timing parameters of the USB interface of the MPC8323E.

Table 54. USB General Timing Parameters

Parameter	Symbol ¹	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	20.83	—	ns	Full speed 48 MHz
USB clock cycle time	t_{USCK}	166.67	—	ns	Low speed 6 MHz
Skew between TXP and TXN	t_{USTSPN}	—	5	ns	—
Skew among RXP, RXN, and RXD	$t_{USRSPND}$	—	10	ns	Full speed transitions
Skew among RXP, RXN, and RXD	t_{USRPND}	—	100	ns	Low speed transitions

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(state)(signal)}$ for receive signals and $t_{(first\ two\ letters\ of\ functional\ block)(state)(signal)}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
- Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

Figure 41 provide the AC test load for the USB.

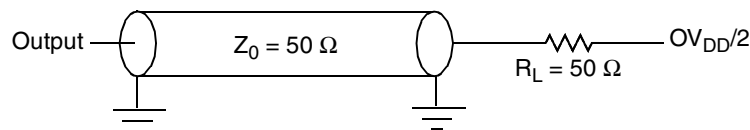
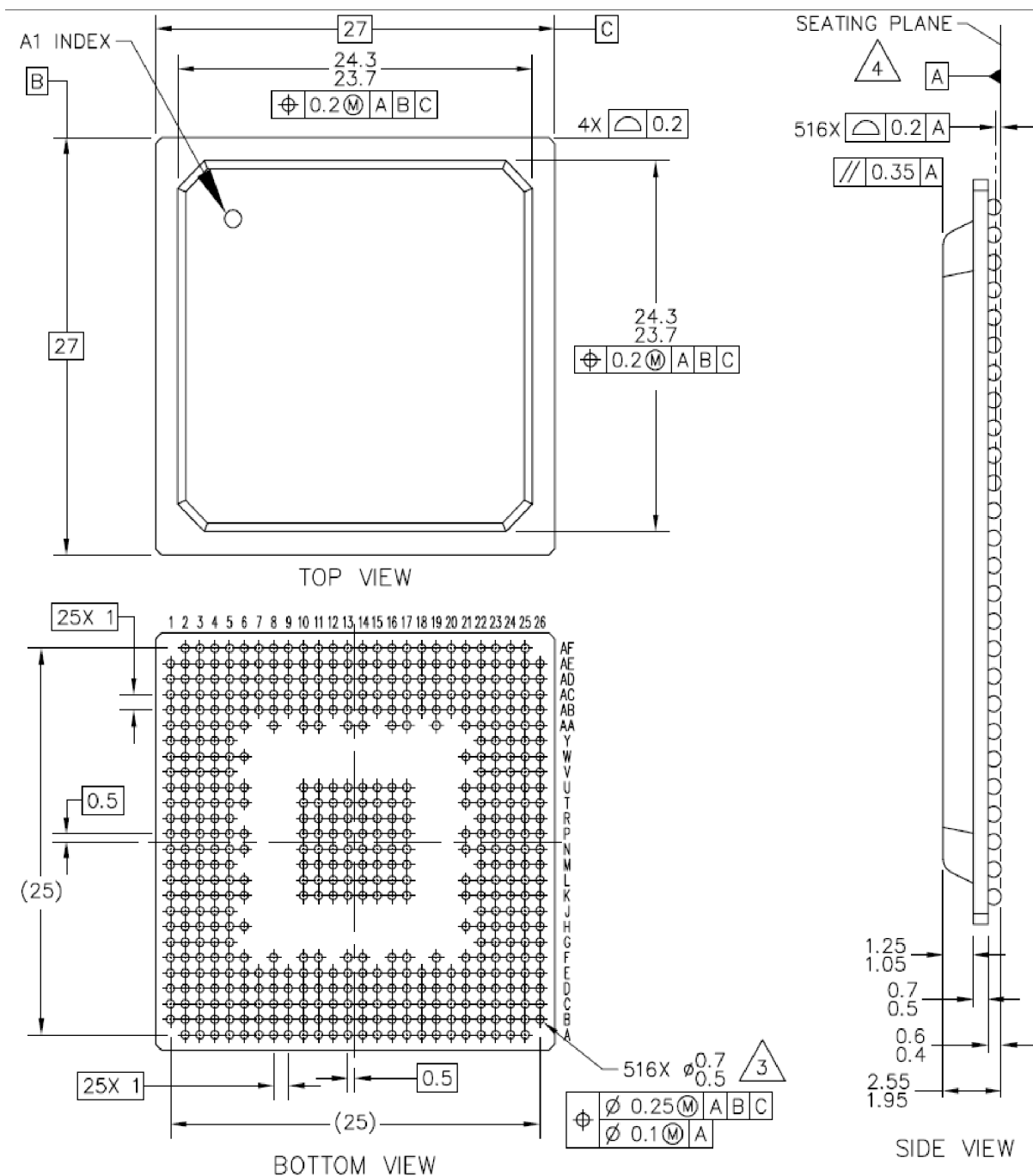


Figure 41. USB AC Test Load



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 42. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8323E PBGA

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	O	GV _{DD}	3
MEMC_MCK	AF14	O	GV _{DD}	—
MEMC_MCK	AE14	O	GV _{DD}	—
MEMC_MODT	AF11	O	GV _{DD}	—
Local Bus Controller Interface				
LAD0	N25	IO	OV _{DD}	7
LAD1	P26	IO	OV _{DD}	7
LAD2	P25	IO	OV _{DD}	7
LAD3	R26	IO	OV _{DD}	7
LAD4	R25	IO	OV _{DD}	7
LAD5	T26	IO	OV _{DD}	7
LAD6	T25	IO	OV _{DD}	7
LAD7	U25	IO	OV _{DD}	7
LAD8	M24	IO	OV _{DD}	7
LAD9	N24	IO	OV _{DD}	7
LAD10	P24	IO	OV _{DD}	7
LAD11	R24	IO	OV _{DD}	7
LAD12	T24	IO	OV _{DD}	7
LAD13	U24	IO	OV _{DD}	7
LAD14	U26	IO	OV _{DD}	7
LAD15	V26	IO	OV _{DD}	7
LA16	K25	O	OV _{DD}	7
LA17	L25	O	OV _{DD}	7
LA18	L26	O	OV _{DD}	7
LA19	L24	O	OV _{DD}	7
LA20	M26	O	OV _{DD}	7
LA21	M25	O	OV _{DD}	7
LA22	N26	O	OV _{DD}	7
LA23	AC24	O	OV _{DD}	7
LA24	AC25	O	OV _{DD}	7
LA25	AB23	O	OV _{DD}	7
LCS0	AB24	O	OV _{DD}	4

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PC10/UPC1_RxDATA[2]/SER5_RXD[2]	B21	IO	OV _{DD}	—
GPIO_PC11/UPC1_RxDATA[3]/SER5_RXD[3]	A20	IO	OV _{DD}	—
GPIO_PC12/UPC1_RxDATA[4]	D19	IO	OV _{DD}	—
GPIO_PC13/UPC1_RxDATA[5]/LSRCID0	C18	IO	OV _{DD}	—
GPIO_PC14/UPC1_RxDATA[6]/LSRCID1	D18	IO	OV _{DD}	—
GPIO_PC15/UPC1_RxDATA[7]/LSRCID2	A25	IO	OV _{DD}	—
GPIO_PC16/UPC1_TxADDR[0]	C21	IO	OV _{DD}	—
GPIO_PC17/UPC1_TxADDR[1]/LSRCID3	D22	IO	OV _{DD}	—
GPIO_PC18/UPC1_TxADDR[2]/LSRCID4	C23	IO	OV _{DD}	—
GPIO_PC19/UPC1_TxADDR[3]/LDVAL	D23	IO	OV _{DD}	—
GPIO_PC20/UPC1_RxADDR[0]	C17	IO	OV _{DD}	—
GPIO_PC21/UPC1_RxADDR[1]	D17	IO	OV _{DD}	—
GPIO_PC22/UPC1_RxADDR[2]	C16	IO	OV _{DD}	—
GPIO_PC23/UPC1_RxADDR[3]	D16	IO	OV _{DD}	—
GPIO_PC24/UPC1_RxSOC/SER5_CD	A16	IO	OV _{DD}	—
GPIO_PC25/UPC1_RxCLAV	D20	IO	OV _{DD}	—
GPIO_PC26/UPC1_RxPRTY/CE_EXT_REQ2	E23	IO	OV _{DD}	—
GPIO_PC27/UPC1_RxEN	B17	IO	OV _{DD}	—
GPIO_PC28/UPC1_TxSOC	B22	IO	OV _{DD}	—
GPIO_PC29/UPC1_TxCLAV/SER5_CTS	A17	IO	OV _{DD}	—
GPIO_PC30/UPC1_TxPRTY	A22	IO	OV _{DD}	—
GPIO_PC31/UPC1_TxEN/SER5_RTS	C20	IO	OV _{DD}	—
GPIO_PD0/SPIMOSI	A2	IO	OV _{DD}	—
GPIO_PD1/SPIMISO	B2	IO	OV _{DD}	—
GPIO_PD2/SPICLK	B3	IO	OV _{DD}	—
GPIO_PD3/SPISEL	A3	IO	OV _{DD}	—
GPIO_PD4/SPI_MDIO/CE_MUX_MDIO	A4	IO	OV _{DD}	—
GPIO_PD5/SPI_MDC/CE_MUX_MDC	B4	IO	OV _{DD}	—
GPIO_PD6/CLK8/BRGO16/CE_EXT_REQ3	F24	IO	OV _{DD}	—
GPIO_PD7/GTM1_TIN1/GTM2_TIN2/CLK5	G24	IO	OV _{DD}	—
GPIO_PD8/GTM1_TGATE1/GTM2_TGATE2/CLK6	H24	IO	OV _{DD}	—
GPIO_PD9/GTM1_TOUT1	D24	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PD10/GTM1_TIN2/GTM2_TIN1/CLK17	J24	IO	OV _{DD}	—
GPIO_PD11/GTM1_TGATE2/GTM2_TGATE1	B25	IO	OV _{DD}	—
GPIO_PD12/GTM1_TOUT2/GTM2_TOUT1	C4	IO	OV _{DD}	—
GPIO_PD13/GTM1_TIN3/GTM2_TIN4/BRGO8	D4	IO	OV _{DD}	—
GPIO_PD14/GTM1_TGATE3/GTM2_TGATE4	D5	IO	OV _{DD}	—
GPIO_PD15/GTM1_TOUT3	A5	IO	OV _{DD}	—
GPIO_PD16/GTM1_TIN4/GTM2_TIN3	B5	IO	OV _{DD}	—
GPIO_PD17/GTM1_TGATE4/GTM2_TGATE3	C5	IO	OV _{DD}	—
GPIO_PD18/GTM1_TOUT4/GTM2_TOUT3	A6	IO	OV _{DD}	—
GPIO_PD19/CE_RISC1_INT/CE_EXT_REQ4	B6	IO	OV _{DD}	—
GPIO_PD20/CLK18/BRGO6	D21	IO	OV _{DD}	—
GPIO_PD21/CLK16/BRGO5/UPC1_CLKO	C19	IO	OV _{DD}	—
GPIO_PD22/CLK4/BRGO9/UCC2_CLKO	A7	IO	OV _{DD}	—
GPIO_PD23/CLK3/BRGO10/UCC3_CLKO	B7	IO	OV _{DD}	—
GPIO_PD24/CLK10/BRGO2/UCC4_CLKO	A12	IO	OV _{DD}	—
GPIO_PD25/CLK13/BRGO16/UCC5_CLKO	B10	IO	OV _{DD}	—
GPIO_PD26/CLK2/BRGO4/UCC1_CLKO	E4	IO	OV _{DD}	—
GPIO_PD27/CLK1/BRGO3	F4	IO	OV _{DD}	—
GPIO_PD28/CLK19/BRGO11	D15	IO	OV _{DD}	—
GPIO_PD29/CLK15/BRGO8	C6	IO	OV _{DD}	—
GPIO_PD30/CLK14	D6	IO	OV _{DD}	—
GPIO_PD31/CLK7/BRGO15	E24	IO	OV _{DD}	—
Power and Ground Supplies				
GV _{DD}	AA8, AA10, AA11, AA13, AA14, AA16, AA17, AA19, AA21, AB9, AB10, AB11, AB12, AB14, AB18, AB20, AB21, AC6, AC8, AC14, AC18	GV _{DD}	—	—
OV _{DD}	E5, E6, E8, E9, E10, E12, E14, E15, E16, E18, E19, E20, E22, F5, F6, F8, F10, F14, F16, F19, F22, G22, H5, H6, H21, J5, J22, K21, K22, L5, L6, L22, M5, M22, N5, N21, N22, P6, P22, P23, R5, R23, T5, T21, T22, U6, U22, V5, V22, W22, Y5, AB5, AB6, AC5	OV _{DD}	—	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	K10, K11, K12, K13, K14, K15, K16, K17, L10, L17, M10, M17, N10, N17, P10, P17, R10, R17, T10, T17, U10, U11, U12, U13, U14, U15, U16, U17	V_{DD}	—	—
V_{SS}	B23, E7, E11, E13, E17, E21, F11, F13, F17, F21, F23, G5, H22, K5, K6, L11, L12, L13, L14, L15, L16, L21, M11, M12, M13, M14, M15, M16, N6, N11, N12, N13, N14, N15, N16, P5, P11, P12, P13, P14, P15, P16, P21, R11, R12, R13, R14, R15, R16, R22, T6, T11, T12, T13, T14, T15, T16, U5, U21, V23, W5, W6, W21, W23, W24, Y22, AA5, AA6, AA22, AA25, AB7, AB13, AB19, AB22, AC10, AC12, AC16, AC20	V_{SS}	—	—
No Connect				
NC	C22	—	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD} .
2. This pin is an open drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD} .
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG and local bus pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow the PCI specification's recommendation.
6. This pin must always be tied to GND. 7. This pin has weak internal pull-down N-FET that is always enabled. 8. Though this pin has weak internal pull-up yet it is recommended to apply an external pull-up.

shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 59. CSB Frequency Options

CFG_CLKIN_DIV_B at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	Input Clock Frequency (MHz) ²		
			25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)		
High	0010	2 : 1			133
High	0011	3 : 1		100	
High	0100	4 : 1	100	133	
High	0101	5 : 1	125		
High	0110	6 : 1			
High	0111	7 : 1			
High	1000	8 : 1			
High	1001	9 : 1			
High	1010	10 : 1			
High	1011	11 : 1			
High	1100	12 : 1			
High	1101	13 : 1			
High	1110	14 : 1			
High	1111	15 : 1			
High	0000	16 : 1			
Low	0010	2 : 1			133
Low	0011	3 : 1		100	
Low	0100	4 : 1		133	
Low	0101	5 : 1			
Low	0110	6 : 1			
Low	0111	7 : 1			
Low	1000	8 : 1			
Low	1001	9 : 1			
Low	1010	10 : 1			
Low	1011	11 : 1			
Low	1100	12 : 1			
Low	1101	13 : 1			
Low	1110	14 : 1			
Low	1111	15 : 1			
Low	0000	16 : 1			

¹ CFG_CLKIN_DIV_B is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV_B must be pulled up (high) in agent mode.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

22.5 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 60 shows the encodings for RCWL[COREPLL]. COREPLL values not listed in Table 60 should be considered reserved.

Table 60. e300 Core PLL Configuration

RCWL[COREPLL]			<i>core_clk</i> : <i>csb_clk</i> Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷2
01	0001	1	1.5:1	÷4
10	0001	1	1.5:1	÷8
11	0001	1	1.5:1	÷8
00	0010	0	2:1	÷2
01	0010	0	2:1	÷4
10	0010	0	2:1	÷8
11	0010	0	2:1	÷8
00	0010	1	2.5:1	÷2
01	0010	1	2.5:1	÷4
10	0010	1	2.5:1	÷8
11	0010	1	2.5:1	÷8
00	0011	0	3:1	÷2
01	0011	0	3:1	÷4
10	0011	0	3:1	÷8
11	0011	0	3:1	÷8

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 500–800 MHz.

22.6 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. [Table 61](#) shows the multiplication factor encodings for the QUICC Engine PLL.

Table 61. QUICC Engine PLL Multiplication Factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/(1 + RCWL[CEPDF])
00000–00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in [Table 62](#).

Table 62. QUICC Engine PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

$$ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$$

$$\text{QUICC Engine VCO Frequency} = ce_clk \times \text{VCO divider} \times (1 + \text{CEPDF})$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-567-8082
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics 800-522-2800
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

24.7 Pull-Up Resistor Requirements

The MPC8323E requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins including I²C pins, Ethernet Management MDIO pin, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see AN3361, “MPC8321E/MPC8323E PowerQUICC Design Checklist,” Rev. 1.

25 Ordering Information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in [Section 25.1, “Part Numbers Fully Addressed by This Document.”](#)

25.1 Part Numbers Fully Addressed by This Document

[Table 66](#) provides the Freescale part numbering nomenclature for the MPC8323E family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

Table 66. Part Numbering Nomenclature

MPC	nnnn	E	C	VR	AF	D	C	A
Product Code	Part Identifier	Encryption Acceleration	Temperature Range ¹	Package ²	e300 Core Frequency ³	DDR Frequency	QUICC Engine Frequency	Revision Level
MPC	8323	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	VR = Pb-free PBGA ZQ = Pb PBGA	AD = 266 MHz AF = 333 MHz	D = 266 MHz	C = 200 MHz	Contact local Freescale sales office

Notes:

1. Contact local Freescale office on availability of parts with C temperature range.
2. See [Section 21, “Package and Pin Listings,”](#) for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.