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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8321zqaddc

1 Overview

The MPC8323E incorporates the e300c2 (MPC603e-based) core built on Power Architecture® technology, which includes 16 Kbytes of L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The e300c2 core does not contain a floating point unit (FPU). The MPC8323E also includes a 32-bit PCI controller, four DMA channels, a security engine, and a 32-bit DDR1/DDR2 memory controller.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8323E. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). Note that the MPC8321 and MPC8321E do not support UTOPIA. A block diagram of the MPC8323E is shown in Figure 1.

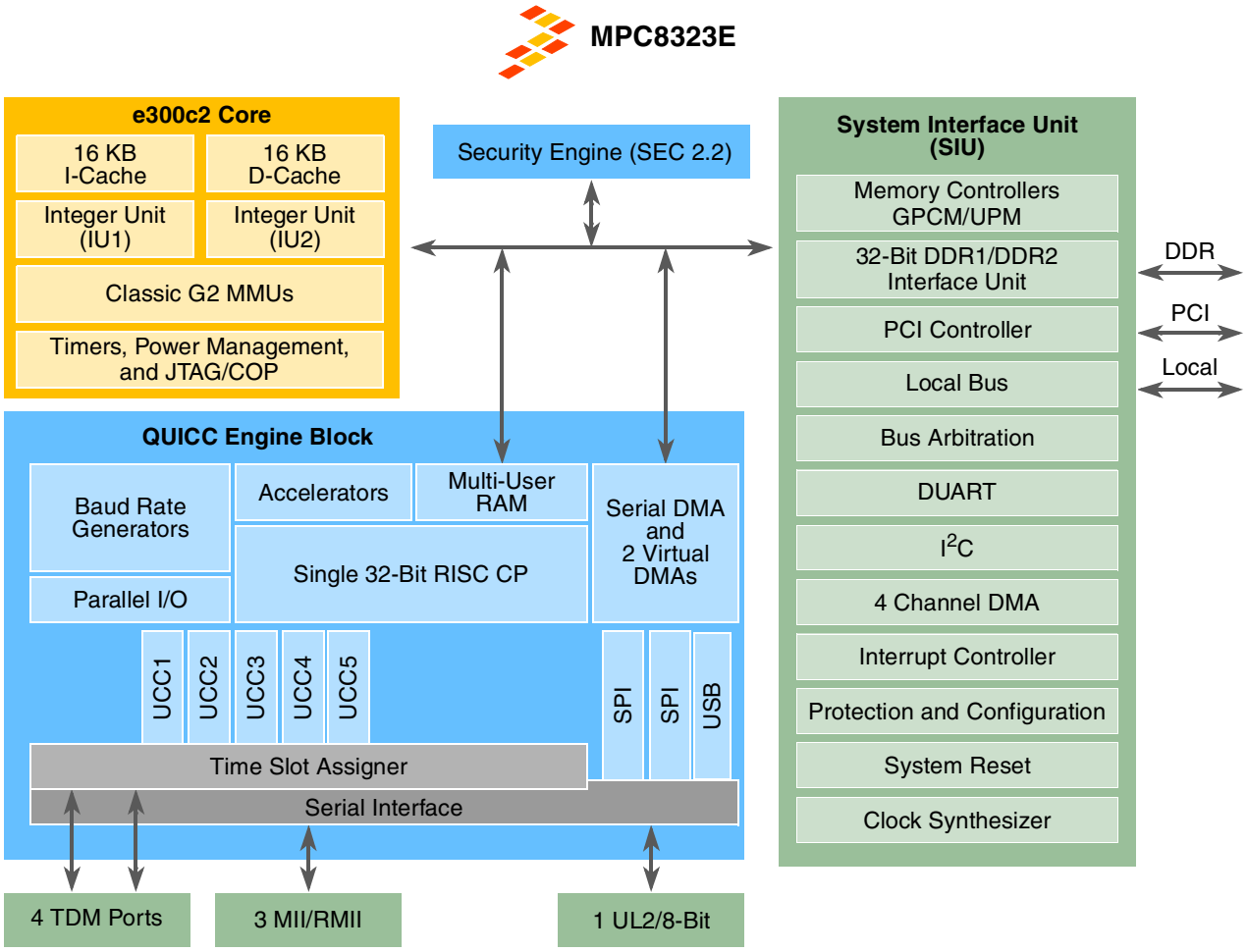


Figure 1. MPC8323E Block Diagram

Each of the five UCCs can support a variety of communication protocols: 10/100 Mbps Ethernet, serial ATM, HDLC, UART, and BISYNC—and, in the MPC8323E and MPC8323, multi-PHY ATM and ATM support for up to OC-3 speeds.

Table 26. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load.

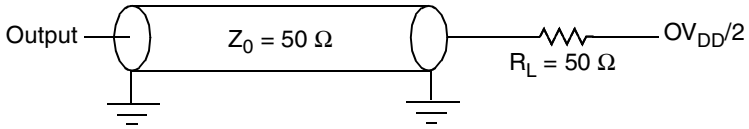


Figure 11. AC Test Load

Figure 12 shows the RMII receive AC timing diagram.

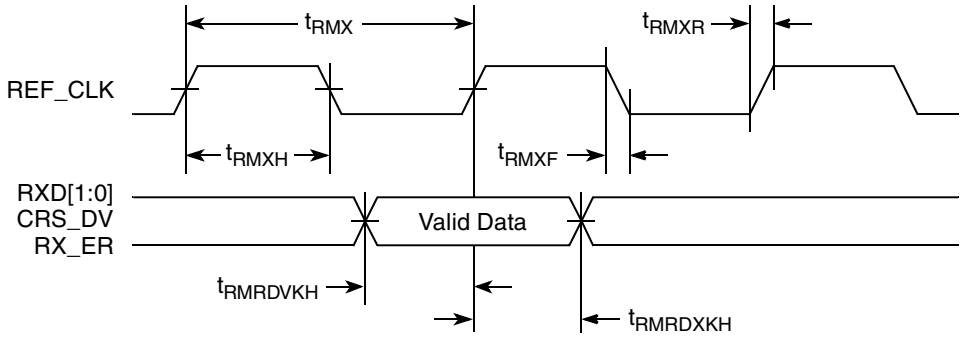


Figure 12. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, “Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics.”

Figure 13 shows the MII management AC timing diagram.

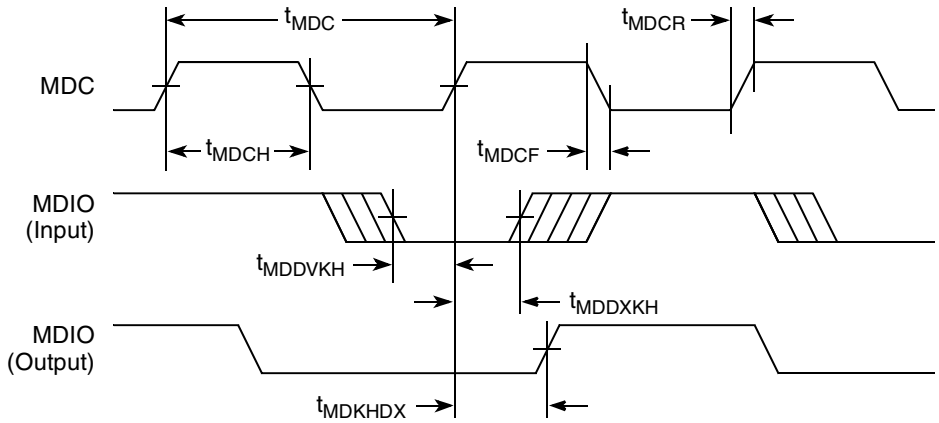


Figure 13. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8323E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±5	µA

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8323E.

Table 30. Local Bus General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK*n*)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK*n*)	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5

Table 30. Local Bus General Timing Parameters (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock (LCLK*n*) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK*n*) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8
Local bus clock (LCLK*n*) duty cycle	t_{LBDC}	47	53	%	—
Local bus clock (LCLK*n*) jitter specification	t_{LBRJ}	—	400	ps	—
Delay between the input clock (PCI_SYNC_IN) of local bus output clock (LCLK*n*)	t_{LBCDL}	—	1.7	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 14 provides the AC test load for the local bus.

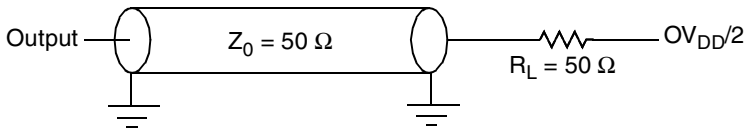


Figure 14. Local Bus C Test Load

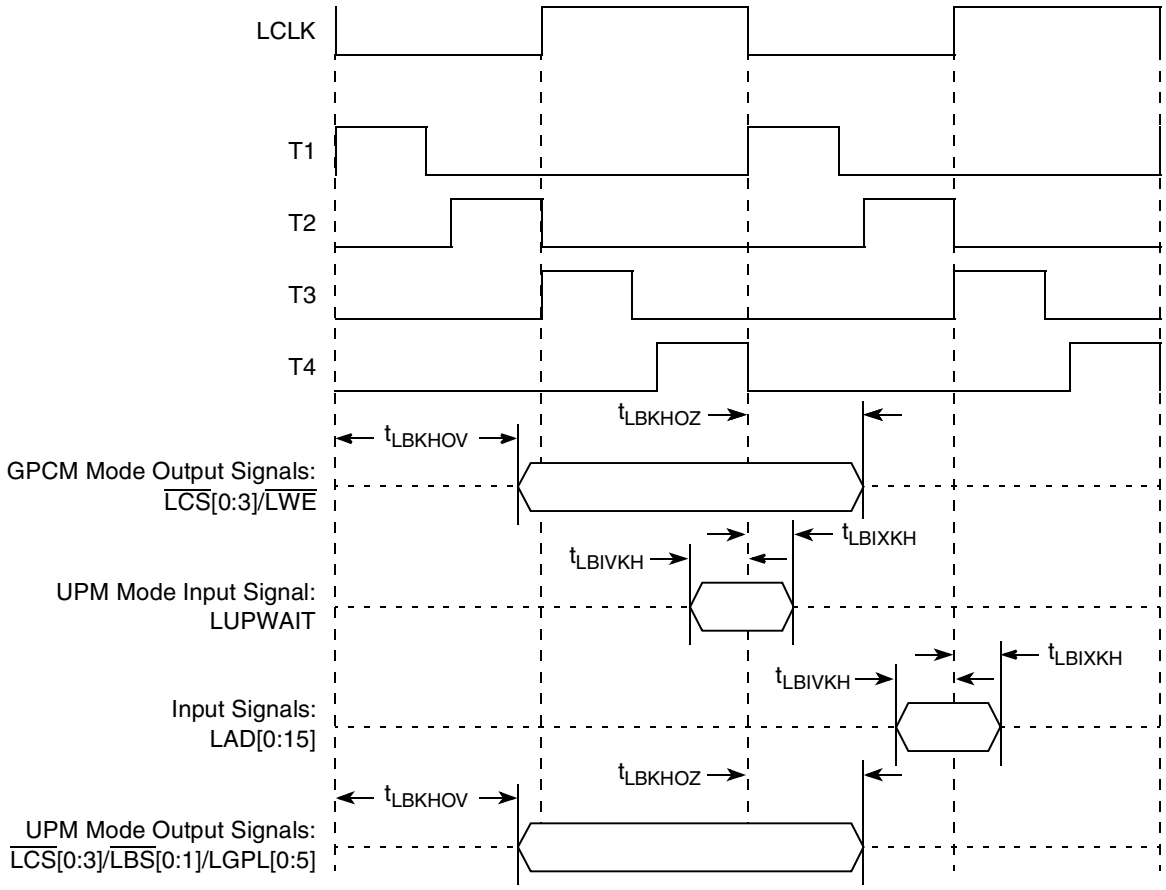


Figure 17. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8323E.

10.1 JTAG DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E.

Table 31. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.5	OV_{DD} + 0.3	V

Table 32. JTAG AC Timing Specifications (Independent of CLKIN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	 5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 18 provides the AC test load for TDO and the boundary-scan outputs of the MPC8323E.

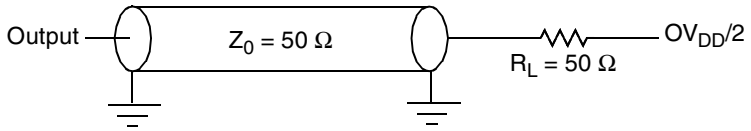


Figure 18. AC Test Load for the JTAG Interface

Figure 19 provides the JTAG clock input timing diagram.

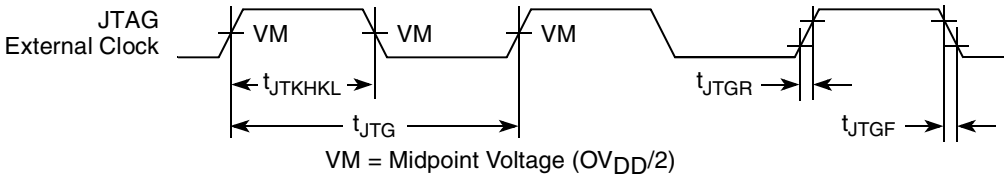


Figure 19. JTAG Clock Input Timing Diagram

Figure 20 provides the $\overline{\text{TRST}}$ timing diagram.

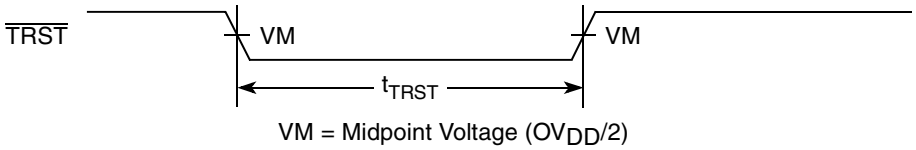


Figure 20. $\overline{\text{TRST}}$ Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

Table 33. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I²C interface of the MPC8323E.

Table 34. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0[2]	— 0.9[3]	μs

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8323E.

12.1 PCI DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the PCI interface of the MPC8323E.

Table 35. PCI DC Electrical Characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 µA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 µA	—	0.2	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	µA

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.
2. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.3 Local Bus Specifications*.

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8323E. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8323E is configured as a host or agent device. Table 36 shows the PCI AC timing specifications at 66 MHz.

Table 36. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedence	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Table 44. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 30 provides the AC test load for the SPI.

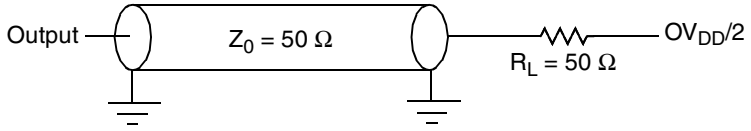
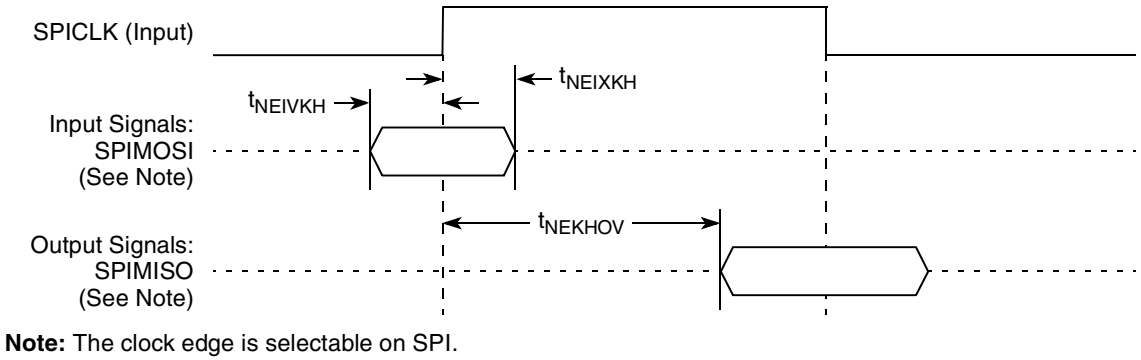


Figure 30. SPI AC Test Load

Figure 31 and Figure 32 represent the AC timing from Table 45. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

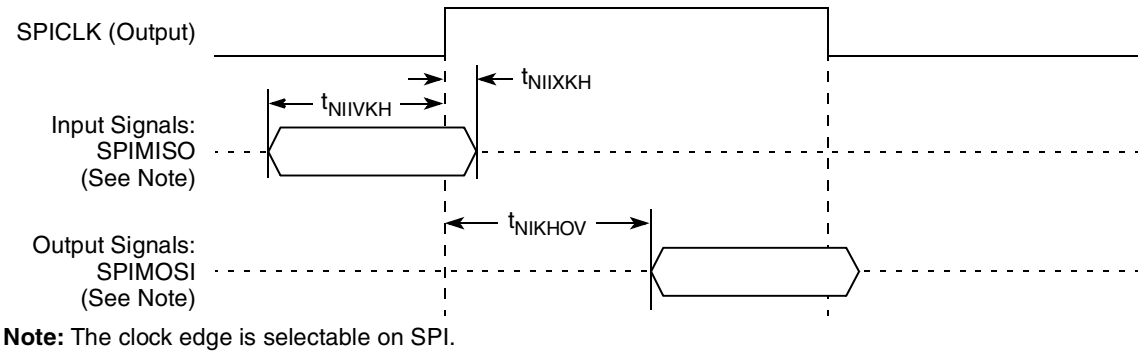
Figure 31 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 31. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 32 shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 32. SPI AC Timing in Master Mode (Internal Clock) Diagram

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8323E.

17.1 TDM/SI DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the MPC8323E TDM/SI.

Table 46. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V

21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8323E is available in a thermally enhanced Plastic Ball Grid Array (PBGA); see Section 21.1, "Package Parameters for the MPC8323E PBGA," and Section 21.2, "Mechanical Dimensions of the MPC8323E PBGA," for information on the PBGA.

21.1 Package Parameters for the MPC8323E PBGA

The package parameters are as provided in the following list. The package type is 27 mm × 27 mm, 516 PBGA.

Package outline	27 mm × 27 mm
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.6 mm

21.2 Mechanical Dimensions of the MPC8323E PBGA

Figure 42 shows the mechanical dimensions and bottom surface nomenclature of the MPC8323E, 516-PBGA package.

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LCS1}}$	AB25	O	OV_{DD}	4
$\overline{\text{LCS2}}$	AA23	O	OV_{DD}	4
$\overline{\text{LCS3}}$	AA24	O	OV_{DD}	4
$\overline{\text{LWE0}}$	Y23	O	OV_{DD}	4
$\overline{\text{LWE1}}$	W25	O	OV_{DD}	4
LBCTL	V25	O	OV_{DD}	4
LALE	V24	O	OV_{DD}	7
CFG_RESET_SOURCE[0]/LSDA10/LGPL0	L23	IO	OV_{DD}	—
CFG_RESET_SOURCE[1]/$\overline{\text{LSDWE}}$/LGPL1	K23	IO	OV_{DD}	—
$\overline{\text{LSDRAS}}$/LGPL2/$\overline{\text{LOE}}$	J23	O	OV_{DD}	4
CFG_RESET_SOURCE[2]/$\overline{\text{LSDCAS}}$/LGPL3	H23	IO	OV_{DD}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	G23	IO	OV_{DD}	4, 8
LGPL5	AC22	O	OV_{DD}	4
LCLK0	Y24	O	OV_{DD}	7
LCLK1	Y25	O	OV_{DD}	7
DUART				
UART_SOUT1/MSRCID0 (DDR ID)/LSRCID0	G1	IO	OV_{DD}	—
UART_SIN1/MSRCID1 (DDR ID)/LSRCID1	G2	IO	OV_{DD}	—
$\overline{\text{UART\_CTS1}}$/MSRCID2 (DDR ID)/LSRCID2	H3	IO	OV_{DD}	—
$\overline{\text{UART\_RTS1}}$/MSRCID3 (DDR ID)/LSRCID3	K3	IO	OV_{DD}	—
UART_SOUT2/MSRCID4 (DDR ID)/LSRCID4	H2	IO	OV_{DD}	—
UART_SIN2/MDVAL (DDR ID)/LDVAL	H1	IO	OV_{DD}	—
$\overline{\text{UART\_CTS2}}$	J3	IO	OV_{DD}	—
$\overline{\text{UART\_RTS2}}$	K4	IO	OV_{DD}	—
I^2C interface				
IIC_SDA/$\overline{\text{CKSTOP\_OUT}}$	AE24	IO	OV_{DD}	2
IIC_SCL/$\overline{\text{CKSTOP\_IN}}$	AF24	IO	OV_{DD}	2
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	AD25	O	OV_{DD}	—
$\overline{\text{IRQ0}}$/$\overline{\text{MCP\_IN}}$	AD26	I	OV_{DD}	—
$\overline{\text{IRQ1}}$	K1	IO	OV_{DD}	—
$\overline{\text{IRQ2}}$	K2	I	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ3}}$	J2	I	OV_{DD}	—
$\overline{\text{IRQ4}}$	J1	I	OV_{DD}	—
$\overline{\text{IRQ5}}$	AE26	I	OV_{DD}	—
$\overline{\text{IRQ6}}$/$\overline{\text{CKSTOP\_OUT}}$	AE25	IO	OV_{DD}	—
$\overline{\text{IRQ7}}$/$\overline{\text{CKSTOP\_IN}}$	AF25	I	OV_{DD}	—
$\overline{\text{CFG\_CLKIN\_DIV}}$	F1	I	OV_{DD}	—
CFG_LBIU_MUX_EN	M23	I	OV_{DD}	—
JTAG				
TCK	W26	I	OV_{DD}	—
TDI	Y26	I	OV_{DD}	4
TDO	AA26	O	OV_{DD}	3
TMS	AB26	I	OV_{DD}	4
$\overline{\text{TRST}}$	AC26	I	OV_{DD}	4
TEST				
TEST_MODE	N23	I	OV_{DD}	6
PMC				
$\overline{\text{QUIESCE}}$	T23	O	OV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AC23	IO	OV_{DD}	1
$\overline{\text{PORESET}}$	AD23	I	OV_{DD}	—
$\overline{\text{SRESET}}$	AD24	IO	OV_{DD}	2
Clocks				
CLKIN	R3	I	OV_{DD}	—
$\overline{\text{CLKIN}}$	P4	O	OV_{DD}	—
PCI_SYNC_OUT	V1	O	OV_{DD}	3
RTC_PIT_CLOCK	U23	I	OV_{DD}	—
PCI_SYNC_IN/PCI_CLK	V2	I	OV_{DD}	—
PCI_CLK0/clkpd_cerisc1_ipg_clkout/DPTC_OSC	T3	O	OV_{DD}	—
PCI_CLK1/clkpd_half_cemb4ucc1_ipg_clkout/ CLOCK_XLB_CLOCK_OUT	U2	O	OV_{DD}	—
PCI_CLK2/clkpd_third_cesog_ipg_clkout/ cecl_ipg_ce_clock	R4	O	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE/GPIO				
GPIO_PA0/SER1_TXD[0]/TDMA_TXD[0]/USBTXN	G3	IO	OV_{DD}	—
GPIO_PA1/SER1_TXD[1]/TDMA_TXD[1]/USBTXP	F3	IO	OV_{DD}	—
GPIO_PA2/SER1_TXD[2]/TDMA_TXD[2]	F2	IO	OV_{DD}	—
GPIO_PA3/SER1_TXD[3]/TDMA_TXD[3]	E3	IO	OV_{DD}	—
GPIO_PA4/SER1_RXD[0]/TDMA_RXD[0]/USBRXP	E2	IO	OV_{DD}	—
GPIO_PA5/SER1_RXD[1]/TDMA_RXD[1]/USBRXN	E1	IO	OV_{DD}	—
GPIO_PA6/SER1_RXD[2]/TDMA_RXD[2]/USBRXD	D3	IO	OV_{DD}	—
GPIO_PA7/SER1_RXD[3]/TDMA_RXD[3]	D2	IO	OV_{DD}	—
GPIO_PA8/SER1_CD/TDMA_REQ/$\overline{\text{USBOE}}$	D1	IO	OV_{DD}	—
GPIO_PA9 TDMA_CLKO	C3	IO	OV_{DD}	—
GPIO_PA10/SER1_CTS/TDMA_RSYNC	C2	IO	OV_{DD}	—
GPIO_PA11/TDMA_STROBE	C1	IO	OV_{DD}	—
GPIO_PA12/SER1_RTS/TDMA_TSYNC	B1	IO	OV_{DD}	—
GPIO_PA13/CLK9/BRGO9	H4	IO	OV_{DD}	—
GPIO_PA14/CLK11/BRGO10	G4	IO	OV_{DD}	—
GPIO_PA15/BRGO7	J4	IO	OV_{DD}	—
GPIO_PA16/ LA0 (LBIU)	K24	IO	OV_{DD}	—
GPIO_PA17/ LA1 (LBIU)	K26	IO	OV_{DD}	—
GPIO_PA18/Enet2_TXD[0]/SER2_TXD[0]/ TDMB_TXD[0]/LA2 (LBIU)	G25	IO	OV_{DD}	—
GPIO_PA19/Enet2_TXD[1]/SER2_TXD[1]/ TDMB_TXD[1]/LA3 (LBIU)	G26	IO	OV_{DD}	—
GPIO_PA20/Enet2_TXD[2]/SER2_TXD[2]/ TDMB_TXD[2]/LA4 (LBIU)	H25	IO	OV_{DD}	—
GPIO_PA21/Enet2_TXD[3]/SER2_TXD[3]/ TDMB_TXD[3]/LA5 (LBIU)	H26	IO	OV_{DD}	—
GPIO_PA22/Enet2_RXD[0]/SER2_RXD[0]/ TDMB_RXD[0]/LA6 (LBIU)	C25	IO	OV_{DD}	—
GPIO_PA23/Enet2_RXD[1]/SER2_RXD[1]/ TDMB_RXD[1]/LA7 (LBIU)	C26	IO	OV_{DD}	—
GPIO_PA24/Enet2_RXD[2]/SER2_RXD[2]/ TDMB_RXD[2]/LA8 (LBIU)	D25	IO	OV_{DD}	—
GPIO_PA25/Enet2_RXD[3]/SER2_RXD[3]/ TDMB_RXD[3]/LA9 (LBIU)	D26	IO	OV_{DD}	—

22 Clocking

Figure 43 shows the internal distribution of clocks within the MPC8323E.

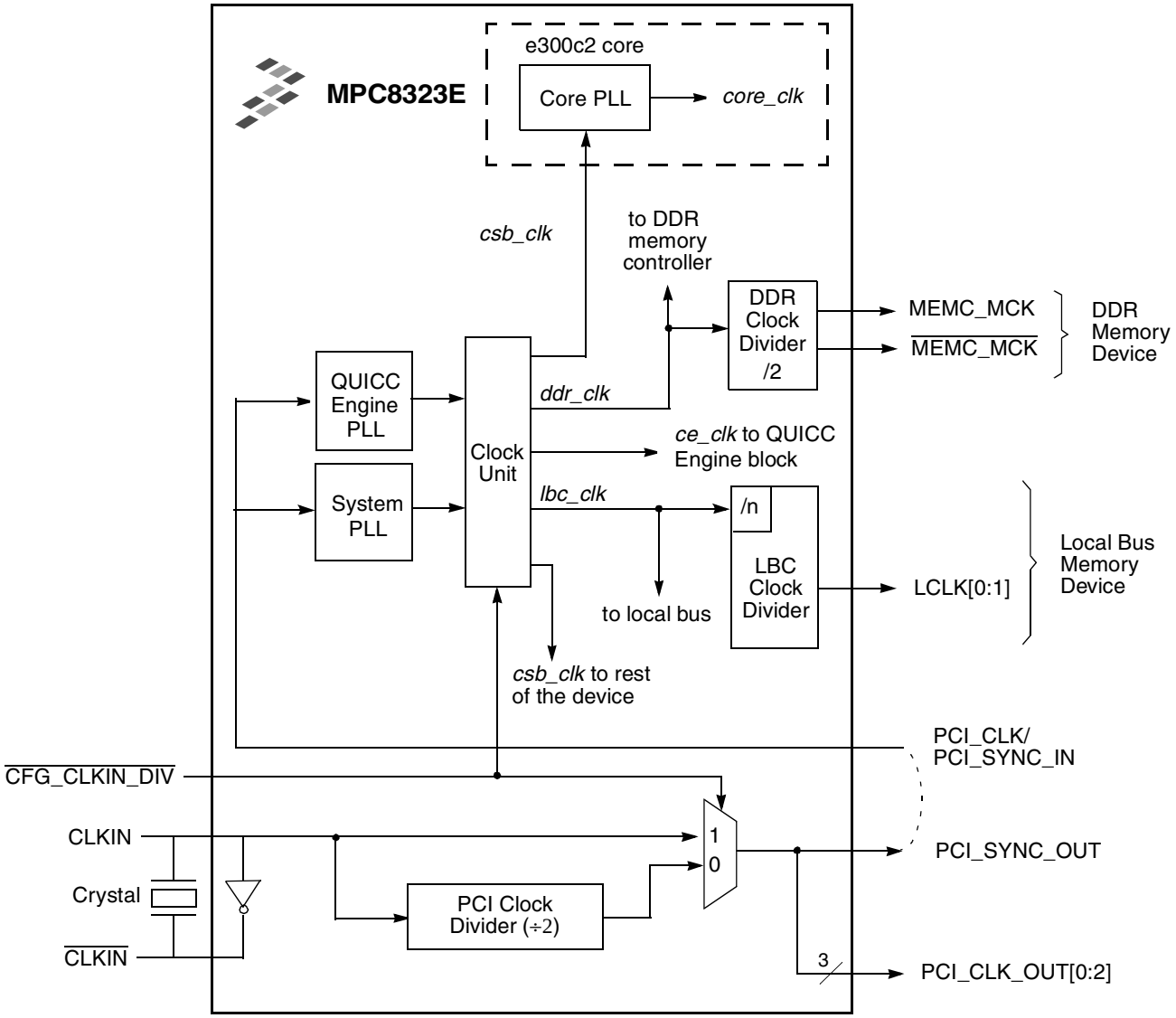


Figure 43. MPC8323E Clock Subsystem

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode, respectively.

22.1 Clocking in PCI Host Mode

When the MPC8323E is configured as a PCI host device (RCWH[PCIHOST] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexors. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

22.1.1 PCI Clock Outputs (PCI_CLK_OUT[0:2])

When the MPC8323E is configured as a PCI host, it provides three separate clock output signals, PCI_CLK_OUT[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOE*n*] bit. All output clocks are phase-aligned to each other.

22.2 Clocking in PCI Agent Mode

When the MPC8323E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND, and the clock output signals, PCI_CLK_OUT*n* and PCI_SYNC_OUT, are not used.

22.3 System Clock Domains

As shown in Figure 43, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*ce_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lb_clk*)

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = [\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})] \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\text{CFG\_CLKIN\_DIV}}$) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300c2 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See the “Reset Configuration” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-567-8082
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics 800-522-2800
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 44 shows the PLL power supply filter circuit.

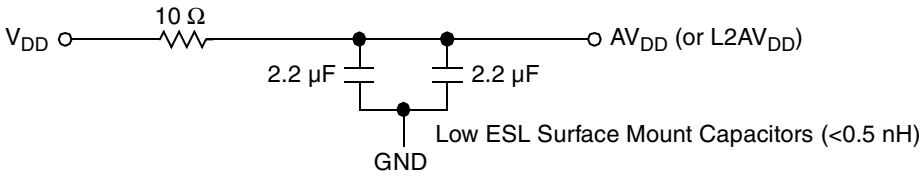


Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8323E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8323E system, and the MPC8323E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pins of the MPC8323E. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, or GV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, OV_{DD}, and GND pins of the MPC8323E.

24.5 Output Buffer DC Impedance

The MPC8323E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The

Table 67. Document Revision History

Rev. No.	Date	Substantive Change(s)
2	4/2008	• Removed Figures 2 and 3 overshoot and undershoot voltage specs from Section 2.1.2, "Power Supply Voltage Specification," and footnotes 4 and 5 from Table 1. • Corrected QUIESCE signal to be an output signal in Table 55. • Added column for GVDD (1.8 V) - DDR2 - to Table 6 with 0.212-W typical power dissipation. • Added Figure 4 DDR input timing diagram. • Removed CE_TRB* and CE_PIO* signals from Table 55. • Added three local bus AC specifications to Table 30 (duty cycle, jitter, delay between input clock and local bus clock). • Added row in Table 2 stating junction temperature range of 0 to 105•C. • Modified Section 2.2, "Power Sequencing," to include $\overline{\text{PORESET}}$ requirement.
1	6/2007	Correction to descriptive text in Section 2.2.
0	6/2007	Initial release.