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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8323czqaddc

NOTE

The QUICC Engine block can also support a UTOPIA level 2 capable of supporting 31 multi-PHY (MPC8323E- and MPC8323-specific).

The MPC8323E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In summary, the MPC8323E family provides users with a highly integrated, fully programmable communications processor. This helps ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

1.1 MPC8323E Features

Major features of the MPC8323E are as follows:

- High-performance, low-power, and cost-effective single-chip data-plane/control-plane solution for ATM or IP/Ethernet packet processing (or both).
- MPC8323E QUICC Engine block offers a future-proof solution for next generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards.
- Single platform architecture supports the convergence of IP packet networks and ATM networks.
- DDR1/DDR2 memory controller—one 32-bit interface at up to 266 MHz supporting both DDR1 and DDR2.
- An e300c2 core built on Power Architecture technology with 16-Kbyte instruction and data caches, and dual integer units.
- Peripheral interfaces such as 32-bit PCI (2.2) interface up to 66-MHz operation, 16-bit local bus interface up to 66-MHz operation, and USB 2.0 (full-/low-speed).
- Security engine provides acceleration for control and data plane security protocols.
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration.

1.1.1 Protocols

The protocols are as follows:

- ATM SAR up to 155 Mbps (OC-3) full duplex, with ATM traffic shaping (ATF TM4.1)
- Support for ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- Support for IMA and ATM transmission convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- Support for 64 channels of HDLC/transparent

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8323E. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions[3]

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	1
PLL supply voltage	AV_{DD}	1.0 V ± 50 mV	V	1
DDR1 and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
PCI, local bus, DUART, system control and power management, I^2C, SPI, and JTAG I/O voltage	OV_{DD}	3.3 V ± 300 mV	V	1
Junction temperature	T_A/T_J	0 to 105	°C	2

Note:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.
3. All IO pins should be interfaced with peripherals operating at same voltage level.
4. This voltage is the input to the filter discussed in Section 24.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced due to voltage drop across the filter.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8323E

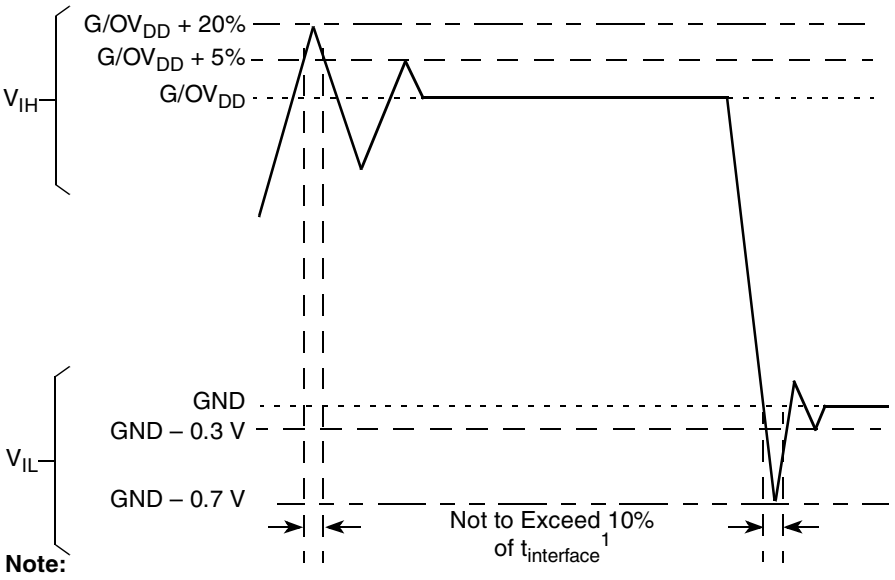


Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}

Table 6. Estimated Typical I/O Power Dissipation (continued)

Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 32 bits	—	—	0.12	W	—
PCI I/O load = 30 pF	66 MHz, 32 bits	—	—	0.057	W	—
QUICC Engine block and other I/Os	UTOPIA 8-bit 31 PHYs	—	—	0.041	W	Multiply by number of interfaces used.
	TDM serial	—	—	0.001	W	
	TDM nibble	—	—	0.004	W	
	HDLC/TRAN serial	—	—	0.003	W	
	HDLC/TRAN nibble	—	—	0.025	W	
	DUART	—	—	0.017	W	
	MIIs	—	—	0.009	W	
	RMII	—	—	0.009	W	
	Ethernet management	—	—	0.002	W	
	USB	—	—	0.001	W	
	SPI	—	—	0.001	W	
	Timer output	—	—	0.002	W	

NOTE

$AV_{DD}n$ (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V

Table 11. Reset Signals DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3 V supply.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR1 and DDR2 SDRAM interface of the MPC8323E. Note that DDR1 SDRAM is D*n*_GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is D*n*_GV_{DD}(typ) = 1.8 V. The AC electrical specifications are the same for DDR1 and DDR2 SDRAM.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8323E when D*n*_GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for D*n*_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MVREFn_{REF}	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	MVREFn_{REF} – 0.04	MVREFn_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MVREFn_{REF} + 0.125	D*n*_GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREFn_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.35 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. MVREFn_{REF} is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREFn_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREFn_{REF}. This rail should track variations in the DC level of MVREFn_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le$ D*n*_GV_{DD}.

Table 13 provides the DDR2 capacitance when D*n*_GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for D*n*_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1

Table 13. DDR2 SDRAM Capacitance for D*n*_GV$_{DD}$(typ) = 1.8 V

Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV$_{DD}$ = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25 °C, V_{OUT} = D*n*_GV$_{DD}$ ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR1 SDRAM component(s) of the MPC8323E when D*n*_GV$_{DD}$(typ) = 2.5 V.

Table 14. DDR1 SDRAM DC Electrical Characteristics for D*n*_GV$_{DD}$(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV$_{DD}$	2.375	2.625	V	1
I/O reference voltage	MVREF*n*$_{REF}$	0.49 × D*n*_GV$_{DD}$	0.51 × D*n*_GV$_{DD}$	V	2
I/O termination voltage	V_{TT}	MVREF*n*$_{REF}$ – 0.04	MVREF*n*$_{REF}$ + 0.04	V	3
Input high voltage	V_{IH}	MVREF*n*$_{REF}$ + 0.15	D*n*_GV$_{DD}$ + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF*n*$_{REF}$ – 0.15	V	—
Output leakage current	I_{OZ}	–9.9	–9.9	µA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Notes:
1. D*n*_GV$_{DD}$ is expected to be within 50 mV of the DRAM D*n*_GV$_{DD}$ at all times.
2. MVREF*n*$_{REF}$ is expected to be equal to 0.5 × D*n*_GV$_{DD}$, and to track D*n*_GV$_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n*$_{REF}$ may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF*n*$_{REF}$. This rail should track variations in the DC level of MVREF*n*$_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV$_{DD}$.

Table 15 provides the DDR1 capacitance D*n*_GV$_{DD}$(typ) = 2.5 V.

Table 15. DDR1 SDRAM Capacitance for D*n*_GV$_{DD}$(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ,DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV$_{DD}$ = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25° C, V_{OUT} = D*n*_GV$_{DD}$ ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR1 and DDR2 SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM (D*n*_GV_{DD}(typ) = 1.8 V).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with D*n*_GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MVREFn_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MVREFn_{REF} + 0.25	—	V	—

Table 17 provides the input AC timing specifications for the DDR1 SDRAM (D*n*_GV_{DD}(typ) = 2.5 V).

Table 17. DDR1 SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with D*n*_GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MVREFn_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MVREFn_{REF} + 0.31	—	V	—

Table 18 provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 18. DDR1 and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with D*n*_GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
266 MHz		–750	750		
200 MHz		–1250	1250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with D*n*_GV$_{DD}$ of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.9 1.0	 — —	ns	5
MDQ/MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100 1200	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock fall time	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

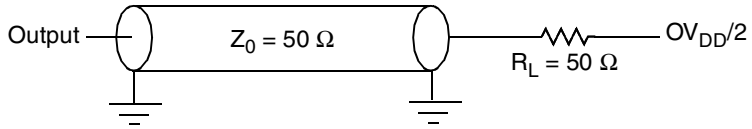


Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

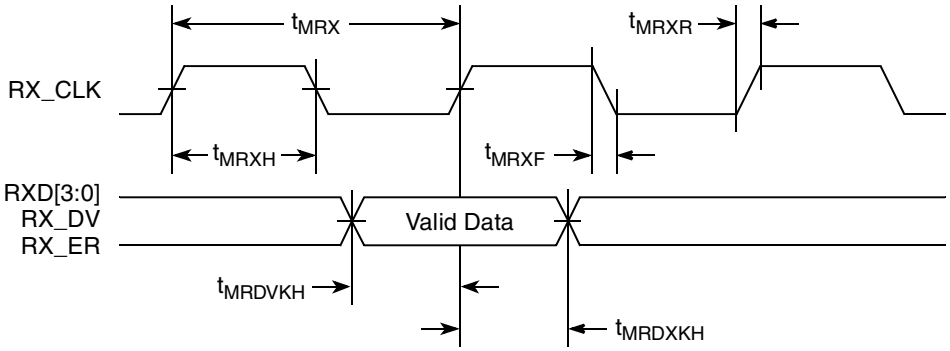


Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMII Transmit AC Timing Specifications

Table 23 provides the RMII transmit AC timing specifications.

Table 25. RMII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the RMII transmit AC timing diagram.

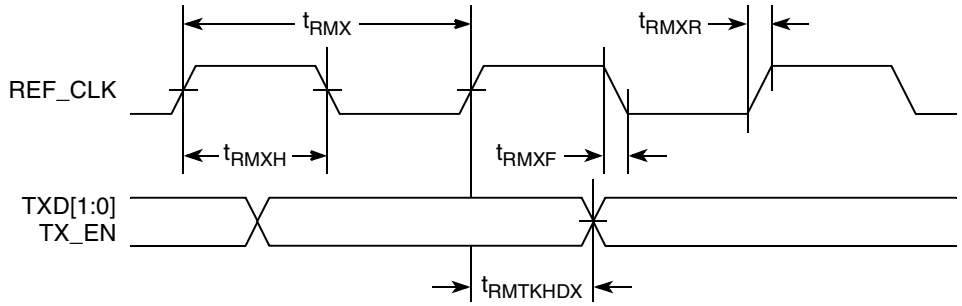


Figure 10. RMII Transmit AC Timing Diagram

8.2.2.2 RMII Receive AC Timing Specifications

Table 24 provides the RMII receive AC timing specifications.

Table 26. RMII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.10	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII Management AC Electrical Specifications

Table 28 provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 37 shows the PCI AC timing specifications at 33 MHz.

Table 37. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedence	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 25 provides the AC test load for PCI.

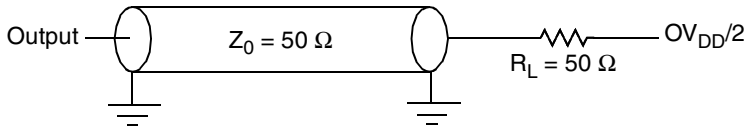


Figure 25. PCI AC Test Load

Figure 26 shows the PCI input AC timing conditions.

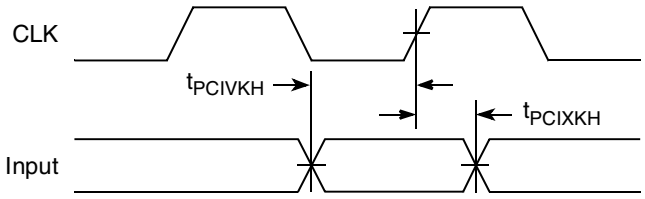


Figure 26. PCI Input AC Timing Measurement Conditions

Figure 27 shows the PCI output AC timing conditions.

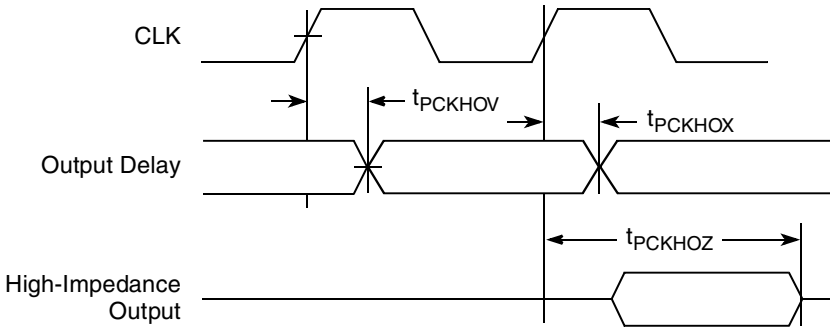


Figure 27. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8323E.

13.1 Timer DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the MPC8323E timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 38. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

13.2 Timer AC Timing Specifications

Table 39 provides the timer input and output AC timing specifications.

Table 39. Timer Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Figure 28 provides the AC test load for the timers.

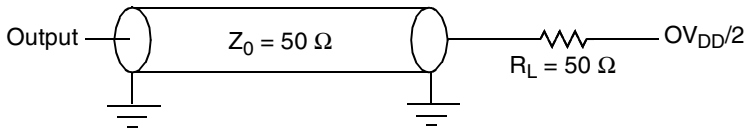


Figure 28. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8323E.

14.1 GPIO DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E GPIO.

Table 40. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

Table 41 provides the GPIO input and output AC timing specifications.

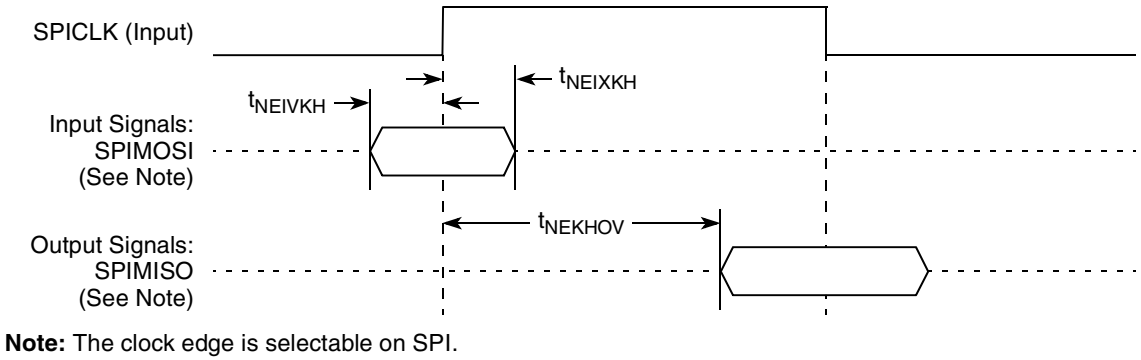
Table 41. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 31 and Figure 32 represent the AC timing from Table 45. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

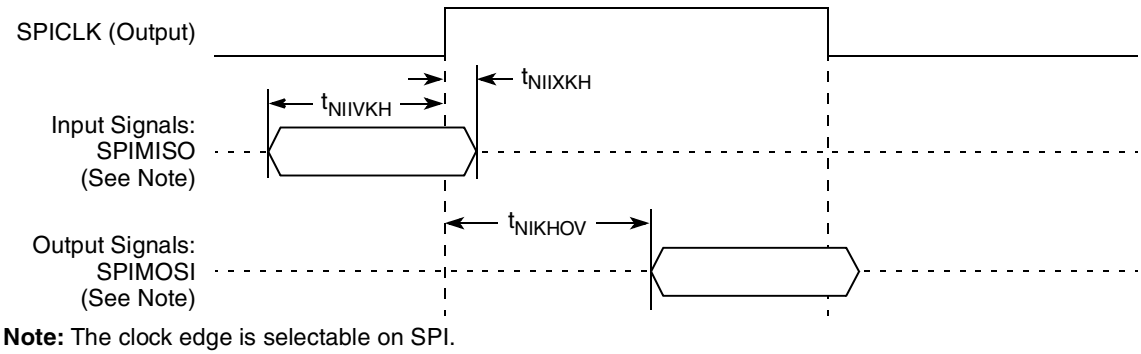
Figure 31 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 31. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 32 shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 32. SPI AC Timing in Master Mode (Internal Clock) Diagram

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8323E.

17.1 TDM/SI DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the MPC8323E TDM/SI.

Table 46. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	O	GV_{DD}	3
MEMC_MCK	AF14	O	GV_{DD}	—
$\overline{\text{MEMC\_MCK}}$	AE14	O	GV_{DD}	—
MEMC_MODT	AF11	O	GV_{DD}	—
Local Bus Controller Interface				
LAD0	N25	IO	OV_{DD}	7
LAD1	P26	IO	OV_{DD}	7
LAD2	P25	IO	OV_{DD}	7
LAD3	R26	IO	OV_{DD}	7
LAD4	R25	IO	OV_{DD}	7
LAD5	T26	IO	OV_{DD}	7
LAD6	T25	IO	OV_{DD}	7
LAD7	U25	IO	OV_{DD}	7
LAD8	M24	IO	OV_{DD}	7
LAD9	N24	IO	OV_{DD}	7
LAD10	P24	IO	OV_{DD}	7
LAD11	R24	IO	OV_{DD}	7
LAD12	T24	IO	OV_{DD}	7
LAD13	U24	IO	OV_{DD}	7
LAD14	U26	IO	OV_{DD}	7
LAD15	V26	IO	OV_{DD}	7
LA16	K25	O	OV_{DD}	7
LA17	L25	O	OV_{DD}	7
LA18	L26	O	OV_{DD}	7
LA19	L24	O	OV_{DD}	7
LA20	M26	O	OV_{DD}	7
LA21	M25	O	OV_{DD}	7
LA22	N26	O	OV_{DD}	7
LA23	AC24	O	OV_{DD}	7
LA24	AC25	O	OV_{DD}	7
LA25	AB23	O	OV_{DD}	7
$\overline{\text{LCS0}}$	AB24	O	OV_{DD}	4

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Supplies				
$AV_{DD}1$	P3	I	$AV_{DD}1$	—
$AV_{DD}2$	AA1	I	$AV_{DD}2$	—
$AV_{DD}3$	AB15	I	$AV_{DD}3$	—
$AV_{DD}4$	C24	I	$AV_{DD}4$	—
MVREF1	AB8	I	DDR reference voltage	—
MVREF2	AB17	I	DDR reference voltage	—
PCI				
$\overline{\text{PCI\_INTA}}$ /$\overline{\text{IRQ\_OUT}}$	AF2	O	OV_{DD}	2
$\overline{\text{PCI\_RESET\_OUT}}$	AE2	O	OV_{DD}	—
PCI_AD0/MSRCID0 (DDR ID)	L1	IO	OV_{DD}	—
PCI_AD1/MSRCID1 (DDR ID)	L2	IO	OV_{DD}	—
PCI_AD2/MSRCID2 (DDR ID)	M1	IO	OV_{DD}	—
PCI_AD3/MSRCID3 (DDR ID)	M2	IO	OV_{DD}	—
PCI_AD4/MSRCID4 (DDR ID)	L3	IO	OV_{DD}	—
PCI_AD5/MDVAL (DDR ID)	N1	IO	OV_{DD}	—
PCI_AD6	N2	IO	OV_{DD}	—
PCI_AD7	M3	IO	OV_{DD}	—
PCI_AD8	P1	IO	OV_{DD}	—
PCI_AD9	R1	IO	OV_{DD}	—
PCI_AD10	N3	IO	OV_{DD}	—
PCI_AD11	N4	IO	OV_{DD}	—
PCI_AD12	T1	IO	OV_{DD}	—
PCI_AD13	R2	IO	OV_{DD}	—
PCI_AD14/ECID_TMODE_IN	T2	IO	OV_{DD}	—
PCI_AD15	U1	IO	OV_{DD}	—
PCI_AD16	Y2	IO	OV_{DD}	—
PCI_AD17	Y1	IO	OV_{DD}	—
PCI_AD18	AA2	IO	OV_{DD}	—
PCI_AD19	AB1	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_AD20	AB2	IO	OV_{DD}	—
PCI_AD21	Y4	IO	OV_{DD}	—
PCI_AD22	AC1	IO	OV_{DD}	—
PCI_AD23	AA3	IO	OV_{DD}	—
PCI_AD24	AA4	IO	OV_{DD}	—
PCI_AD25	AD1	IO	OV_{DD}	—
PCI_AD26	AD2	IO	OV_{DD}	—
PCI_AD27	AB3	IO	OV_{DD}	—
PCI_AD28	AB4	IO	OV_{DD}	—
PCI_AD29	AE1	IO	OV_{DD}	—
PCI_AD30	AC3	IO	OV_{DD}	—
PCI_AD31	AC4	IO	OV_{DD}	—
PCI_C_$\overline{BE0}$	M4	IO	OV_{DD}	—
PCI_C_$\overline{BE1}$	T4	IO	OV_{DD}	—
PCI_C_$\overline{BE2}$	Y3	IO	OV_{DD}	—
PCI_C_$\overline{BE3}$	AC2	IO	OV_{DD}	—
PCI_PAR	U3	IO	OV_{DD}	—
$\overline{PCI\_FRAME}$	W1	IO	OV_{DD}	5
$\overline{PCI\_TRDY}$	W4	IO	OV_{DD}	5
$\overline{PCI\_IRDY}$	W2	IO	OV_{DD}	5
$\overline{PCI\_STOP}$	V4	IO	OV_{DD}	5
$\overline{PCI\_DEVSEL}$	W3	IO	OV_{DD}	5
PCI_IDSEL	P2	I	OV_{DD}	—
$\overline{PCI\_SERR}$	U4	IO	OV_{DD}	5
$\overline{PCI\_PERR}$	V3	IO	OV_{DD}	5
$\overline{PCI\_REQ0}$	AD4	IO	OV_{DD}	—
$\overline{PCI\_REQ1}$/CPCI_HS_ES	AE3	I	OV_{DD}	—
$\overline{PCI\_REQ2}$	AF3	I	OV_{DD}	—
$\overline{PCI\_GNT0}$	AD3	IO	OV_{DD}	—
$\overline{PCI\_GNT1}$/CPCI_HS_LED	AE4	O	OV_{DD}	—
$\overline{PCI\_GNT2}$/CPCI_HS_ENUM	AF4	O	OV_{DD}	—
M66EN	L4	I	OV_{DD}	—

22.1 Clocking in PCI Host Mode

When the MPC8323E is configured as a PCI host device (RCWH[PCIHOST] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexors. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

22.1.1 PCI Clock Outputs (PCI_CLK_OUT[0:2])

When the MPC8323E is configured as a PCI host, it provides three separate clock output signals, PCI_CLK_OUT[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOE*n*] bit. All output clocks are phase-aligned to each other.

22.2 Clocking in PCI Agent Mode

When the MPC8323E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND, and the clock output signals, PCI_CLK_OUT*n* and PCI_SYNC_OUT, are not used.

22.3 System Clock Domains

As shown in Figure 43, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*ce_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lb_clk*)

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = [\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})] \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\text{CFG\_CLKIN\_DIV}}$) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300c2 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See the “Reset Configuration” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 59. CSB Frequency Options

CFG_CLKIN_DIV_B at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
High	0010	2 : 1			133
High	0011	3 : 1		100	
High	0100	4 : 1	100	133	
High	0101	5 : 1	125		
High	0110	6 : 1			
High	0111	7 : 1			
High	1000	8 : 1			
High	1001	9 : 1			
High	1010	10 : 1			
High	1011	11 : 1			
High	1100	12 : 1			
High	1101	13 : 1			
High	1110	14 : 1			
High	1111	15 : 1			
High	0000	16 : 1			
Low	0010	2 : 1			133
Low	0011	3 : 1		100	
Low	0100	4 : 1		133	
Low	0101	5 : 1			
Low	0110	6 : 1			
Low	0111	7 : 1			
Low	1000	8 : 1			
Low	1001	9 : 1			
Low	1010	10 : 1			
Low	1011	11 : 1			
Low	1100	12 : 1			
Low	1101	13 : 1			
Low	1110	14 : 1			
Low	1111	15 : 1			
Low	0000	16 : 1			

1 CFG_CLKIN_DIV_B is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV_B must be pulled up (high) in agent mode.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

22.7 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8323E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 63 shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

Table 63. Suggested PLL Configurations

Conf No.	SPMF	Core PLL	CEMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0110	0	33.33	133.33	266.66	200
2	0100	0000101	1000	0	25	100	250	200
3	0010	0000100	0011	0	66.67	133.33	266.66	200
4	0100	0000101	0110	0	33.33	133.33	333.33	200
5	0101	0000101	1000	0	25	125	312.5	200
6	0010	0000101	0011	0	66.67	133.33	333.33	200

23 Thermal

This section describes the thermal specifications of the MPC8323E.

23.1 Thermal Characteristics

Table 64 provides the package thermal characteristics for the 516 27×27 mm PBGA of the MPC8323E.

Table 64. Package Thermal Characteristics for PBGA

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	21	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	23	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	13	°C/W	4
Junction-to-case	—	$R_{\theta JC}$	9	°C/W	5