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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8323czqafdc

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8323E. The MPC8323E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DDn}	–0.3 to 1.26	V	—
DDR1 and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
PCI, local bus, DUART, system control and power management, I ² C, SPI, MII, RMII, MII management, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.6	V	—
Input voltage	DDR1/DDR2 DRAM signals	MV_{IN}	–0.3 to ($GV_{DD} + 0.3$)	V	2
	DDR1/DDR2 DRAM reference	MV_{REF}	–0.3 to ($GV_{DD} + 0.3$)	V	2
	Local bus, DUART, CLKIN, system control and power management, I ² C, SPI, and JTAG signals	OV_{IN}	–0.3 to ($OV_{DD} + 0.3$)	V	3
	PCI	OV_{IN}	–0.3 to ($OV_{DD} + 0.3$)	V	5
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

- Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	$OV_{DD} = 3.3 \text{ V}$
PCI signals	25	
DDR1 signal	18	$GV_{DD} = 2.5 \text{ V}$
DDR2 signal	18	$GV_{DD} = 1.8 \text{ V}$
DUART, system control, I2C, SPI, JTAG	42	$OV_{DD} = 3.3 \text{ V}$
GPIO signals	42	$OV_{DD} = 3.3 \text{ V}$

2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input capacitance for all pins except CLKIN	C_I	6	8	pF	—
Input capacitance for CLKIN	$C_{I\text{CLKIN}}$	10	—	pF	1

Note:

1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and IO supply voltages (GV_{DD} and OV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} and OV_{DD}) and assert **PORESET** before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating **PORESET**.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD} and OV_{DD}) do not have any ordering requirements with respect to one another.

Table 6. Estimated Typical I/O Power Dissipation (continued)

Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 32 bits	—	—	0.12	W	—
PCI I/O load = 30 pF	66 MHz, 32 bits	—	—	0.057	W	—
QUICC Engine block and other I/Os	UTOPIA 8-bit 31 PHYs	—	—	0.041	W	Multiply by number of interfaces used.
	TDM serial	—	—	0.001	W	
	TDM nibble	—	—	0.004	W	
	HDLC/TRAN serial	—	—	0.003	W	
	HDLC/TRAN nibble	—	—	0.025	W	
	DUART	—	—	0.017	W	
	MIIs	—	—	0.009	W	
	RMII	—	—	0.009	W	
	Ethernet management	—	—	0.002	W	
	USB	—	—	0.001	W	
	SPI	—	—	0.001	W	
	Timer output	—	—	0.002	W	

NOTE

AV_{DDn} (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	$OV_{DD} + 0.3$	V
Input low voltage	—	V_{IL}	−0.3	0.4	V

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
$\overline{\text{HRESET}}/\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

1. $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is in PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{\text{OH}} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$\text{OV}_{\text{DD}} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR1 and DDR2 SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM ($Dn_GV_{DD}(typ) = 1.8\text{ V}$).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with Dn_GV_{DD} of $1.8 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MVREFn_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MVREFn_{REF} + 0.25$	—	V	—

Table 17 provides the input AC timing specifications for the DDR1 SDRAM ($Dn_GV_{DD}(typ) = 2.5\text{ V}$).

Table 17. DDR1 SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with Dn_GV_{DD} of $2.5 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MVREFn_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MVREFn_{REF} + 0.31$	—	V	—

Table 18 provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 18. DDR1 and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with Dn_GV_{DD} of $(1.8\text{ or }2.5\text{ V}) \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
266 MHz		–750	750		
200 MHz		–1250	1250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

Figure 4 shows the input timing diagram for the DDR controller.

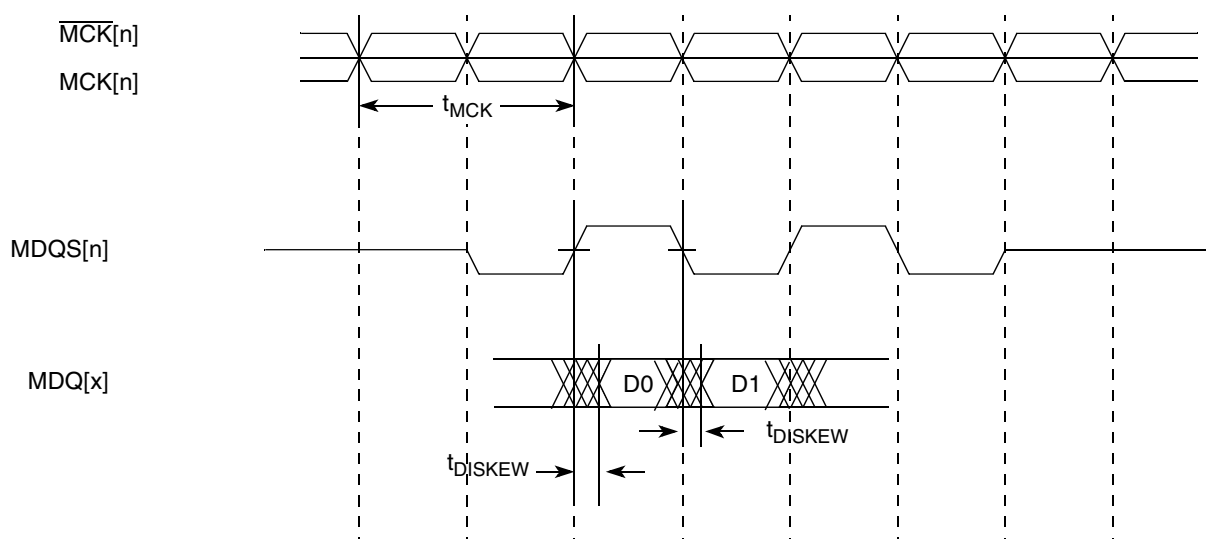


Figure 4. DDR Input Timing Diagram

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

Table 19 provides the output AC timing specifications for the DDR1 and DDR2 SDRAM interfaces.

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with Dn_GV_{DD} of (1.8 or 2.5 V) \pm 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK cycle time, (MCK/ $\overline{\text{MCK}}$ crossing)	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	2.5 3.5	— —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHAX}	2.5 3.5	— —	ns	3
$\overline{\text{MCS}}$ output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	2.5 3.5	— —	ns	3
$\overline{\text{MCS}}$ output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	2.5 3.5	— —	ns	3
MCK to MDQS Skew	t_{DDKMHM}	-0.6	0.6	ns	4

Table 23. MII Transmit AC Timing Specifications (continued)

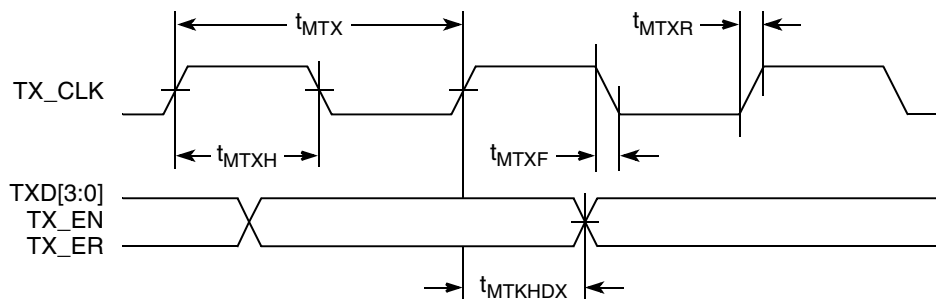
At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
TX_CLK data clock fall time	t_{MTXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 7 shows the MII transmit AC timing diagram.


Figure 7. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time	t_{MRXR}	1.0	—	4.0	ns

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

Table 33. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V _{IH}	0.7 × OV _{DD}	OV _{DD} + 0.3	V	—
Input low voltage level	V _{IL}	−0.3	0.3 × OV _{DD}	V	—
Low level output voltage	V _{OL}	0	0.4	V	1
Output fall time from V _{IH} (min) to V _{IL} (max) with a bus capacitance from 10 to 400 pF	t _{I2CLKV}	20 + 0.1 × C _B	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C _I	—	10	pF	—
Input current (0 V ≤ V _{IN} ≤ OV _{DD})	I _{IN}	—	±5	μA	4

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I²C interface of the MPC8323E.

Table 34. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol ¹	Min	Max	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL}	1.3	—	μs
High period of the SCL clock	t _{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	—	μs
Data setup time	t _{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	— 0 ²	— 0.9 ³	μs

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8323E.

12.1 PCI DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the PCI interface of the MPC8323E.

Table 35. PCI DC Electrical Characteristics^{1,2}

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL} \text{ (max)}$	-0.3	0.8	V
High-level output voltage	V_{OH}	$OV_{DD} = \text{min},$ $I_{OH} = -100 \mu\text{A}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	$OV_{DD} = \text{min},$ $I_{OL} = 100 \mu\text{A}$	—	0.2	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

Notes:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.
- Ranges listed do not meet the full range of the DC specifications of the *PCI 2.3 Local Bus Specifications*.

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8323E. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8323E is configured as a host or agent device. Table 36 shows the PCI AC timing specifications at 66 MHz.

Table 36. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.

Table 37 shows the PCI AC timing specifications at 33 MHz.

Table 37. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 25 provides the AC test load for PCI.

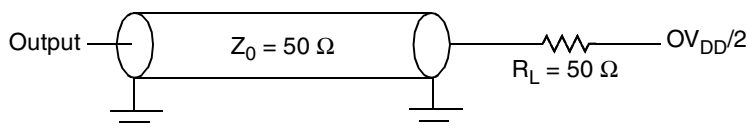


Figure 25. PCI AC Test Load

Figure 26 shows the PCI input AC timing conditions.

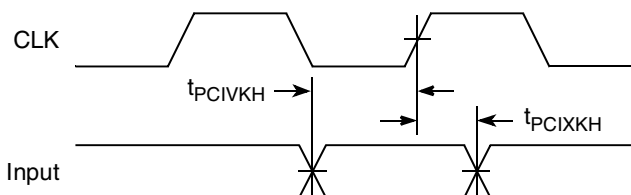


Figure 26. PCI Input AC Timing Measurement Conditions

Figure 27 shows the PCI output AC timing conditions.

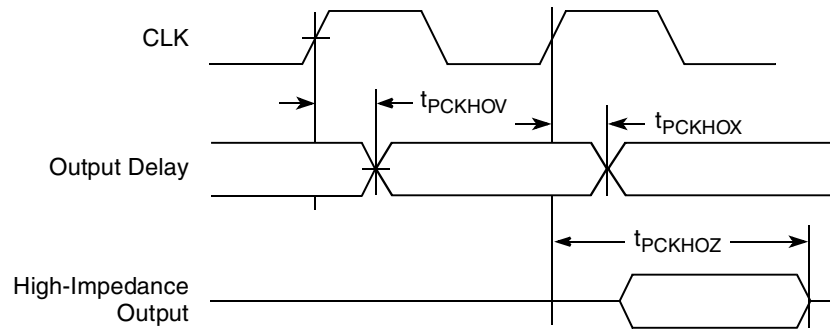


Figure 27. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8323E.

13.1 Timer DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the MPC8323E timer pins, including TIN , \overline{TOUT} , $TGATE$, and RTC_CLK .

Table 38. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

13.2 Timer AC Timing Specifications

Table 39 provides the timer input and output AC timing specifications.

Table 39. Timer Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Figure 28 provides the AC test load for the timers.

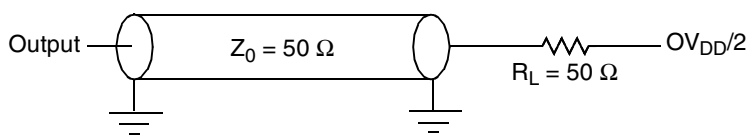


Figure 28. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8323E.

14.1 GPIO DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E GPIO.

Table 40. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA	—

Note:

1. This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

Table 41 provides the GPIO input and output AC timing specifications.

Table 41. GPIO Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 29 provides the AC test load for the GPIO.

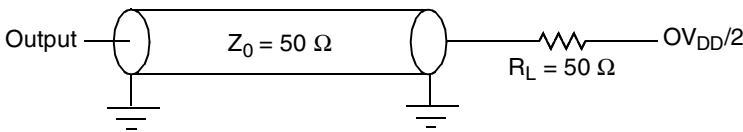


Figure 29. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8323E.

15.1 IPIC DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the external interrupt pins of the MPC8323E.

Table 42. IPIC DC Electrical Characteristics^{1,2}

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	—	—	± 5	μA
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

Notes:

1. This table applies for pins $\overline{IRQ}[0:7]$, $\overline{IRQ_OUT}$, $\overline{MCP_OUT}$, and CE ports Interrupts.
2. $\overline{IRQ_OUT}$ and $\overline{MCP_OUT}$ are open drain pins, thus V_{OH} is not relevant for those pins.

15.2 IPIC AC Timing Specifications

Table 43 provides the IPIC input and output AC timing specifications.

Table 43. IPIC Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Table 44. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	$t_{NIKH OV}$	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	$t_{NEKH OV}$	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{NIKH OV}$ symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 30 provides the AC test load for the SPI.

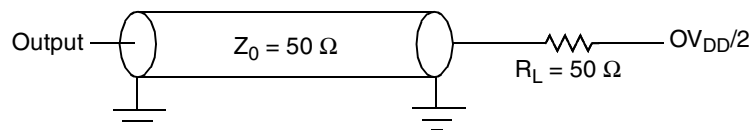
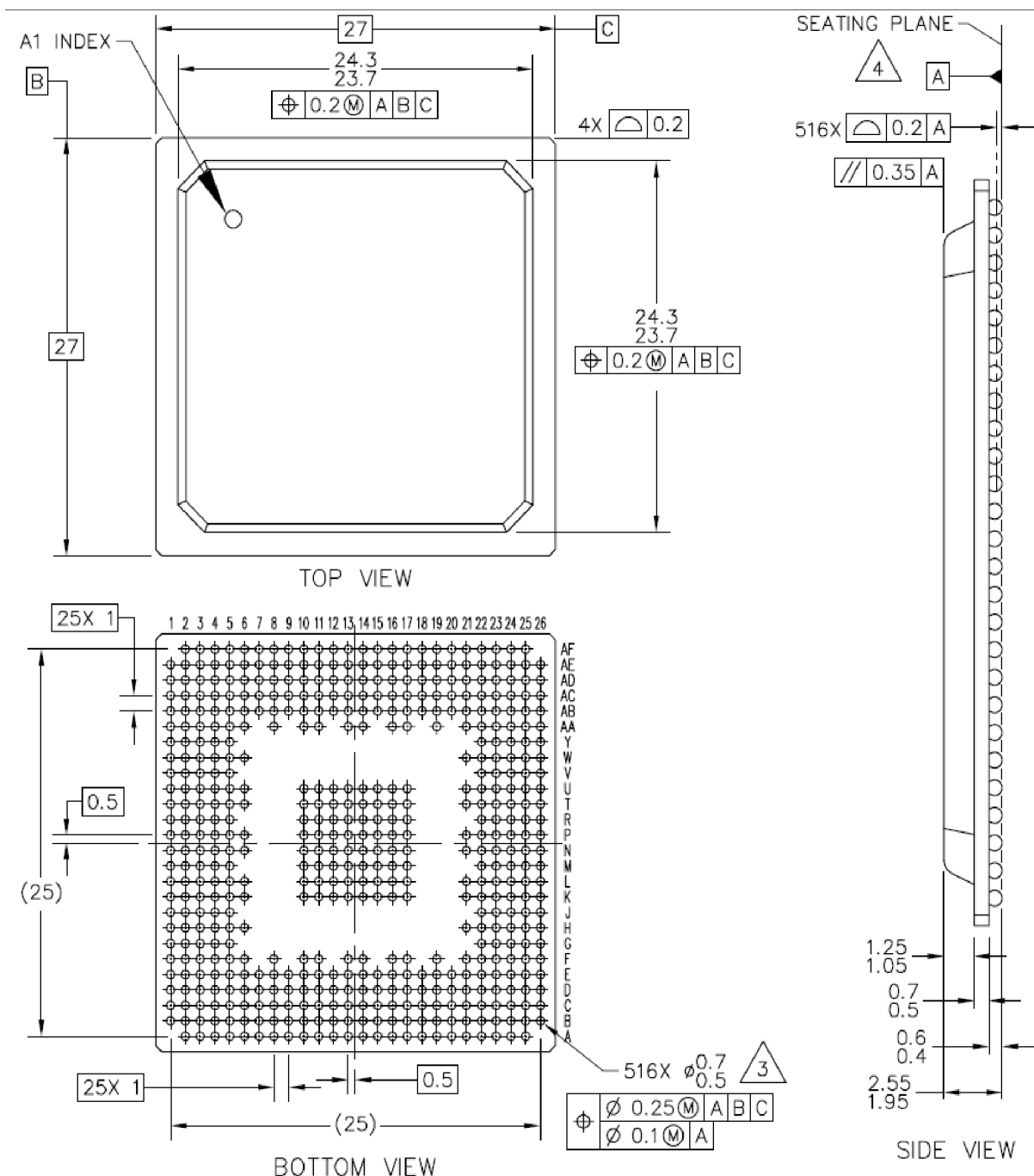


Figure 30. SPI AC Test Load



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 42. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8323E PBGA

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LCS1}}$	AB25	O	OV_{DD}	4
$\overline{\text{LCS2}}$	AA23	O	OV_{DD}	4
$\overline{\text{LCS3}}$	AA24	O	OV_{DD}	4
$\overline{\text{LWE0}}$	Y23	O	OV_{DD}	4
$\overline{\text{LWE1}}$	W25	O	OV_{DD}	4
LBCTL	V25	O	OV_{DD}	4
LALE	V24	O	OV_{DD}	7
CFG_RESET_SOURCE[0]/LSDA10/LGPL0	L23	IO	OV_{DD}	—
CFG_RESET_SOURCE[1]/ $\overline{\text{LSDWE}}$ /LGPL1	K23	IO	OV_{DD}	—
$\overline{\text{LSDRAS}}$ /LGPL2/ $\overline{\text{LOE}}$	J23	O	OV_{DD}	4
CFG_RESET_SOURCE[2]/ $\overline{\text{LSDCAS}}$ /LGPL3	H23	IO	OV_{DD}	—
LGPL4/ $\overline{\text{LGTA}}$ /LUPWAIT/LPBSE	G23	IO	OV_{DD}	4, 8
LGPL5	AC22	O	OV_{DD}	4
LCLK0	Y24	O	OV_{DD}	7
LCLK1	Y25	O	OV_{DD}	7
DUART				
UART_SOUT1/MSRCID0 (DDR ID)/LSRCID0	G1	IO	OV_{DD}	—
UART_SIN1/MSRCID1 (DDR ID)/LSRCID1	G2	IO	OV_{DD}	—
$\overline{\text{UART_CTS1}}$ /MSRCID2 (DDR ID)/LSRCID2	H3	IO	OV_{DD}	—
$\overline{\text{UART_RTS1}}$ /MSRCID3 (DDR ID)/LSRCID3	K3	IO	OV_{DD}	—
UART_SOUT2/MSRCID4 (DDR ID)/LSRCID4	H2	IO	OV_{DD}	—
UART_SIN2/MDVAL (DDR ID)/LDVAL	H1	IO	OV_{DD}	—
$\overline{\text{UART_CTS2}}$	J3	IO	OV_{DD}	—
$\overline{\text{UART_RTS2}}$	K4	IO	OV_{DD}	—
I²C interface				
IIC_SDA/ $\overline{\text{CKSTOP_OUT}}$	AE24	IO	OV_{DD}	2
IIC_SCL/ $\overline{\text{CKSTOP_IN}}$	AF24	IO	OV_{DD}	2
Programmable Interrupt Controller				
$\overline{\text{MCP_OUT}}$	AD25	O	OV_{DD}	—
$\overline{\text{IRQ0/MCP_IN}}$	AD26	I	OV_{DD}	—
$\overline{\text{IRQ1}}$	K1	IO	OV_{DD}	—
$\overline{\text{IRQ2}}$	K2	I	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_AD20	AB2	IO	OV _{DD}	—
PCI_AD21	Y4	IO	OV _{DD}	—
PCI_AD22	AC1	IO	OV _{DD}	—
PCI_AD23	AA3	IO	OV _{DD}	—
PCI_AD24	AA4	IO	OV _{DD}	—
PCI_AD25	AD1	IO	OV _{DD}	—
PCI_AD26	AD2	IO	OV _{DD}	—
PCI_AD27	AB3	IO	OV _{DD}	—
PCI_AD28	AB4	IO	OV _{DD}	—
PCI_AD29	AE1	IO	OV _{DD}	—
PCI_AD30	AC3	IO	OV _{DD}	—
PCI_AD31	AC4	IO	OV _{DD}	—
PCI_C_BE0	M4	IO	OV _{DD}	—
PCI_C_BE1	T4	IO	OV _{DD}	—
PCI_C_BE2	Y3	IO	OV _{DD}	—
PCI_C_BE3	AC2	IO	OV _{DD}	—
PCI_PAR	U3	IO	OV _{DD}	—
PCI_FRAME	W1	IO	OV _{DD}	5
PCI_TRDY	W4	IO	OV _{DD}	5
PCI_IRDY	W2	IO	OV _{DD}	5
PCI_STOP	V4	IO	OV _{DD}	5
PCI_DEVSEL	W3	IO	OV _{DD}	5
PCI_IDSEL	P2	I	OV _{DD}	—
PCI_SERR	U4	IO	OV _{DD}	5
PCI_PERR	V3	IO	OV _{DD}	5
PCI_REQ0	AD4	IO	OV _{DD}	—
PCI_REQ1/CPCI_HS_ES	AE3	I	OV _{DD}	—
PCI_REQ2	AF3	I	OV _{DD}	—
PCI_GNT0	AD3	IO	OV _{DD}	—
PCI_GNT1/CPCI_HS_LED	AE4	O	OV _{DD}	—
PCI_GNT2/CPCI_HS_ENUM	AF4	O	OV _{DD}	—
M66EN	L4	I	OV _{DD}	—

22.1 Clocking in PCI Host Mode

When the MPC8323E is configured as a PCI host device ($RCWH[PCIHOST] = 1$), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider ($\div 2$) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexors. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

22.1.1 PCI Clock Outputs (PCI_CLK_OUT[0:2])

When the MPC8323E is configured as a PCI host, it provides three separate clock output signals, PCI_CLK_OUT[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOEn] bit. All output clocks are phase-aligned to each other.

22.2 Clocking in PCI Agent Mode

When the MPC8323E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND, and the clock output signals, PCI_CLK_OUTn and PCI_SYNC_OUT, are not used.

22.3 System Clock Domains

As shown in [Figure 43](#), the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*ce_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lb_clk*)

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = [PCI_SYNC_IN \times (1 + \sim \overline{CFG_CLKIN_DIV})] \times SPMF$$

In PCI host mode, $PCI_SYNC_IN \times (1 + \sim \overline{CFG_CLKIN_DIV})$ is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300c2 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See the “Reset Configuration” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

Table 57. Operating Frequencies for PBGA (continued)

Characteristic ¹	Max Operating Frequency	Unit
DDR1/DDR2 memory bus frequency (MCLK) ²	133	MHz
Local bus frequency (LCLK _n) ³	66	MHz
PCI input frequency (CLKIN or PCI_CLK)	66	MHz

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.

² The DDR1/DDR2 data rate is 2x the DDR1/DDR2 memory bus frequency.

³ The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

22.4 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 300–600 MHz.

Table 58. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

As described in Section 22, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59

25.2 Part Marking

Parts are marked as in the example shown in [Figure 46](#).

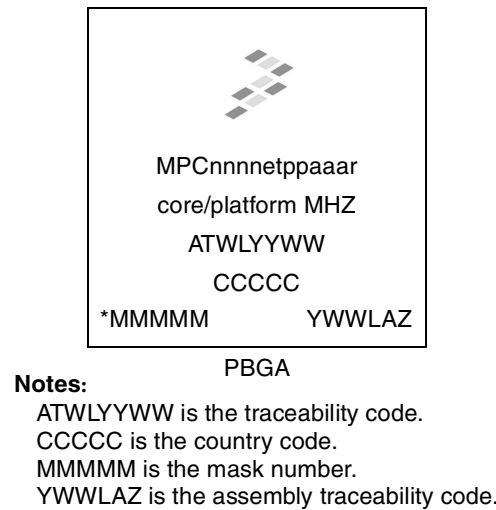


Figure 46. Freescale Part Marking for PBGA Devices

26 Document Revision History

[Table 67](#) provides a revision history for this hardware specification.

Table 67. Document Revision History

Rev. No.	Date	Substantive Change(s)
4	09/2010	<ul style="list-style-type: none"> Replaced all instances of “LCCR” with “LCRR” throughout. Added footnotes 3 and 4 in Table 2, “Recommended Operating Conditions³.” Modified Section 8.1.1, “DC Electrical Characteristics.” Modified Table 23, “MII Transmit AC Timing Specifications.” Modified Table 24, “MII Receive AC Timing Specifications.” Added footnote 7 and 8, and modified some signal names in Table 55, “MPC8323E PBGA Pinout Listing.”
3	12/2009	<ul style="list-style-type: none"> Removed references for note 4 from Table 1. Added Figure 2 in Section 2.1.2, “Power Supply Voltage Specification. Added symbol T_A in Table 2. Added footnote 2 in Table 2. Added a note in Section 4, “Clock Input Timing for rise/fall time of QE input pins. Modified CLKIN, PCI_CLK rise/fall time parameters in Table 8. Modified min value of t_{MCK} in Table 19. Modified Figure 43. Modified formula for ce_clk calculation in Section 22.3, “System Clock Domains. Added a note in Section 22.4, “System PLL Configuration. Removed the signal ECID_TMODE_IN from Table 55. Removed all references of RST signals from Table 55.