



#### Welcome to E-XFL.COM

#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8323ecvraddc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### NOTE

The QUICC Engine block can also support a UTOPIA level 2 capable of supporting 31 multi-PHY (MPC8323E- and MPC8323-specific).

The MPC8323E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In summary, the MPC8323E family provides users with a highly integrated, fully programmable communications processor. This helps ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

## 1.1 MPC8323E Features

Major features of the MPC8323E are as follows:

- High-performance, low-power, and cost-effective single-chip data-plane/control-plane solution for ATM or IP/Ethernet packet processing (or both).
- MPC8323E QUICC Engine block offers a future-proof solution for next generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards.
- Single platform architecture supports the convergence of IP packet networks and ATM networks.
- DDR1/DDR2 memory controller—one 32-bit interface at up to 266 MHz supporting both DDR1 and DDR2.
- An e300c2 core built on Power Architecture technology with 16-Kbyte instruction and data caches, and dual integer units.
- Peripheral interfaces such as 32-bit PCI (2.2) interface up to 66-MHz operation, 16-bit local bus interface up to 66-MHz operation, and USB 2.0 (full-/low-speed).
- Security engine provides acceleration for control and data plane security protocols.
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration.

## 1.1.1 Protocols

The protocols are as follows:

- ATM SAR up to 155 Mbps (OC-3) full duplex, with ATM traffic shaping (ATF TM4.1)
- Support for ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- Support for IMA and ATM transmission convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- Support for 64 channels of HDLC/transparent





## 1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i<sup>TM</sup> standard, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

## 1.4 DDR Memory Controller

The MPC8323E DDR1/DDR2 memory controller includes the following features:

- Single 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266-MHz data rate
- Support for two ×16 devices
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O
- Support for 1 chip select only
- FCRAM, ECC, hardware/software calibration, bit deskew, QIN stage, or atomic logic are not supported.

## 1.5 PCI Controller

The MPC8323E PCI controller includes the following features:

- PCI Specification Revision 2.3 compatible
- Single 32-bit data PCI interface operates up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

## **1.6 Programmable Interrupt Controller (PIC)**

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 35 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.





## 2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8323E. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V <sub>DD</sub>	1.0 V ± 50 mV	V	1
PLL supply voltage	AV <sub>DD</sub>	1.0 V ± 50 mV	V	1
DDR1 and DDR2 DRAM I/O voltage	GV <sub>DD</sub>	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
PCI, local bus, DUART, system control and power management, I <sup>2</sup> C, SPI, and JTAG I/O voltage	OV <sub>DD</sub>	3.3 V ± 300 mV	V	1
Junction temperature	T <sub>A</sub> /T <sub>J</sub>	0 to 105	°C	2

#### Table 2. Recommended Operating Conditions<sup>3</sup>

Note:

1. GV<sub>DD</sub>, OV<sub>DD</sub>, AV<sub>DD</sub>, and V<sub>DD</sub> must track each other and must vary in the same direction—either in the positive or negative direction.

2. Minimum temperature is specified with T<sub>A</sub>; maximum temperature is specified with T<sub>J</sub>.

3. All IO pins should be interfaced with peripherals operating at same voltage level.

4. This voltage is the input to the filter discussed in Section 24.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced due to voltage drop across the filter.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8323E



Figure 2. Overshoot/Undershoot Voltage for GV<sub>DD</sub>/OV<sub>DD</sub>



Electrical Characteristics

## 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV <sub>DD</sub> = 3.3 V
PCI signals	25	
DDR1 signal	18	GV <sub>DD</sub> = 2.5 V
DDR2 signal	18	GV <sub>DD</sub> = 1.8 V
DUART, system control, I2C, SPI, JTAG	42	OV <sub>DD</sub> = 3.3 V
GPIO signals	42	OV <sub>DD</sub> = 3.3 V

Table 3. Output Drive Capability

## 2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

**Table 4. Input Capacitance Specification** 

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input capacitance for all pins except CLKIN	CI	6	8	pF	_
Input capacitance for CLKIN	C <sub>ICLKIN</sub>	10		pF	1

Note:

1. The external clock generator should be able to drive 10 pF.

## 2.2 Power Sequencing

The device does not require the core supply voltage  $(V_{DD})$  and IO supply voltages  $(GV_{DD})$  and  $OV_{DD})$  to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage  $(V_{DD})$  before the I/O voltage  $(GV_{DD})$  and  $OV_{DD}$  and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies  $(GV_{DD})$  and  $OV_{DD}$  do not have any ordering requirements with respect to one another.



CLKIN input current	$0 \ V \leq V_{IN} \leq OV_{DD}$	I <sub>IN</sub>	_	±5	μA
PCI_SYNC_IN input current	$\begin{array}{c} 0 \ V \leq V_{IN} \leq 0.5 \ V \ or \\ OV_{DD} - 0.5 \ V \leq V_{IN} \leq OV_{DD} \end{array}$	I <sub>IN</sub>	_	±5	μA
PCI_SYNC_IN input current	$0.5~V \leq V_{IN} \leq OV_{DD} - 0.5~V$	I <sub>IN</sub>	—	±50	μA

## 4.2 AC Electrical Characteristics

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI\_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 8 provides the clock input (CLKIN/PCI\_CLK) AC timing specifications for the MPC8323E.

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
CLKIN/PCI_CLK frequency	f <sub>CLKIN</sub>	25	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t <sub>CLKIN</sub>	15	—	—	ns	—
CLKIN rise and fall time	t <sub>KH</sub> , t <sub>KL</sub>	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t <sub>PCH</sub> , t <sub>PCL</sub>	0.6	0.8	1.2	ns	2
CLKIN/PCI_CLK duty cycle	t <sub>KHK</sub> /t <sub>CLKIN</sub>	40	—	60	%	3
CLKIN/PCI_CLK jitter		—	—	±150	ps	4, 5

**Table 8. CLKIN AC Timing Specifications** 

Notes:

1. **Caution:** The system, core, security, and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.

2. Rise and fall times for CLKIN/PCI\_CLK are measured at 0.4 and 2.7 V.

3. Timing is guaranteed by design and characterization.

4. This represents the total input jitter—short term and long term—and is guaranteed by design.

5. The CLKIN/PCI\_CLK driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

## 5 **RESET Initialization**

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8323E. Table 9 provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET Initialization Timir	g Specifications
-------------------------------------	------------------

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overrightarrow{\text{HRESET}}$ or $\overrightarrow{\text{SRESET}}$ (input) to activate reset flow	32	_	t <sub>PCI_SYNC_IN</sub>	1
Required assertion time of $\overrightarrow{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8323E is in PCI host mode	32		t <sub>CLKIN</sub>	2
Required assertion time of PORESET with stable clock applied to PCI_SYNC_IN when the MPC8323E is in PCI agent mode	32	_	<sup>t</sup> PCI_SYNC_IN	1



DDR1 and DDR2 SDRAM

Table 11. Reset Signals DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Input current	I <sub>IN</sub>	$0 \ V \leq V_{IN} \leq OV_{DD}$		±5	μA	—

Note:

1. This specification applies when operating from 3.3 V supply.

# 6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR1 and DDR2 SDRAM interface of the MPC8323E. Note that DDR1 SDRAM is  $Dn_GV_{DD}(typ) = 2.5$  V and DDR2 SDRAM is  $Dn_GV_{DD}(typ) = 1.8$  V. The AC electrical specifications are the same for DDR1 and DDR2 SDRAM.

## 6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8323E when  $Dn_GV_{DD}(typ) = 1.8 \text{ V}$ .

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	D <i>n_</i> GV <sub>DD</sub>	1.71	1.89	V	1
I/O reference voltage	MVREF <i>n</i> REF	$0.49 \times Dn_GV_{DD}$	$0.49 \times Dn_GV_{DD}$ $0.51 \times Dn_GV_{DD}$		2
I/O termination voltage	V <sub>TT</sub>	MVREFn <sub>REF</sub> – 0.04	MVREF <i>n</i> <sub>REF</sub> + 0.04	V	3
Input high voltage	V <sub>IH</sub>	MVREFn <sub>REF</sub> + 0.125	D <i>n_</i> GV <sub>DD</sub> + 0.3	V	—
Input low voltage	V <sub>IL</sub>	-0.3	MVREFn <sub>REF</sub> – 0.125	V	—
Output leakage current	I <sub>OZ</sub>	-9.9	9.9	μA	4
Output high current (V <sub>OUT</sub> = 1.35 V)	I <sub>ОН</sub>	-13.4	—	mA	—
Output low current (V <sub>OUT</sub> = 0.280 V)	I <sub>OL</sub>	13.4	—	mA	—

Table 12. DDR2 SDRAM DC Electrical Characteristics for Dn\_GV<sub>DD</sub>(typ) = 1.8 V

#### Notes:

1.  $Dn_GV_{DD}$  is expected to be within 50 mV of the DRAM  $Dn_GV_{DD}$  at all times.

- 2. MVREF  $n_{\text{REF}}$  is expected to be equal to  $0.5 \times Dn_{\text{GV}_{\text{DD}}}$ , and to track  $Dn_{\text{GV}_{\text{DD}}}$  DC variations as measured at the receiver. Peak-to-peak noise on MVREF  $n_{\text{REF}}$  may not exceed ±2% of the DC value.
- 3. V<sub>TT</sub> is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF*n*<sub>REF</sub>. This rail should track variations in the DC level of MVREF*n*<sub>REF</sub>.

4. Output leakage is measured with all outputs disabled, 0 V  $\leq$  V<sub>OUT</sub>  $\leq$  Dn\_GV<sub>DD</sub>.

Table 13 provides the DDR2 capacitance when  $Dn_GV_{DD}(typ) = 1.8$  V.

#### Table 13. DDR2 SDRAM Capacitance for Dn\_GV<sub>DD</sub>(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C <sub>IO</sub>	6	8	pF	1



#### **Ethernet and MII Management**

#### Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with  $\text{OV}_{\text{DD}}$  of 3.3 V  $\pm$  10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typical	Мах	Unit
RX_CLK clock fall time	t <sub>MRXF</sub>	1.0	_	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>MRDVKH</sub> symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>MRX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>MRDXKL</sub> symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>MRX</sub> clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>MRX</sub> represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>

Figure 8 provides the AC test load.



Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.



Figure 9. MII Receive AC Timing Diagram

## 8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.



Local Bus

Figure 13 shows the MII management AC timing diagram.



Figure 13. MII Management Interface Timing Diagram

# 9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8323E.

## 9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics
---

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V <sub>IH</sub>	2	OV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V
High-level output voltage, I <sub>OH</sub> = −100 μA	V <sub>OH</sub>	OV <sub>DD</sub> – 0.2	—	V
Low-level output voltage, I <sub>OL</sub> = 100 μA	V <sub>OL</sub>	—	0.2	V
Input current	I <sub>IN</sub>	—	±5	μA

## 9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8323E.

Table 30. Local Bus General Timing Parameters

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
Local bus cycle time	t <sub>LBK</sub>	15	—	ns	2
Input setup to local bus clock (LCLKn)	t <sub>LBIVKH</sub>	7	—	ns	3, 4
Input hold from local bus clock (LCLKn)	t <sub>LBIXKH</sub>	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t <sub>LBOTOT1</sub>	1.5	—	ns	5



Figure 15 through Figure 17 show the local bus signals.





Figure 17. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

# 10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1<sup>TM</sup> (JTAG) interface of the MPC8323E.

## **10.1 JTAG DC Electrical Characteristics**

Table 31 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E.

Table 31. JTAG	Interface D	OC Electrical	Characteristics
----------------	-------------	---------------	-----------------

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -6.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 6.0 mA	_	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	_	0.4	V
Input high voltage	V <sub>IH</sub>	—	2.5	OV <sub>DD</sub> + 0.3	V



# 12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8323E.

## 12.1 PCI DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the PCI interface of the MPC8323E.

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V <sub>IH</sub>	$V_{OUT} \ge V_{OH}$ (min) or	2	OV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	$V_{OUT} \le V_{OL}$ (max)	-0.3	0.8	V
High-level output voltage	V <sub>OH</sub>	OV <sub>DD</sub> = min, I <sub>OH</sub> = −100 μA	OV <sub>DD</sub> – 0.2	_	V
Low-level output voltage	V <sub>OL</sub>	OV <sub>DD</sub> = min, I <sub>OL</sub> = 100 μA	_	0.2	V
Input current	I <sub>IN</sub>	$0 V \le V_{IN} \le OV_{DD}$	_	±5	μA

#### Table 35. PCI DC Electrical Characteristics<sup>1,2</sup>

#### Notes:

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1 and Table 2.

2. Ranges listed do not meet the full range of the DC specifications of the PCI 2.3 Local Bus Specifications.

## 12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8323E. Note that the PCI\_CLK or PCI\_SYNC\_IN signal is used as the PCI input clock depending on whether the MPC8323E is configured as a host or agent device. Table 36 shows the PCI AC timing specifications at 66 MHz.

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Clock to output valid	t <sub>PCKHOV</sub>	_	6.0	ns	2
Output hold from clock	t <sub>PCKHOX</sub>	1	_	ns	2
Clock to output high impedence	t <sub>PCKHOZ</sub>	_	14	ns	2, 3
Input setup to clock	t <sub>PCIVKH</sub>	3.0	_	ns	2, 4
Input hold from clock	t <sub>PCIXKH</sub>	0	—	ns	2, 4

#### Table 36. PCI AC Timing Specifications at 66 MHz

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>PCIVKH</sub> symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI\_SYNC\_IN clock, t<sub>SYS</sub>, reference (K) going to the high (H) state or setup time. Also, t<sub>PCRHFV</sub> symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>

- 2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.



Figure 29 provides the AC test load for the GPIO.



## 15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8323E.

## **15.1 IPIC DC Electrical Characteristics**

Table 42 provides the DC electrical characteristics for the external interrupt pins of the MPC8323E.

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V <sub>IH</sub>	—	2.0	OV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	-0.3	0.8	V
Input current	I <sub>IN</sub>	—	—	±5	μA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 6.0 mA	_	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	0.4	V

Table 42. IPIC DC Electrical Characteristics<sup>1,2</sup>

#### Notes:

1. This table applies for pins IRQ[0:7], IRQ\_OUT, MCP\_OUT, and CE ports Interrupts.

2. IRQ\_OUT and MCP\_OUT are open drain pins, thus V<sub>OH</sub> is not relevant for those pins.

## 15.2 IPIC AC Timing Specifications

Table 43 provides the IPIC input and output AC timing specifications.

#### Table 43. IPIC Input AC Timing Specifications<sup>1</sup>

Characteristic	Symbol <sup>2</sup>	Min	Unit
IPIC inputs—minimum pulse width	t <sub>PIWID</sub>	20	ns

#### Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any
external synchronous logic. IPIC inputs are required to be valid for at least t<sub>PIWID</sub> ns to ensure proper operation when working
in edge triggered mode.



SPI

# 16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

## **16.1 SPI DC Electrical Characteristics**

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -6.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 6.0 mA	—	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	0.4	V
Input high voltage	V <sub>IH</sub>	—	2.0	OV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	-0.3	0.8	V
Input current	I <sub>IN</sub>	$0 \ V \le V_{IN} \le OV_{DD}$	—	±5	μA

#### Table 44. SPI DC Electrical Characteristics

## 16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications<sup>1</sup>

Characteristic	Symbol <sup>2</sup>	Min	Мах	Unit
SPI outputs—Master mode (internal clock) delay	t <sub>NIKHOV</sub>	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t <sub>NEKHOV</sub>	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t <sub>NIIVKH</sub>	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t <sub>NIIXKH</sub>	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t <sub>NEIVKH</sub>	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t <sub>NEIXKH</sub>	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t<sub>NIKHOV</sub> symbolizes the NMSI outputs internal timing (NI) for the time t<sub>SPI</sub> memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
</sub></sub>

Figure 30 provides the AC test load for the SPI.



Figure 30. SPI AC Test Load



Figure 35 provides the AC test load for the UTOPIA.



Figure 36 and Figure 37 represent the AC timing from Table 49. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 36 shows the UTOPIA timing with external clock.



Figure 36. UTOPIA AC Timing (External Clock) Diagram

Figure 37 shows the UTOPIA timing with internal clock.



Figure 37. UTOPIA AC Timing (Internal Clock) Diagram





# 19 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART of the MPC8323E.

## 19.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Table 50 provides the DC electrical characteristics for the MPC8323E HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 50. HDLC, BISYNC, Transparent, and	Synchronous UART DC Electrical Characteristics
--	--

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	_	0.5	V
Input high voltage	V <sub>IH</sub>	—	2.0	OV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	-0.3	0.8	V
Input current	I <sub>IN</sub>	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

# 19.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Table 51 provides the input and output AC timing specifications for HDLC, BISYNC, and transparent UART protocols.

Characteristic	Symbol <sup>2</sup>	Min	Мах	Unit
Outputs—Internal clock delay	t <sub>HIKHOV</sub>	0	5.5	ns
Outputs—External clock delay	t <sub>HEKHOV</sub>	1	10	ns
Outputs—Internal clock high impedance	t <sub>нікнох</sub>	0	5.5	ns
Outputs—External clock high impedance	t <sub>HEKHOX</sub>	1	8	ns
Inputs—Internal clock input setup time	t <sub>HIIVKH</sub>	6	—	ns
Inputs—External clock input setup time	t <sub>HEIVKH</sub>	4	—	ns
Inputs—Internal clock input hold time	t <sub>нихкн</sub>	0	—	ns

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications<sup>1</sup>



Package and Pin Listings

#### Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
CE/GPIO					
GPIO_PA0/SER1_TXD[0]/TDMA_TXD[0]/USBTXN	G3	IO	OV <sub>DD</sub>	_	
GPIO_PA1/SER1_TXD[1]/TDMA_TXD[1]/USBTXP	F3	IO	OV <sub>DD</sub>	_	
GPIO_PA2/SER1_TXD[2]/TDMA_TXD[2]	F2	IO	OV <sub>DD</sub>	_	
GPIO_PA3/SER1_TXD[3]/TDMA_TXD[3]	E3	IO	OV <sub>DD</sub>	_	
GPIO_PA4/SER1_RXD[0]/TDMA_RXD[0]/USBRXP	E2	IO	OV <sub>DD</sub>	_	
GPIO_PA5/SER1_RXD[1]/TDMA_RXD[1]/USBRXN	E1	IO	OV <sub>DD</sub>	_	
GPIO_PA6/SER1_RXD[2]/TDMA_RXD[2]/USBRXD	D3	IO	OV <sub>DD</sub>	_	
GPIO_PA7/SER1_RXD[3]/TDMA_RXD[3]	D2	IO	OV <sub>DD</sub>	_	
GPIO_PA8/SER1_CD/TDMA_REQ/USBOE	D1	IO	OV <sub>DD</sub>	_	
GPIO_PA9 TDMA_CLKO	C3	IO	OV <sub>DD</sub>		
GPIO_PA10/SER1_CTS/TDMA_RSYNC	C2	IO	OV <sub>DD</sub>		
GPIO_PA11/TDMA_STROBE	C1	IO	OV <sub>DD</sub>		
GPIO_PA12/SER1_RTS/TDMA_TSYNC	B1	IO	OV <sub>DD</sub>		
GPIO_PA13/CLK9/BRGO9	H4	IO	OV <sub>DD</sub>		
GPIO_PA14/CLK11/BRGO10	G4	IO	OV <sub>DD</sub>		
GPIO_PA15/BRGO7	J4	IO	OV <sub>DD</sub>		
GPIO_PA16/ LA0 (LBIU)	K24	IO	OV <sub>DD</sub>		
GPIO_PA17/ LA1 (LBIU)	K26	IO	OV <sub>DD</sub>		
GPIO_PA18/Enet2_TXD[0]/SER2_TXD[0]/ TDMB_TXD[0]/LA2 (LBIU)	G25	IO	OV <sub>DD</sub>	_	
GPIO_PA19/Enet2_TXD[1]/SER2_TXD[1]/ TDMB_TXD[1]/LA3 (LBIU)	G26	IO	OV <sub>DD</sub>	_	
GPIO_PA20/Enet2_TXD[2]/SER2_TXD[2]/ TDMB_TXD[2]/LA4 (LBIU)	H25	IO	OV <sub>DD</sub>	_	
GPIO_PA21/Enet2_TXD[3]/SER2_TXD[3]/ TDMB_TXD[3]/LA5 (LBIU)	H26	IO	OV <sub>DD</sub>	_	
GPIO_PA22/Enet2_RXD[0]/SER2_RXD[0]/ TDMB_RXD[0]/LA6 (LBIU)	C25	IO	OV <sub>DD</sub>		
GPIO_PA23/Enet2_RXD[1]/SER2_RXD[1]/ TDMB_RXD[1]/LA7 (LBIU)	C26	IO	OV <sub>DD</sub>	_	
GPIO_PA24/Enet2_RXD[2]/SER2_RXD[2]/ TDMB_RXD[2]/LA8 (LBIU)	D25	IO	OV <sub>DD</sub>	—	
GPIO_PA25/Enet2_RXD[3]/SER2_RXD[3]/ TDMB_RXD[3]/LA9 (LBIU)	D26	IO	OV <sub>DD</sub>	—	



Clocking

## 22.6 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. Table 61 shows the multiplication factor encodings for the QUICC Engine PLL.

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF)
00000-00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

Table 61. QUICC Engine PLL Multiplication Factors

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in Table 62.

Table 62. QUICC Engine PLL VCO Divider

RCWL[CEVCOD]	VCO Divider	
00	4	
01	8	
10	2	
11	Reserved	

### NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

 $ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$ 

QUICC Engine VCO Frequency =  $ce_clk \times VCO$  divider  $\times (1 + CEPDF)$ 



(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

 $T_J$  = junction temperature (°C)

 $T_B$  = board temperature at the package perimeter (°C)

 $R_{\theta IB}$  = junction-to-board thermal resistance (°C/W) per JESD51-8

 $P_D$  = power dissipation in package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

## 23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 $T_J$  = junction temperature (°C)

 $T_T$  = thermocouple temperature on top of package (°C)

 $\Psi_{JT}$  = thermal characterization parameter (°C/W)

 $P_D$  = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 23.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$



Thermal

where:

 $R_{\theta IA}$  = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$  = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$  = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$  is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers <sup>™</sup> P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800



#### System Design Information

output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and  $R_P$  is trimmed until the voltage at the pad equals  $OV_{DD}/2$ .  $R_P$  then becomes the resistance of the pull-up devices.  $R_P$  and  $R_N$  are designed to be close to each other in value. Then,  $Z_0 = (R_P + R_N)/2$ .



Figure 45. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is  $V_1 = R_{source} \times I_{source}$ . Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value  $R_{term}$ . The measured voltage is  $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$ . Solving for the output impedance gives  $R_{source} = R_{term} \times (V_1/V_2 - 1)$ . The drive current is then  $I_{source} = V_1/R_{source}$ .

Table 65 summarizes the signal impedance targets. The driver impedance are targeted at minimum  $V_{DD}$ , nominal  $OV_{DD}$ , 105°C.

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R <sub>N</sub>	42 Target	25 Target	20 Target	Z <sub>0</sub>	W
R <sub>P</sub>	42 Target	25 Target	20 Target	Z <sub>0</sub>	W
Differential	NA	NA	NA	Z <sub>DIFF</sub>	W

**Table 65. Impedance Characteristics** 

Note: Nominal supply voltages. See Table 1,  $T_i = 105^{\circ}C$ .

## 24.6 Configuration Pin Multiplexing

The MPC8323E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k $\Omega$  on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.