



Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8323evrafdc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11iTM standard, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8323E DDR1/DDR2 memory controller includes the following features:

- Single 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266-MHz data rate
- Support for two ×16 devices
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O
- Support for 1 chip select only
- FCRAM, ECC, hardware/software calibration, bit deskew, QIN stage, or atomic logic are not supported.

1.5 PCI Controller

The MPC8323E PCI controller includes the following features:

- PCI Specification Revision 2.3 compatible
- Single 32-bit data PCI interface operates up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

1.6 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 35 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.





2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8323E. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V _{DD}	1.0 V ± 50 mV	V	1
PLL supply voltage	AV _{DD}	1.0 V ± 50 mV	V	1
DDR1 and DDR2 DRAM I/O voltage	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
PCI, local bus, DUART, system control and power management, I ² C, SPI, and JTAG I/O voltage	OV _{DD}	3.3 V ± 300 mV	V	1
Junction temperature	T _A /T _J	0 to 105	°C	2

Table 2. Recommended Operating Conditions³

Note:

1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

2. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.

3. All IO pins should be interfaced with peripherals operating at same voltage level.

4. This voltage is the input to the filter discussed in Section 24.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced due to voltage drop across the filter.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8323E



Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}



Electrical Characteristics

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV _{DD} = 3.3 V
PCI signals	25	
DDR1 signal	18	GV _{DD} = 2.5 V
DDR2 signal	18	GV _{DD} = 1.8 V
DUART, system control, I2C, SPI, JTAG	42	OV _{DD} = 3.3 V
GPIO signals	42	OV _{DD} = 3.3 V

Table 3. Output Drive Capability

2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input capacitance for all pins except CLKIN	CI	6	8	pF	_
Input capacitance for CLKIN	C _{ICLKIN}	10		pF	1

Note:

1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and IO supply voltages (GV_{DD}) and $OV_{DD})$ to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}) and OV_{DD} and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD}) and OV_{DD} do not have any ordering requirements with respect to one another.



DDR1 and DDR2 SDRAM

Table 13. DDR2 SDRAM Capacitance for Dn_GV_{DD}(typ) = 1.8 V

Delta input/output capacitance: DQ, DQS	C _{DIO}	-	0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25 °C, V_{OUT} = $Dn_GV_{DD} \div 2$,

V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR1 SDRAM component(s) of the MPC8323E when $Dn_GV_{DD}(typ) = 2.5 V.$

Parameter/Condition Symbol Min Max Unit Notes V I/O supply voltage 2.375 2.625 Dn_GV_{DD} 1 I/O reference voltage MVREF n_{REF} $0.49 \times Dn_GV_{DD}$ $0.51 \times Dn_GV_{DD}$ V 2 I/O termination voltage MVREF n_{REF} - 0.04 MVREFn_{REF} + 0.04 ٧ 3 VTT Input high voltage VIH MVREFn_{REF} + 0.15 $Dn_GV_{DD} + 0.3$ ٧ ٧ Input low voltage VIL -0.3 MVREFn_{REF} – 0.15 Output leakage current -9.9 loz -9.9 μΑ 4 Output high current (V_{OUT} = 1.95 V) -16.2 mΑ I_{OH} Output low current (V_{OUT} = 0.35 V) 16.2 mΑ I_{OL}

Table 14. DDR1 SDRAM DC Electrical Characteristics for Dn_GV_{DD}(typ) = 2.5 V

Notes:

1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.

2. MVREF n_{BEF} is expected to be equal to $0.5 \times Dn_{\text{GV}DD}$, and to track $Dn_{\text{GV}DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREF nREF may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREFn_{REF}. This rail should track variations in the DC level of MVREFn_{REF}.

4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le Dn_GV_{DD}$.

Table 15 provides the DDR1 capacitance $Dn_GV_{DD}(typ) = 2.5$ V.

Table 15. DDR1 SDRAM Capacitance for Dn_GV_{DD}(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ,DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}		0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 2.5 V \pm 0.125 V$, f = 1 MHz, $T_A = 25^{\circ} C$, $V_{OUT} = Dn_GV_{DD} \div 2$, V_{OUT} (peak-to-peak) = 0.2 V.



DDR1 and DDR2 SDRAM

Figure 4 shows the input timing diagram for the DDR controller.



Figure 4. DDR Input Timing Diagram

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

Table 19 provides the output AC timing specifications for the DDR1 and DDR2 SDRAM interfaces.

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with Dn_GV_{DD} of (1.8 or 2.5 V) \pm 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK cycle time, (MCK/MCK crossing)	t _{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	^t DDKHAS	2.5 3.5		ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t _{DDKHAX}	2.5 3.5		ns	3
MCS output setup with respect to MCK 266 MHz 200 MHz	t _{DDKHCS}	2.5 3.5		ns	3
MCS output hold with respect to MCK 266 MHz 200 MHz	^t DDKHCX	2.5 3.5		ns	3
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4



Ethernet and MII Management

(management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 DC Electrical Characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in Table 22.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage 3.3 V	OV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	I _{OH} = -4.0 mA	OV _{DD} = Min	2.40	OV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 4.0 mA	OV _{DD} = Min	GND	0.50	V
Input high voltage	V _{IH}	—	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	—	-0.3	0.90	V
Input current	I _{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

Table 22. MII and RMII DC Electrical Characteristics

8.2 MII and RMII AC Timing Specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t _{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t _{MTX}	—	40	—	ns
TX_CLK duty cycle	t _{MTXH} /t _{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	^t мткнdх	1	5	15	ns
TX_CLK data clock rise time	t _{MTXR}	1.0	_	4.0	ns



Ethernet and MII Management

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Мах	Unit
RX_CLK clock fall time	t _{MRXF}	1.0	_	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 8 provides the AC test load.



Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.



Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.



Parameter	Symbol ¹	Min	Мах	Unit	Notes
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3	_	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	_	ns	7
Local bus clock (LCLKn) to output valid	t _{LBKHOV}	—	3	ns	3
Local bus clock (LCLKn) to output high impedance for LAD/LDP	t _{LBKHOZ}	—	4	ns	8
Local bus clock (LCLKn) duty cycle	t _{LBDC}	47	53	%	_
Local bus clock (LCLKn) jitter specification	t _{LBRJ}	—	400	ps	_
Delay between the input clock (PCI_SYNC_IN) of local bus output clock (LCLK <i>n</i>)	t _{LBCDL}	—	1.7	ns	_

Table 30. Local Bus General Timing Parameters (continued)

Notes:

The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).

2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).

All signals are measured from OV_{DD}/2 of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.

4. Input timings are measured at the pin.

5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.

 t_{LBOTOT2} should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.

7. t_{LBOTOT3} should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.

8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 14 provides the AC test load for the local bus.



Figure 14. Local Bus C Test Load



Figure 21 provides the boundary-scan timing diagram.



Figure 21. Boundary-Scan Timing Diagram





Figure 22. Test Access Port Timing Diagram



11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

Table 33. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V \pm 10%.

Parameter	Symbol	Min	Мах	Unit	Notes
Input high voltage level	V _{IH}	$0.7 imes OV_{DD}$	OV _{DD} + 0.3	V	
Input low voltage level	V _{IL}	-0.3	$0.3\times\text{OV}_{\text{DD}}$	V	_
Low level output voltage	V _{OL}	0	0.4	V	1
Output fall time from $V_{IH}(min)$ to $V_{IL}(max)$ with a bus capacitance from 10 to 400 pF	^t I2KLKV	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	Cl	_	10	pF	_
Input current (0 V \leq V _{IN} \leq OV _{DD})	I _{IN}	—	±5	μA	4

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. C_B = capacitance of one bus line in pF.

3. Refer to the MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual for information on the digital filter used.

4. I/O pins obstructs the SDA and SCL lines if $\ensuremath{\mathsf{OV}_{\mathsf{DD}}}$ is switched off.

11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I^2C interface of the MPC8323E.

Table 34. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter		Min	Мах	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL}	1.3	—	μs
High period of the SCL clock		0.6	—	μs
Setup time for a repeated START condition		0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)		0.6	_	μs
Data setup time		100	—	ns
Data hold time: CBUS compatible masters I ² C bus devices		$\overline{0^2}$	0.9 ³	μs



SPI

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

Table 44. SPI DC Electrical Characteristics

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
SPI outputs—Master mode (internal clock) delay	t _{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t _{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t _{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t _{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t _{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
</sub></sub>

Figure 30 provides the AC test load for the SPI.



Figure 30. SPI AC Test Load



Figure 39 shows the timing with external clock.





Figure 40 shows the timing with internal clock.



Figure 40. AC Timing (Internal Clock) Diagram



21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

Table 55. MPC8323E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Men	nory Controller Interface			
MEMC_MDQ0	AE9	IO	GV _{DD}	—
MEMC_MDQ1	AD10	IO	GV _{DD}	—
MEMC_MDQ2	AF10	IO	GV _{DD}	—
MEMC_MDQ3	AF9	IO	GV _{DD}	—
MEMC_MDQ4	AF7	IO	GV _{DD}	—
MEMC_MDQ5	AE10	IO	GV _{DD}	—
MEMC_MDQ6	AD9	IO	GV _{DD}	—
MEMC_MDQ7	AF8	IO	GV _{DD}	—
MEMC_MDQ8	AE6	IO	GV _{DD}	—
MEMC_MDQ9	AD7	IO	GV _{DD}	—
MEMC_MDQ10	AF6	IO	GV _{DD}	—
MEMC_MDQ11	AC7	IO	GV _{DD}	—
MEMC_MDQ12	AD8	IO	GV _{DD}	—
MEMC_MDQ13	AE7	IO	GV _{DD}	—
MEMC_MDQ14	AD6	IO	GV _{DD}	—
MEMC_MDQ15	AF5	IO	GV _{DD}	—
MEMC_MDQ16	AD18	IO	GV _{DD}	—
MEMC_MDQ17	AE19	IO	GV _{DD}	—
MEMC_MDQ18	AF17	IO	GV _{DD}	—
MEMC_MDQ19	AF19	IO	GV _{DD}	—
MEMC_MDQ20	AF18	IO	GV _{DD}	—
MEMC_MDQ21	AE18	IO	GV _{DD}	—
MEMC_MDQ22	AF20	Ю	GV _{DD}	—
MEMC_MDQ23	AD19	IO	GV _{DD}	—
MEMC_MDQ24	AD21	IO	GV _{DD}	—
MEMC_MDQ25	AF22	IO	GV _{DD}	—
MEMC_MDQ26	AC21	IO	GV _{DD}	—
MEMC_MDQ27	AF21	IO	GV _{DD}	—
MEMC_MDQ28	AE21	IO	GV _{DD}	



Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ3	J2	I	OV _{DD}	—
IRQ4	J1	I	OV _{DD}	—
IRQ5	AE26	I	OV _{DD}	—
IRQ6/CKSTOP_OUT	AE25	IO	OV _{DD}	—
IRQ7/CKSTOP_IN	AF25	I	OV _{DD}	—
CFG_CLKIN_DIV	F1	I	OV _{DD}	—
CFG_LBIU_MUX_EN	M23	I	OV _{DD}	—
	JTAG		•	
тск	W26	I	OV _{DD}	—
TDI	Y26	I	OV _{DD}	4
TDO	AA26	0	OV _{DD}	3
TMS	AB26	I	OV _{DD}	4
TRST	AC26	I	OV _{DD}	4
	TEST		•	
TEST_MODE	N23	I	OV _{DD}	6
	PMC			
QUIESCE	T23	0	OV _{DD}	—
	System Control			
HRESET	AC23	IO	OV _{DD}	1
PORESET	AD23	I	OV _{DD}	—
SRESET	AD24	IO	OV _{DD}	2
	Clocks	·		
CLKIN	R3	I	OV _{DD}	_
CLKIN	P4	0	OV _{DD}	—
PCI_SYNC_OUT	V1	0	OV _{DD}	3
RTC_PIT_CLOCK	U23	I	OV _{DD}	—
PCI_SYNC_IN/PCI_CLK	V2	I	OV _{DD}	—
PCI_CLK0/clkpd_cerisc1_ipg_clkout/DPTC_OSC	ТЗ	0	OV _{DD}	—
PCI_CLK1/clkpd_half_cemb4ucc1_ipg_clkout/ CLOCK_XLB_CLOCK_OUT	U2	0	OV _{DD}	—
PCI_CLK2/clkpd_third_cesog_ipg_clkout/ cecl_ipg_ce_clock	R4	0	OV _{DD}	

Table 55. MPC8323E PBGA Pinout Listing (continued)



Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PA26/Enet2_RX_ER/SER2_CD/TDMB_REQ/ LA10 (LBIU)	E26	IO	OV _{DD}	—
GPIO_PA27/Enet2_TX_ER/TDMB_CLKO/LA11 (LBIU)	F25	IO	OV _{DD}	—
GPIO_PA28/Enet2_RX_DV/SER2_CTS/ TDMB_RSYNC/LA12 (LBIU)	E25	IO	OV _{DD}	—
GPIO_PA29/Enet2_COL/RXD[4]/SER2_RXD[4]/ TDMB_STROBE/LA13 (LBIU)	J25	IO	OV _{DD}	—
GPIO_PA30/Enet2_TX_EN/SER2_RTS/ TDMB_TSYNC/LA14 (LBIU)	F26	IO	OV _{DD}	—
GPIO_PA31/Enet2_CRS/SDET LA15 (LBIU)	J26	IO	OV _{DD}	—
GPIO_PB0/Enet3_TXD[0]/SER3_TXD[0]/ TDMC_TXD[0]	A13	IO	OV _{DD}	—
GPIO_PB1/Enet3_TXD[1]/SER3_TXD[1]/ TDMC_TXD[1]	B13	IO	OV _{DD}	—
GPIO_PB2/Enet3_TXD[2]/SER3_TXD[2]/ TDMC_TXD[2]	A14	IO	OV _{DD}	—
GPIO_PB3/Enet3_TXD[3]/SER3_TXD[3]/ TDMC_TXD[3]	B14	IO	OV _{DD}	—
GPIO_PB4/Enet3_RXD[0]/SER3_RXD[0]/ TDMC_RXD[0]	B8	IO	OV _{DD}	_
GPIO_PB5/Enet3_RXD[1]/SER3_RXD[1]/ TDMC_RXD[1]	A8	IO	OV _{DD}	
GPIO_PB6/Enet3_RXD[2]/SER3_RXD[2]/ TDMC_RXD[2]	A9	IO	OV _{DD}	
GPIO_PB7/Enet3_RXD[3]/SER3_RXD[3]/ TDMC_RXD[3]	В9	IO	OV _{DD}	_
GPIO_PB8/Enet3_RX_ER/SER3_CD/TDMC_REQ	A11	IO	OV _{DD}	—
GPIO_PB9/Enet3_TX_ER/TDMC_CLKO	B11	IO	OV _{DD}	—
GPIO_PB10/Enet3_RX_DV/SER3_CTS/ TDMC_RSYNC	A10	IO	OV _{DD}	
GPIO_PB11/Enet3_COL/RXD[4]/SER3_RXD[4]/ TDMC_STROBE	A15	IO	OV _{DD}	_
GPIO_PB12/Enet3_TX_EN/SER3_RTS/ TDMC_TSYNC	B12	IO	OV _{DD}	_
GPIO_PB13/Enet3_CRS/SDET	B15	IO	OV _{DD}	—
GPIO_PB14/CLK12	D9	IO	OV _{DD}	—
GPIO_PB15 UPC1_TxADDR[4]	D14	IO	OV _{DD}	—
GPIO_PB16 UPC1_RxADDR[4]	B16	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)



Clocking

22 Clocking

Figure 43 shows the internal distribution of clocks within the MPC8323E.



Figure 43. MPC8323E Clock Subsystem

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode, respectively.



Clocking

22.6 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. Table 61 shows the multiplication factor encodings for the QUICC Engine PLL.

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF)
00000-00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

Table 61. QUICC Engine PLL Multiplication Factors

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in Table 62.

Table 62. QUICC Engine PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

 $ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$

QUICC Engine VCO Frequency = $ce_clk \times VCO$ divider $\times (1 + CEPDF)$



22.7 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8323E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 63 shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

Conf No.	SPMF	Core PLL	CEMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0110	0	33.33	133.33	266.66	200
2	0100	0000101	1000	0	25	100	250	200
3	0010	0000100	0011	0	66.67	133.33	266.66	200
4	0100	0000101	0110	0	33.33	133.33	333.33	200
5	0101	0000101	1000	0	25	125	312.5	200
6	0010	0000101	0011	0	66.67	133.33	333.33	200

Table 63. Suggested PLL Configurations

23 Thermal

This section describes the thermal specifications of the MPC8323E.

23.1 **Thermal Characteristics**

Table 64 provides the package thermal characteristics for the 516 27×27 mm PBGA of the MPC8323E.

Table 64. Package Thermal Characteristics for PBGA							
Characteristic	Board type	Symbol	Value	Unit	Notes		
Junction-to-ambient natural convection	Single-layer board (1s)	R _{θJA}	28	°C/W	1, 2		
Junction-to-ambient natural convection	Four-layer board (2s2p)	R _{θJA}	21	°C/W	1, 2, 3		
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	R _{0JMA}	23	°C/W	1, 3		
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	R _{0JMA}	18	°C/W	1, 3		
Junction-to-board	—	$R_{\theta J B}$	13	°C/W	4		
Junction-to-case	_	R _{θJC}	9	°C/W	5		

. . ----



(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

 T_J = junction temperature (°C)

 T_B = board temperature at the package perimeter (°C)

 $R_{\theta IB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

 P_D = power dissipation in package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 T_J = junction temperature (°C)

 T_T = thermocouple temperature on top of package (°C)

 Ψ_{JT} = thermal characterization parameter (°C/W)

 P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$





Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102
Interface material vendors include the following:	
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

23.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

23.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the