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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8323ezqaddc

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8323E.

7.1 DUART DC Electrical Characteristics

Table 20 provides the DC electrical characteristics for the DUART interface of the MPC8323E.

Table 20. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current (0 V ≤ V_{IN} ≤ OV_{DD})[1]	I_{IN}	—	±5	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 21 provides the AC timing parameters for the DUART interface of the MPC8323E.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet and MII Management

This section provides the AC and DC electrical characteristics for Ethernet and MII management.

8.1 Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics

The electrical characteristics specified here apply to all MII (media independent interface) and RMII (reduced media independent interface), except MDIO (management data input/output) and MDC

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock fall time	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

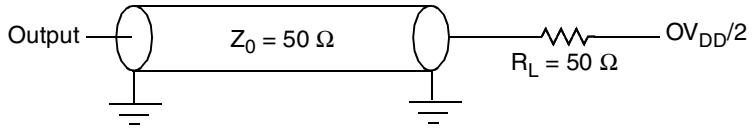


Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

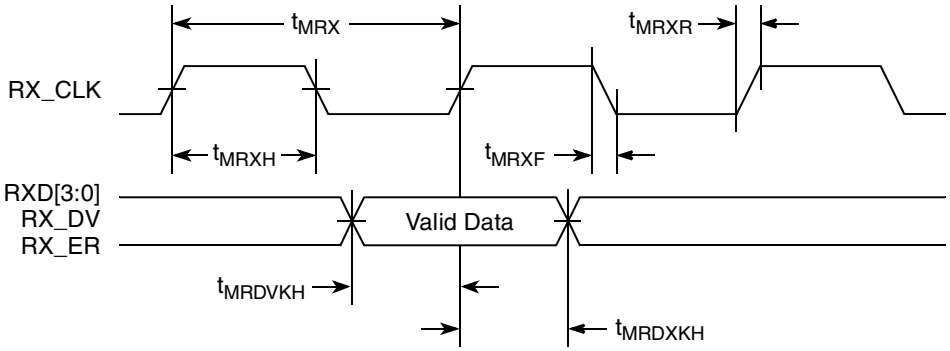


Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMII Transmit AC Timing Specifications

Table 23 provides the RMII transmit AC timing specifications.

Table 25. RMII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the RMII transmit AC timing diagram.

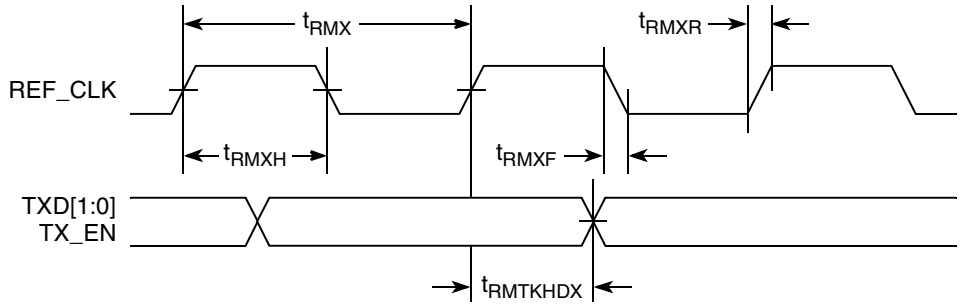


Figure 10. RMII Transmit AC Timing Diagram

8.2.2.2 RMII Receive AC Timing Specifications

Table 24 provides the RMII receive AC timing specifications.

Table 26. RMII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns

Table 26. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load.

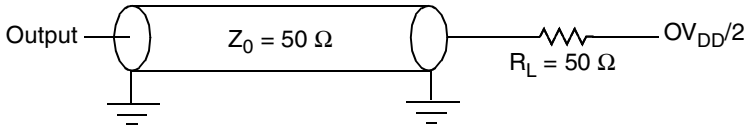


Figure 11. AC Test Load

Figure 12 shows the RMII receive AC timing diagram.

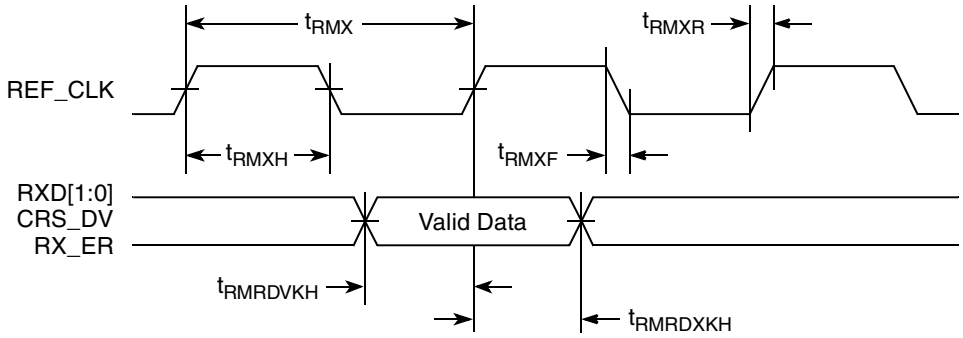


Figure 12. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, “Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics.”

Figure 15 through Figure 17 show the local bus signals.

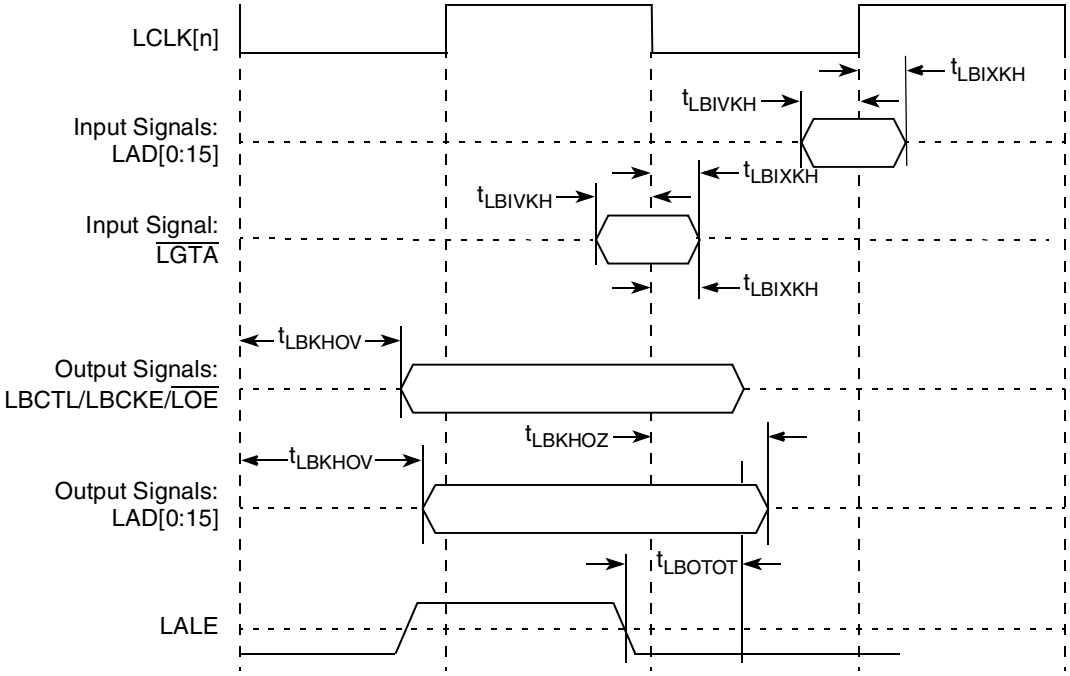


Figure 15. Local Bus Signals, Nonspecial Signals Only

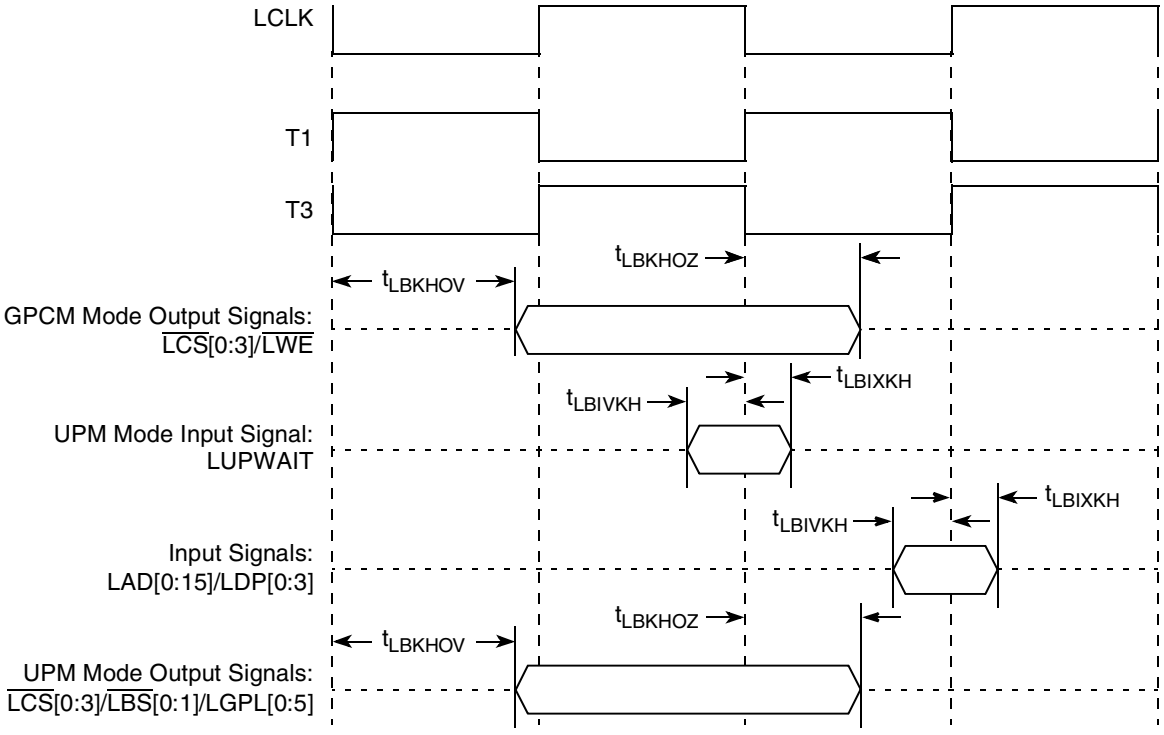


Figure 16. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8323E.

12.1 PCI DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the PCI interface of the MPC8323E.

Table 35. PCI DC Electrical Characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 µA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 µA	—	0.2	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	µA

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.
2. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.3 Local Bus Specifications*.

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8323E. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8323E is configured as a host or agent device. Table 36 shows the PCI AC timing specifications at 66 MHz.

Table 36. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedence	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 29 provides the AC test load for the GPIO.

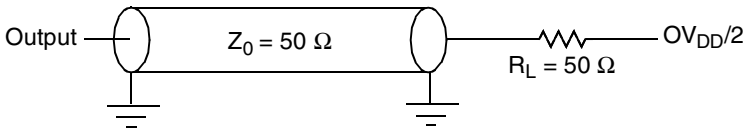


Figure 29. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8323E.

15.1 IPIC DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the external interrupt pins of the MPC8323E.

Table 42. IPIC DC Electrical Characteristics[1,2]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

15.2 IPIC AC Timing Specifications

Table 43 provides the IPIC input and output AC timing specifications.

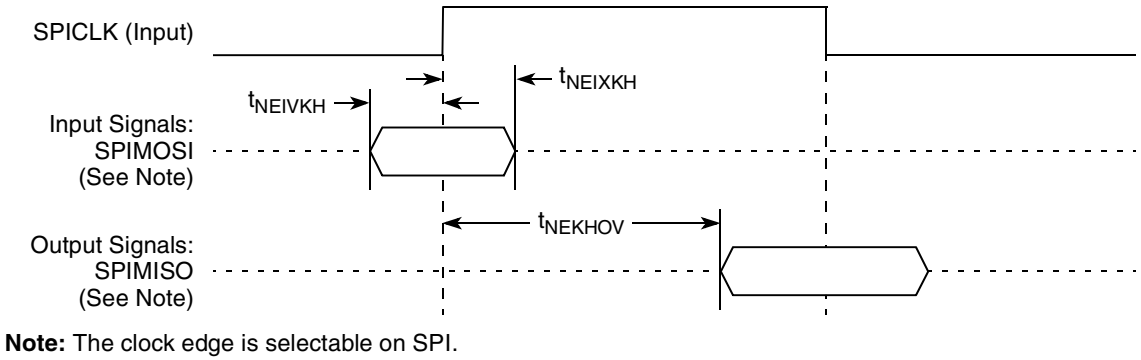
Table 43. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

Figure 31 and Figure 32 represent the AC timing from Table 45. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

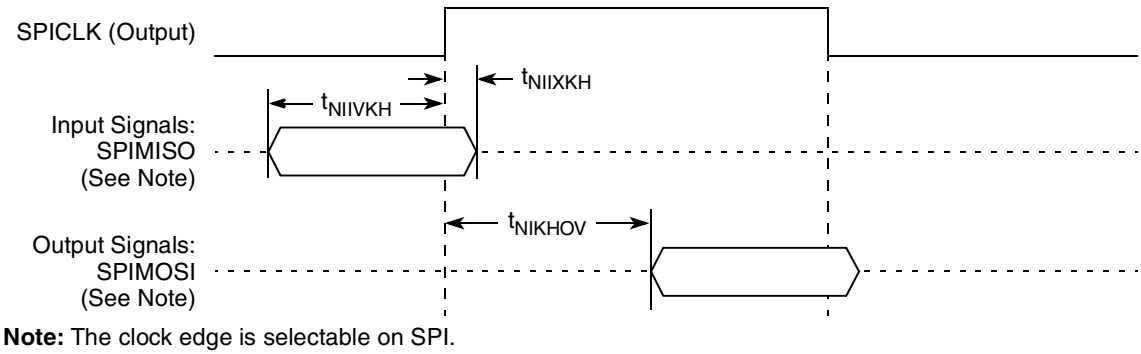
Figure 31 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 31. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 32 shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 32. SPI AC Timing in Master Mode (Internal Clock) Diagram

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8323E.

17.1 TDM/SI DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the MPC8323E TDM/SI.

Table 46. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V

Table 46. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

17.2 TDM/SI AC Timing Specifications

Table 47 provides the TDM/SI input and output AC timing specifications.

Table 47. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	12	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 33 provides the AC test load for the TDM/SI.

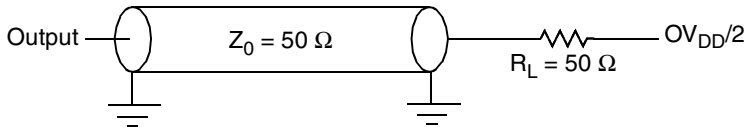
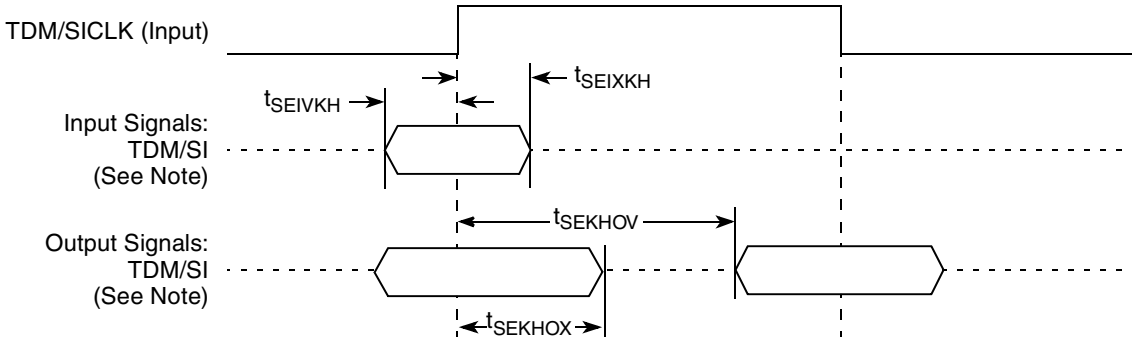


Figure 33. TDM/SI AC Test Load

Figure 34 represents the AC timing from Table 47. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on TDM/SI.

Figure 34. TDM/SI AC Timing (External Clock) Diagram

Figure 35 provides the AC test load for the UTOPIA.

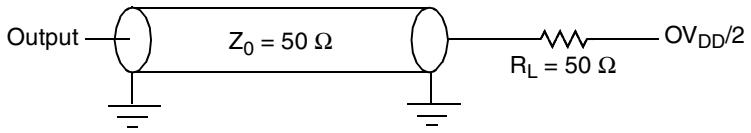


Figure 35. UTOPIA AC Test Load

Figure 36 and Figure 37 represent the AC timing from Table 49. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 36 shows the UTOPIA timing with external clock.

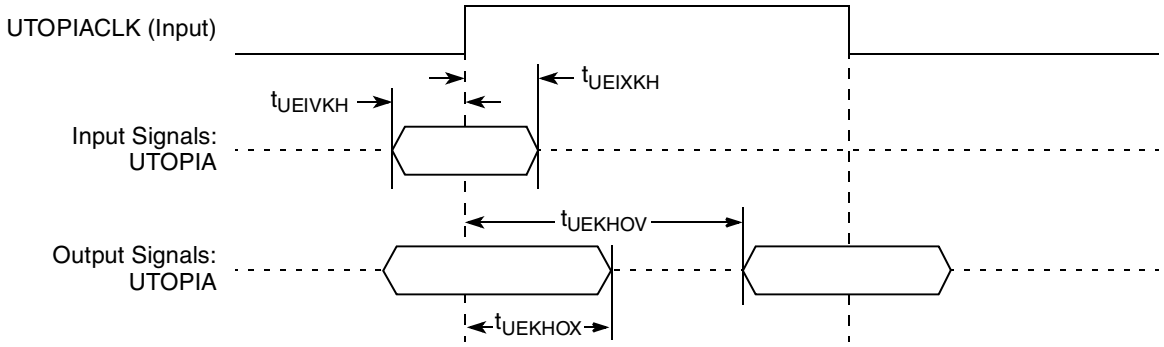


Figure 36. UTOPIA AC Timing (External Clock) Diagram

Figure 37 shows the UTOPIA timing with internal clock.

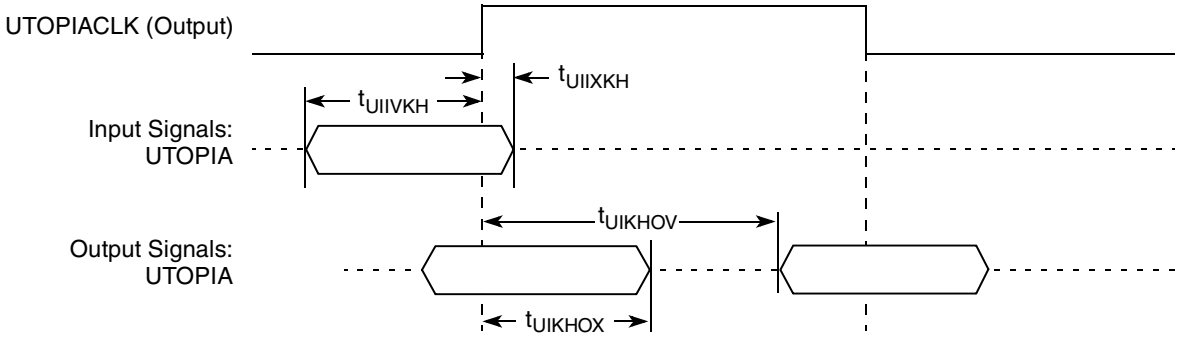


Figure 37. UTOPIA AC Timing (Internal Clock) Diagram

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 52. Synchronous UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	5.5	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	10	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	5.5	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	8	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	4	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	0	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{UAIKHOX}$ symbolizes the outputs internal timing (UAI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 38 provides the AC test load.

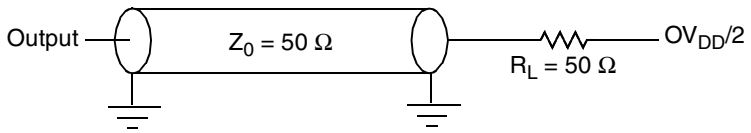


Figure 38. AC Test Load

Figure 39 and Figure 40 represent the AC timing from Table 51. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

20 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8323E.

20.1 USB DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the USB interface.

Table 53. USB DC Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±5	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

20.2 USB AC Electrical Specifications

Table 54 describes the general timing parameters of the USB interface of the MPC8323E.

Table 54. USB General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	20.83	—	ns	Full speed 48 MHz
USB clock cycle time	t_{USCK}	166.67	—	ns	Low speed 6 MHz
Skew between TXP and TXN	t_{USTSPN}	—	5	ns	—
Skew among RXP, RXN, and RXD	$t_{USRSPND}$	—	10	ns	Full speed transitions
Skew among RXP, RXN, and RXD	t_{USRPND}	—	100	ns	Low speed transitions

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(state)(signal)}}$ for receive signals and $t_{\text{(first two letters of functional block)(state)(signal)}}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

Figure 41 provide the AC test load for the USB.

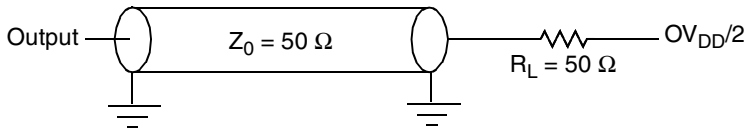


Figure 41. USB AC Test Load

21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

Table 55. MPC8323E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	AE9	IO	GV_{DD}	—
MEMC_MDQ1	AD10	IO	GV_{DD}	—
MEMC_MDQ2	AF10	IO	GV_{DD}	—
MEMC_MDQ3	AF9	IO	GV_{DD}	—
MEMC_MDQ4	AF7	IO	GV_{DD}	—
MEMC_MDQ5	AE10	IO	GV_{DD}	—
MEMC_MDQ6	AD9	IO	GV_{DD}	—
MEMC_MDQ7	AF8	IO	GV_{DD}	—
MEMC_MDQ8	AE6	IO	GV_{DD}	—
MEMC_MDQ9	AD7	IO	GV_{DD}	—
MEMC_MDQ10	AF6	IO	GV_{DD}	—
MEMC_MDQ11	AC7	IO	GV_{DD}	—
MEMC_MDQ12	AD8	IO	GV_{DD}	—
MEMC_MDQ13	AE7	IO	GV_{DD}	—
MEMC_MDQ14	AD6	IO	GV_{DD}	—
MEMC_MDQ15	AF5	IO	GV_{DD}	—
MEMC_MDQ16	AD18	IO	GV_{DD}	—
MEMC_MDQ17	AE19	IO	GV_{DD}	—
MEMC_MDQ18	AF17	IO	GV_{DD}	—
MEMC_MDQ19	AF19	IO	GV_{DD}	—
MEMC_MDQ20	AF18	IO	GV_{DD}	—
MEMC_MDQ21	AE18	IO	GV_{DD}	—
MEMC_MDQ22	AF20	IO	GV_{DD}	—
MEMC_MDQ23	AD19	IO	GV_{DD}	—
MEMC_MDQ24	AD21	IO	GV_{DD}	—
MEMC_MDQ25	AF22	IO	GV_{DD}	—
MEMC_MDQ26	AC21	IO	GV_{DD}	—
MEMC_MDQ27	AF21	IO	GV_{DD}	—
MEMC_MDQ28	AE21	IO	GV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LCS1}}$	AB25	O	OV_{DD}	4
$\overline{\text{LCS2}}$	AA23	O	OV_{DD}	4
$\overline{\text{LCS3}}$	AA24	O	OV_{DD}	4
$\overline{\text{LWE0}}$	Y23	O	OV_{DD}	4
$\overline{\text{LWE1}}$	W25	O	OV_{DD}	4
LBCTL	V25	O	OV_{DD}	4
LALE	V24	O	OV_{DD}	7
CFG_RESET_SOURCE[0]/LSDA10/LGPL0	L23	IO	OV_{DD}	—
CFG_RESET_SOURCE[1]/$\overline{\text{LSDWE}}$/LGPL1	K23	IO	OV_{DD}	—
$\overline{\text{LSDRAS}}$/LGPL2/$\overline{\text{LOE}}$	J23	O	OV_{DD}	4
CFG_RESET_SOURCE[2]/$\overline{\text{LSDCAS}}$/LGPL3	H23	IO	OV_{DD}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	G23	IO	OV_{DD}	4, 8
LGPL5	AC22	O	OV_{DD}	4
LCLK0	Y24	O	OV_{DD}	7
LCLK1	Y25	O	OV_{DD}	7
DUART				
UART_SOUT1/MSRCID0 (DDR ID)/LSRCID0	G1	IO	OV_{DD}	—
UART_SIN1/MSRCID1 (DDR ID)/LSRCID1	G2	IO	OV_{DD}	—
$\overline{\text{UART\_CTS1}}$/MSRCID2 (DDR ID)/LSRCID2	H3	IO	OV_{DD}	—
$\overline{\text{UART\_RTS1}}$/MSRCID3 (DDR ID)/LSRCID3	K3	IO	OV_{DD}	—
UART_SOUT2/MSRCID4 (DDR ID)/LSRCID4	H2	IO	OV_{DD}	—
UART_SIN2/MDVAL (DDR ID)/LDVAL	H1	IO	OV_{DD}	—
$\overline{\text{UART\_CTS2}}$	J3	IO	OV_{DD}	—
$\overline{\text{UART\_RTS2}}$	K4	IO	OV_{DD}	—
I^2C interface				
IIC_SDA/$\overline{\text{CKSTOP\_OUT}}$	AE24	IO	OV_{DD}	2
IIC_SCL/$\overline{\text{CKSTOP\_IN}}$	AF24	IO	OV_{DD}	2
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	AD25	O	OV_{DD}	—
$\overline{\text{IRQ0}}$/$\overline{\text{MCP\_IN}}$	AD26	I	OV_{DD}	—
$\overline{\text{IRQ1}}$	K1	IO	OV_{DD}	—
$\overline{\text{IRQ2}}$	K2	I	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ3}}$	J2	I	OV_{DD}	—
$\overline{\text{IRQ4}}$	J1	I	OV_{DD}	—
$\overline{\text{IRQ5}}$	AE26	I	OV_{DD}	—
$\overline{\text{IRQ6}}$/$\overline{\text{CKSTOP\_OUT}}$	AE25	IO	OV_{DD}	—
$\overline{\text{IRQ7}}$/$\overline{\text{CKSTOP\_IN}}$	AF25	I	OV_{DD}	—
$\overline{\text{CFG\_CLKIN\_DIV}}$	F1	I	OV_{DD}	—
CFG_LBIU_MUX_EN	M23	I	OV_{DD}	—
JTAG				
TCK	W26	I	OV_{DD}	—
TDI	Y26	I	OV_{DD}	4
TDO	AA26	O	OV_{DD}	3
TMS	AB26	I	OV_{DD}	4
$\overline{\text{TRST}}$	AC26	I	OV_{DD}	4
TEST				
TEST_MODE	N23	I	OV_{DD}	6
PMC				
$\overline{\text{QUIESCE}}$	T23	O	OV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AC23	IO	OV_{DD}	1
$\overline{\text{PORESET}}$	AD23	I	OV_{DD}	—
$\overline{\text{SRESET}}$	AD24	IO	OV_{DD}	2
Clocks				
CLKIN	R3	I	OV_{DD}	—
$\overline{\text{CLKIN}}$	P4	O	OV_{DD}	—
PCI_SYNC_OUT	V1	O	OV_{DD}	3
RTC_PIT_CLOCK	U23	I	OV_{DD}	—
PCI_SYNC_IN/PCI_CLK	V2	I	OV_{DD}	—
PCI_CLK0/clkpd_cerisc1_ipg_clkout/DPTC_OSC	T3	O	OV_{DD}	—
PCI_CLK1/clkpd_half_cemb4ucc1_ipg_clkout/ CLOCK_XLB_CLOCK_OUT	U2	O	OV_{DD}	—
PCI_CLK2/clkpd_third_cesog_ipg_clkout/ cecl_ipg_ce_clock	R4	O	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PA26/Enet2_RX_ER/SER2_CD/TDMB_REQ/ LA10 (LBIU)	E26	IO	OV_{DD}	—
GPIO_PA27/Enet2_TX_ER/TDMB_CLKO/LA11 (LBIU)	F25	IO	OV_{DD}	—
GPIO_PA28/Enet2_RX_DV/SER2_CTS/ TDMB_RSYNC/LA12 (LBIU)	E25	IO	OV_{DD}	—
GPIO_PA29/Enet2_COL/RXD[4]/SER2_RXD[4]/ TDMB_STROBE/LA13 (LBIU)	J25	IO	OV_{DD}	—
GPIO_PA30/Enet2_TX_EN/SER2_RTS/ TDMB_TSYNC/LA14 (LBIU)	F26	IO	OV_{DD}	—
GPIO_PA31/Enet2_CRS/SDET LA15 (LBIU)	J26	IO	OV_{DD}	—
GPIO_PB0/Enet3_TXD[0]/SER3_TXD[0]/ TDMC_TXD[0]	A13	IO	OV_{DD}	—
GPIO_PB1/Enet3_TXD[1]/SER3_TXD[1]/ TDMC_TXD[1]	B13	IO	OV_{DD}	—
GPIO_PB2/Enet3_TXD[2]/SER3_TXD[2]/ TDMC_TXD[2]	A14	IO	OV_{DD}	—
GPIO_PB3/Enet3_TXD[3]/SER3_TXD[3]/ TDMC_TXD[3]	B14	IO	OV_{DD}	—
GPIO_PB4/Enet3_RXD[0]/SER3_RXD[0]/ TDMC_RXD[0]	B8	IO	OV_{DD}	—
GPIO_PB5/Enet3_RXD[1]/SER3_RXD[1]/ TDMC_RXD[1]	A8	IO	OV_{DD}	—
GPIO_PB6/Enet3_RXD[2]/SER3_RXD[2]/ TDMC_RXD[2]	A9	IO	OV_{DD}	—
GPIO_PB7/Enet3_RXD[3]/SER3_RXD[3]/ TDMC_RXD[3]	B9	IO	OV_{DD}	—
GPIO_PB8/Enet3_RX_ER/SER3_CD/TDMC_REQ	A11	IO	OV_{DD}	—
GPIO_PB9/Enet3_TX_ER/TDMC_CLKO	B11	IO	OV_{DD}	—
GPIO_PB10/Enet3_RX_DV/SER3_CTS/ TDMC_RSYNC	A10	IO	OV_{DD}	—
GPIO_PB11/Enet3_COL/RXD[4]/SER3_RXD[4]/ TDMC_STROBE	A15	IO	OV_{DD}	—
GPIO_PB12/Enet3_TX_EN/SER3_RTS/ TDMC_TSYNC	B12	IO	OV_{DD}	—
GPIO_PB13/Enet3_CRS/SDET	B15	IO	OV_{DD}	—
GPIO_PB14/CLK12	D9	IO	OV_{DD}	—
GPIO_PB15 UPC1_TxADDR[4]	D14	IO	OV_{DD}	—
GPIO_PB16 UPC1_RxADDR[4]	B16	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PB17/BRGO1/CE_EXT_REQ1	D10	IO	OV_{DD}	—
GPIO_PB18/Enet4_TXD[0]/SER4_TXD[0]/ TDMD_TXD[0]	C10	IO	OV_{DD}	—
GPIO_PB19/Enet4_TXD[1]/SER4_TXD[1]/ TDMD_TXD[1]	C9	IO	OV_{DD}	—
GPIO_PB20/Enet4_TXD[2]/SER4_TXD[2]/ TDMD_TXD[2]	D8	IO	OV_{DD}	—
GPIO_PB21/Enet4_TXD[3]/SER4_TXD[3]/ TDMD_TXD[3]	C8	IO	OV_{DD}	—
GPIO_PB22/Enet4_RXD[0]/SER4_RXD[0]/ TDMD_RXD[0]	C15	IO	OV_{DD}	—
GPIO_PB23/Enet4_RXD[1]/SER4_RXD[1]/ TDMD_RXD[1]	C14	IO	OV_{DD}	—
GPIO_PB24/Enet4_RXD[2]/SER4_RXD[2]/ TDMD_RXD[2]	D13	IO	OV_{DD}	—
GPIO_PB25/Enet4_RXD[3]/SER4_RXD[3]/ TDMD_RXD[3]	C13	IO	OV_{DD}	—
GPIO_PB26/Enet4_RX_ER/SER4_CD/TDMD_REQ	C12	IO	OV_{DD}	—
GPIO_PB27/Enet4_TX_ER/TDMD_CLKO	D11	IO	OV_{DD}	—
GPIO_PB28/Enet4_RX_DV/SER4_CTS/ TDMD_RSYNC	D12	IO	OV_{DD}	—
GPIO_PB29/Enet4_COL/RXD[4]/SER4_RXD[4]/ TDMD_STROBE	D7	IO	OV_{DD}	—
GPIO_PB30/Enet4_TX_EN/SER4_RTS/ TDMD_TSYNC	C11	IO	OV_{DD}	—
GPIO_PB31/Enet4_CRS/SDET	C7	IO	OV_{DD}	—
GPIO_PC0/UPC1_TxDATA[0]/SER5_TXD[0]	A18	IO	OV_{DD}	—
GPIO_PC1/UPC1_TxDATA[1]/SER5_TXD[1]	A19	IO	OV_{DD}	—
GPIO_PC2/UPC1_TxDATA[2]/SER5_TXD[2]	B18	IO	OV_{DD}	—
GPIO_PC3/UPC1_TxDATA[3]/SER5_TXD[3]	B19	IO	OV_{DD}	—
GPIO_PC4/UPC1_TxDATA[4]	A24	IO	OV_{DD}	—
GPIO_PC5/UPC1_TxDATA[5]	B24	IO	OV_{DD}	—
GPIO_PC6/UPC1_TxDATA[6]	A23	IO	OV_{DD}	—
GPIO_PC7/UPC1_TxDATA[7]	B26	IO	OV_{DD}	—
GPIO_PC8/UPC1_RxDATA[0]/SER5_RXD[0]	A21	IO	OV_{DD}	—
GPIO_PC9/UPC1_RxDATA[1]/SER5_RXD[1]	B20	IO	OV_{DD}	—

22.5 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 60 shows the encodings for RCWL[COREPLL]. COREPLL values not listed in Table 60 should be considered reserved.

Table 60. e300 Core PLL Configuration

RCWL[COREPLL]			***core_clk* : *csb_clk* Ratio**	**VCO Divider**
0-1	**2-5**	**6**		
nn	**0000**	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	**0001**	0	1:1	÷2
01	**0001**	0	1:1	÷4
10	**0001**	0	1:1	÷8
11	**0001**	0	1:1	÷8
00	**0001**	1	1.5:1	÷2
01	**0001**	1	1.5:1	÷4
10	**0001**	1	1.5:1	÷8
11	**0001**	1	1.5:1	÷8
00	**0010**	0	2:1	÷2
01	**0010**	0	2:1	÷4
10	**0010**	0	2:1	÷8
11	**0010**	0	2:1	÷8
00	**0010**	1	2.5:1	÷2
01	**0010**	1	2.5:1	÷4
10	**0010**	1	2.5:1	÷8
11	**0010**	1	2.5:1	÷8
00	**0011**	0	3:1	÷2
01	**0011**	0	3:1	÷4
10	**0011**	0	3:1	÷8
11	**0011**	0	3:1	÷8

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 500–800 MHz.

25.2 Part Marking

Parts are marked as in the example shown in Figure 46.

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 46. Freescale Part Marking for PBGA Devices

26 Document Revision History

Table 67 provides a revision history for this hardware specification.

Table 67. Document Revision History

Rev. No.	Date	Substantive Change(s)
4	09/2010	• Replaced all instances of “LCCR” with “LCRR” throughout. • Added footnotes 3 and 4 in Table 2, “Recommended Operating Conditions[3].” • Modified Section 8.1.1, “DC Electrical Characteristics.” • Modified Table 23, “MII Transmit AC Timing Specifications.” • Modified Table 24, “MII Receive AC Timing Specifications.” • Added footnote 7 and 8, and modified some signal names in Table 55, ”MPC8323E PBGA Pinout Listing.”
3	12/2009	• Removed references for note 4 from Table 1. • Added Figure 2 in Section 2.1.2, “Power Supply Voltage Specification. • Added symbol T_A in Table 2. • Added footnote 2 in Table 2. • Added a note in Section 4, “Clock Input Timing for rise/fall time of QE input pins. • Modified CLKIN, PCI_CLK rise/fall time parameters in Table 8. Modified min value of t_{MCK} in Table 19. • Modified Figure 43. • Modified formula for ce_clk calculation in Section 22.3, “System Clock Domains. • Added a note in Section 22.4, “System PLL Configuration. • Removed the signal ECID_TMODE_IN from Table 55. • Removed all references of RST signals from Table 55.

Table 67. Document Revision History

Rev. No.	Date	Substantive Change(s)
2	4/2008	• Removed Figures 2 and 3 overshoot and undershoot voltage specs from Section 2.1.2, "Power Supply Voltage Specification," and footnotes 4 and 5 from Table 1. • Corrected QUIESCE signal to be an output signal in Table 55. • Added column for GVDD (1.8 V) - DDR2 - to Table 6 with 0.212-W typical power dissipation. • Added Figure 4 DDR input timing diagram. • Removed CE_TRB* and CE_PIO* signals from Table 55. • Added three local bus AC specifications to Table 30 (duty cycle, jitter, delay between input clock and local bus clock). • Added row in Table 2 stating junction temperature range of 0 to 105•C. • Modified Section 2.2, "Power Sequencing," to include $\overline{\text{PORESET}}$ requirement.
1	6/2007	Correction to descriptive text in Section 2.2.
0	6/2007	Initial release.