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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	•
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8323vrafdc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11iTM standard, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8323E DDR1/DDR2 memory controller includes the following features:

- Single 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266-MHz data rate
- Support for two ×16 devices
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O
- Support for 1 chip select only
- FCRAM, ECC, hardware/software calibration, bit deskew, QIN stage, or atomic logic are not supported.

1.5 PCI Controller

The MPC8323E PCI controller includes the following features:

- PCI Specification Revision 2.3 compatible
- Single 32-bit data PCI interface operates up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

1.6 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 35 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.



Electrical Characteristics

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8323E. The MPC8323E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

					-
Chara	acteristic	Symbol	Max Value	Unit	Notes
Core supply voltage		V _{DD}	-0.3 to 1.26	V	—
PLL supply voltage		AV_{DDn}	–0.3 to 1.26	V	_
DDR1 and DDR2 DRAM I/O voltage		GV _{DD}	–0.3 to 2.75 –0.3 to 1.98	V	_
PCI, local bus, DUART, system control and power management, I ² C, SPI, MII, RMII, MII management, and JTAG I/O voltage		OV _{DD}	-0.3 to 3.6	V	—
Input voltage	DDR1/DDR2 DRAM signals	MV _{IN}	–0.3 to (GV _{DD} + 0.3)	V	2
	DDR1/DDR2 DRAM reference	MV _{REF}	–0.3 to (GV _{DD} + 0.3)	V	2
	Local bus, DUART, CLKIN, system control and power management, I ² C, SPI, and JTAG signals	OV _{IN}	–0.3 to (OV _{DD} + 0.3)	V	3
	PCI	OVIN	–0.3 to (OV _{DD} + 0.3)	V	5
Storage temperature range		T _{STG}	–55 to 150	°C	_

Table 1. Absolute Maximum Ratings¹

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

 Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.



Clock Input Timing

Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 32 bits	_		0.12	W	_
PCI I/O load = 30 pF	66 MHz, 32 bits	—		0.057	W	—
QUICC Engine block and	UTOPIA 8-bit 31 PHYs	—	_	0.041	W	Multiply by
other I/Os	TDM serial	—	_	0.001	W	interfaces used.
	TDM nibble	—	_	0.004	W	
	HDLC/TRAN serial	—	_	0.003	W	
	HDLC/TRAN nibble	—	_	0.025	W	
	DUART	—	_	0.017	W	
	Mils	—	_	0.009	W	
	RMII	—	_	0.009	W	
	Ethernet management	—	_	0.002	W	
	USB	—	_	0.001	W	
	SPI	—	—	0.001	W	
	Timer output	—	—	0.002	W	

Table 6. Estimated Typical I/O Power Dissipation (continued)

NOTE

 $AV_{DD}n$ (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

Parameter	Condition	Symbol	Min	Мах	Unit
Input high voltage	—	V _{IH}	2.7	OV _{DD} + 0.3	V
Input low voltage	_	V _{IL}	-0.3	0.4	V

Table 7. CLKIN DC Electrical Characteristics



DDR1 and DDR2 SDRAM

Table 13. DDR2 SDRAM Capacitance for Dn_GV_{DD}(typ) = 1.8 V

Delta input/output capacitance: DQ, DQS	C _{DIO}	-	0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25 °C, V_{OUT} = $Dn_GV_{DD} \div 2$,

V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR1 SDRAM component(s) of the MPC8323E when $Dn_GV_{DD}(typ) = 2.5 V.$

Parameter/Condition Symbol Min Max Unit Notes V I/O supply voltage 2.375 2.625 Dn_GV_{DD} 1 I/O reference voltage MVREF n_{REF} $0.49 \times Dn_GV_{DD}$ $0.51 \times Dn_GV_{DD}$ V 2 I/O termination voltage MVREF n_{REF} - 0.04 MVREFn_{REF} + 0.04 ٧ 3 VTT Input high voltage VIH MVREFn_{REF} + 0.15 $Dn_GV_{DD} + 0.3$ ٧ ٧ Input low voltage VIL -0.3 MVREFn_{REF} – 0.15 Output leakage current -9.9 loz -9.9 μΑ 4 Output high current (V_{OUT} = 1.95 V) -16.2 mΑ I_{OH} Output low current (V_{OUT} = 0.35 V) 16.2 mΑ I_{OL}

Table 14. DDR1 SDRAM DC Electrical Characteristics for Dn_GV_{DD}(typ) = 2.5 V

Notes:

1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.

2. MVREF n_{BEF} is expected to be equal to $0.5 \times Dn_{\text{GV}DD}$, and to track $Dn_{\text{GV}DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREF nREF may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREFn_{REF}. This rail should track variations in the DC level of MVREFn_{REF}.

4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le Dn_GV_{DD}$.

Table 15 provides the DDR1 capacitance $Dn_GV_{DD}(typ) = 2.5$ V.

Table 15. DDR1 SDRAM Capacitance for Dn_GV_{DD}(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ,DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}		0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$, f = 1 MHz, $T_A = 25^{\circ} \text{ C}$, $V_{OUT} = Dn_GV_{DD} \div 2$, V_{OUT} (peak-to-peak) = 0.2 V.



6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR1 and DDR2 SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM ($Dn_GV_{DD}(typ) = 1.8 \text{ V}$).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with Dn_GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MVREF <i>n</i> _{REF} – 0.25	V	—
AC input high voltage	V _{IH}	MVREFn _{REF} + 0.25	_	V	

Table 17 provides the input AC timing specifications for the DDR1 SDRAM ($Dn_GV_{DD}(typ) = 2.5 V$).

Table 17. DDR1 SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with Dn_GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V _{IL}	—	MVREF <i>n</i> _{REF} – 0.31	V	
AC input high voltage	V _{IH}	MVREF <i>n</i> _{REF} + 0.31	_	V	

Table 18 provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 18. DDR1 and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with Dn_GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller skew for MDQS—MDQ/MDM 266 MHz 200 MHz	^t CISKEW	-750 -1250	750 1250	ps	1, 2

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.

 The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = ±(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.



Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with Dn_GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQ/MDM output setup with respect to MDQS	^t DDKHDS, t _{DDKLDS}			ns	5
266 MHz		0.9	—		
200 MHz		1.0	—		
MDQ/MDM output hold with respect to MDQS	t _{DDKHDX,} t _{DDKLDX}			ps	5
266 MHz		1100	—		
200 MHz		1200	—		
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{\text{MCK}}-0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t _{DDKHME}	-0.6	0.6	ns	6

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
</sub>

2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ± 0.1 V.

3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual for a description and understanding of the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.



Table 23. MII Transmit AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
TX_CLK data clock fall time	t _{MTXF}	1.0	_	4.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

Figure 7 shows the MII transmit AC timing diagram.



Figure 7. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Мах	Unit
RX_CLK clock period 10 Mbps	t _{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t _{MRX}	—	40	—	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time	t _{MRXR}	1.0	—	4.0	ns



Table 32. JTAG AC Timing Specifications (Independent of CLKIN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{JTKLDZ} t _{JTKLOZ}	2 2	19 9	ns	5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

- 2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K)} going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4. Non-JTAG signal input timing with respect to t_{TCLK}.

- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design and characterization.

Figure 18 provides the AC test load for TDO and the boundary-scan outputs of the MPC8323E.



Figure 18. AC Test Load for the JTAG Interface

Figure 19 provides the JTAG clock input timing diagram.



Figure 19. JTAG Clock Input Timing Diagram

Figure 20 provides the TRST timing diagram.





Figure 28 provides the AC test load for the timers.



14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8323E.

14.1 GPIO DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E GPIO.

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V	1
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V	1
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V	1
Input low voltage	V _{IL}	—	-0.3	0.8	V	—
Input current	I _{IN}	$0 \ V \leq V_{IN} \leq OV_{DD}$	_	±5	μA	—

Table 40. GPIO DC Electrical Characteristics

Note:

1. This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

Table 41 provides the GPIO input and output AC timing specifications.

Table 41. GPIO Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.



Figure 29 provides the AC test load for the GPIO.



15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8323E.

15.1 IPIC DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the external interrupt pins of the MPC8323E.

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	—	±5	μA
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

Table 42. IPIC DC Electrical Characteristics^{1,2}

Notes:

1. This table applies for pins IRQ[0:7], IRQ_OUT, MCP_OUT, and CE ports Interrupts.

2. IRQ_OUT and MCP_OUT are open drain pins, thus V_{OH} is not relevant for those pins.

15.2 IPIC AC Timing Specifications

Table 43 provides the IPIC input and output AC timing specifications.

Table 43. IPIC Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any
external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working
in edge triggered mode.



SPI

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 \ V \le V_{IN} \le OV_{DD}$	—	±5	μA

Table 44. SPI DC Electrical Characteristics

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
SPI outputs—Master mode (internal clock) delay	t _{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t _{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t _{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t _{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t _{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
</sub></sub>

Figure 30 provides the AC test load for the SPI.



Figure 30. SPI AC Test Load



TDM/SI

Table 46. TDM	SI DC Electrica	Characteristics	(continued)
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Characteristic	Symbol	Condition	Min	Мах	Unit
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 \ V \leq V_{IN} \leq OV_{DD}$	—	±5	μA

17.2 TDM/SI AC Timing Specifications

Table 47 provides the TDM/SI input and output AC timing specifications.

Table 47. TDM/SI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
TDM/SI outputs—External clock delay	t _{SEKHOV}	2	12	ns
TDM/SI outputs—External clock High Impedance	t _{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t _{SEIVKH}	5		ns
TDM/SI inputs—External clock input hold time	t _{SEIXKH}	2	_	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time t_{TDM/SI} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).}

Figure 33 provides the AC test load for the TDM/SI.



Figure 33. TDM/SI AC Test Load

Figure 34 represents the AC timing from Table 47. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Figure 34. TDM/SI AC Timing (External Clock) Diagram



Figure 39 shows the timing with external clock.





Figure 40 shows the timing with internal clock.



Figure 40. AC Timing (Internal Clock) Diagram



21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8323E is available in a thermally enhanced Plastic Ball Grid Array (PBGA); see Section 21.1, "Package Parameters for the MPC8323E PBGA," and Section 21.2, "Mechanical Dimensions of the MPC8323E PBGA," for information on the PBGA.

21.1 Package Parameters for the MPC8323E PBGA

The package parameters are as provided in the following list. The package type is $27 \text{ mm} \times 27 \text{ mm}$, 516 PBGA.

Package outline	$27 \text{ mm} \times 27 \text{ mm}$
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.6 mm

21.2 Mechanical Dimensions of the MPC8323E PBGA

Figure 42 shows the mechanical dimensions and bottom surface nomenclature of the MPC8323E, 516-PBGA package.



Package and Pin Listings



Notes:

1.All dimensions are in millimeters.

2.Dimensions and tolerances per ASME Y14.5M-1994.

3.Maximum solder ball diameter measured parallel to datum A.

4.Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 42. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8323E PBGA



Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	0	GV _{DD}	3
MEMC_MCK	AF14	0	GV _{DD}	—
MEMC_MCK	AE14	0	GV _{DD}	—
MEMC_MODT	AF11	0	GV _{DD}	—
Local B	us Controller Interface			
LAD0	N25	IO	OV _{DD}	7
LAD1	P26	IO	OV _{DD}	7
LAD2	P25	IO	OV _{DD}	7
LAD3	R26	IO	OV _{DD}	7
LAD4	R25	IO	OV _{DD}	7
LAD5	T26	IO	OV _{DD}	7
LAD6	T25	IO	OV _{DD}	7
LAD7	U25	IO	OV _{DD}	7
LAD8	M24	IO	OV _{DD}	7
LAD9	N24	IO	OV _{DD}	7
LAD10	P24	IO	OV _{DD}	7
LAD11	R24	IO	OV _{DD}	7
LAD12	T24	IO	OV _{DD}	7
LAD13	U24	IO	OV _{DD}	7
LAD14	U26	IO	OV _{DD}	7
LAD15	V26	IO	OV _{DD}	7
LA16	K25	0	OV _{DD}	7
LA17	L25	0	OV _{DD}	7
LA18	L26	0	OV _{DD}	7
LA19	L24	0	OV _{DD}	7
LA20	M26	0	OV _{DD}	7
LA21	M25	0	OV _{DD}	7
LA22	N26	0	OV _{DD}	7
LA23	AC24	0	OV _{DD}	7
LA24	AC25	0	OV _{DD}	7
LA25	AB23	0	OV _{DD}	7
LCS0	AB24	0	OV _{DD}	4

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PA26/Enet2_RX_ER/SER2_CD/TDMB_REQ/ LA10 (LBIU)	E26	IO	OV _{DD}	_
GPIO_PA27/Enet2_TX_ER/TDMB_CLKO/LA11 (LBIU)	F25	IO	OV _{DD}	—
GPIO_PA28/Enet2_RX_DV/SER2_CTS/ TDMB_RSYNC/LA12 (LBIU)	E25	IO	OV _{DD}	
GPIO_PA29/Enet2_COL/RXD[4]/SER2_RXD[4]/ TDMB_STROBE/LA13 (LBIU)	J25	IO	OV _{DD}	
GPIO_PA30/Enet2_TX_EN/SER2_RTS/ TDMB_TSYNC/LA14 (LBIU)	F26	IO	OV _{DD}	
GPIO_PA31/Enet2_CRS/SDET LA15 (LBIU)	J26	IO	OV _{DD}	—
GPIO_PB0/Enet3_TXD[0]/SER3_TXD[0]/ TDMC_TXD[0]	A13	IO	OV _{DD}	
GPIO_PB1/Enet3_TXD[1]/SER3_TXD[1]/ TDMC_TXD[1]	B13	IO	OV _{DD}	
GPIO_PB2/Enet3_TXD[2]/SER3_TXD[2]/ TDMC_TXD[2]	A14	IO	OV _{DD}	
GPIO_PB3/Enet3_TXD[3]/SER3_TXD[3]/ TDMC_TXD[3]	B14	IO	OV _{DD}	
GPIO_PB4/Enet3_RXD[0]/SER3_RXD[0]/ TDMC_RXD[0]	B8	IO	OV _{DD}	
GPIO_PB5/Enet3_RXD[1]/SER3_RXD[1]/ TDMC_RXD[1]	A8	IO	OV _{DD}	
GPIO_PB6/Enet3_RXD[2]/SER3_RXD[2]/ TDMC_RXD[2]	A9	IO	OV _{DD}	
GPIO_PB7/Enet3_RXD[3]/SER3_RXD[3]/ TDMC_RXD[3]	В9	IO	OV _{DD}	
GPIO_PB8/Enet3_RX_ER/SER3_CD/TDMC_REQ	A11	IO	OV _{DD}	—
GPIO_PB9/Enet3_TX_ER/TDMC_CLKO	B11	IO	OV _{DD}	—
GPIO_PB10/Enet3_RX_DV/SER3_CTS/ TDMC_RSYNC	A10	IO	OV _{DD}	
GPIO_PB11/Enet3_COL/RXD[4]/SER3_RXD[4]/ TDMC_STROBE	A15	IO	OV _{DD}	
GPIO_PB12/Enet3_TX_EN/SER3_RTS/ TDMC_TSYNC	B12	IO	OV _{DD}	
GPIO_PB13/Enet3_CRS/SDET	B15	IO	OV _{DD}	—
GPIO_PB14/CLK12	D9	IO	OV _{DD}	—
GPIO_PB15 UPC1_TxADDR[4]	D14	IO	OV _{DD}	—
GPIO_PB16 UPC1_RxADDR[4]	B16	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Characteristic ¹	Max Operating Frequency	Unit
DDR1/DDR2 memory bus frequency (MCLK) ²	133	MHz
Local bus frequency (LCLKn) ³	66	MHz
PCI input frequency (CLKIN or PCI_CLK)	66	MHz

Table 57. Operating Frequencies for PBGA (continued)

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.

² The DDR1/DDR2 data rate is 2× the DDR1/DDR2 memory bus frequency.

³ The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

22.4 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = $2 \times (CSB \text{ frequency}) \times (System PLL VCO divider})$.

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 300–600 MHz.

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111-1111	Reserved

Table 58. System PLL Multiplication Factors

As described in Section 22, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59

Clocking

22.6 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. Table 61 shows the multiplication factor encodings for the QUICC Engine PLL.

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF)
00000-00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

Table 61. QUICC Engine PLL Multiplication Factors

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in Table 62.

Table 62. QUICC Engine PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

 $ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$

QUICC Engine VCO Frequency = $ce_clk \times VCO$ divider $\times (1 + CEPDF)$

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Document Number: MPC8323EEC Rev. 4 09/2010

