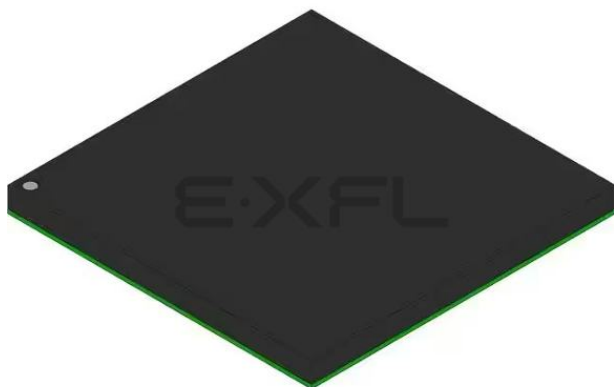




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2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	$OV_{DD} = 3.3\text{ V}$
PCI signals	25	
DDR1 signal	18	$GV_{DD} = 2.5\text{ V}$
DDR2 signal	18	$GV_{DD} = 1.8\text{ V}$
DUART, system control, I2C, SPI, JTAG	42	$OV_{DD} = 3.3\text{ V}$
GPIO signals	42	$OV_{DD} = 3.3\text{ V}$

2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input capacitance for all pins except CLKIN	C_I	6	8	pF	—
Input capacitance for CLKIN	$C_{I\text{CLKIN}}$	10	—	pF	1

Note:

1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and IO supply voltages (GV_{DD} and OV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD} and OV_{DD}) do not have any ordering requirements with respect to one another.

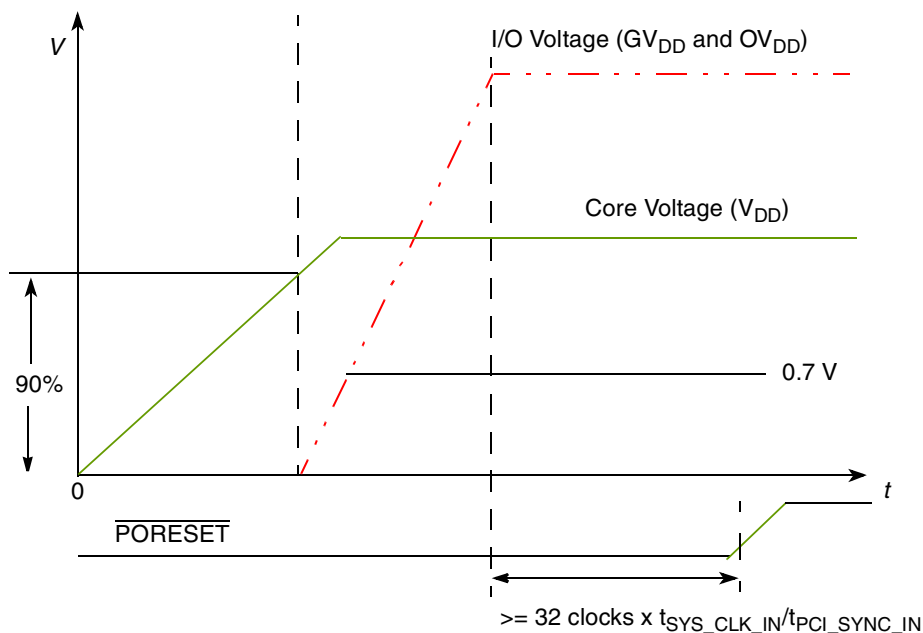


Figure 3. MPC8323E Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation for this family of MPC8323E devices is shown in [Table 5](#).

Table 5. MPC8323E Power Dissipation

CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Core Frequency (MHz)	Typical	Maximum	Unit	Notes
133	200	266	0.74	1.48	W	1, 2, 3
133	200	333	0.78	1.62	W	1, 2, 3

Notes:

1. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or AV_{DD} . For I/O power values, see [Table 6](#).
2. Typical power is based on a nominal voltage of $V_{DD} = 1.0$ V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the MPC8323MDS evaluation board using WC process silicon.
3. Maximum power is based on a voltage of $V_{DD} = 1.07$ V, WC process, a junction $T_J = 110^{\circ}\text{C}$, and an artificial smoke test.

[Table 6](#) shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V $R_s = 20\ \Omega$ $R_t = 50\ \Omega$ 1 pair of clocks	266 MHz, 1×32 bits	0.212	0.367	—	W	—

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
$\overline{\text{HRESET}}/\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

1. $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is in PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{\text{OH}} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$\text{OV}_{\text{DD}} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8323E.

7.1 DUART DC Electrical Characteristics

Table 20 provides the DC electrical characteristics for the DUART interface of the MPC8323E.

Table 20. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage OV_{DD}	V_{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V
Input current ($0 V \leq V_{IN} \leq OV_{DD}$) ¹	I_{IN}	—	± 5	μA

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 21 provides the AC timing parameters for the DUART interface of the MPC8323E.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:

- Actual attainable baud rate is limited by the latency of interrupt processing.
- The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet and MII Management

This section provides the AC and DC electrical characteristics for Ethernet and MII management.

8.1 Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics

The electrical characteristics specified here apply to all MII (media independent interface) and RMII (reduced media independent interface), except MDIO (management data input/output) and MDC

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 27](#).

Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—	2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$ $OV_{DD} = \text{Min}$	2.10	$OV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$ $OV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	2.00	—	V
Input low voltage	V_{IL}	—	—	0.80	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

8.3.2 MII Management AC Electrical Specifications

[Table 28](#) provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V $\pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 30. Local Bus General Timing Parameters (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock (LCLK _n) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK _n) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8
Local bus clock (LCLK _n) duty cycle	t_{LBDC}	47	53	%	—
Local bus clock (LCLK _n) jitter specification	t_{LBRJ}	—	400	ps	—
Delay between the input clock (PCI_SYNC_IN) of local bus output clock (LCLK _n)	t_{LBCTL}	—	1.7	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 14 provides the AC test load for the local bus.

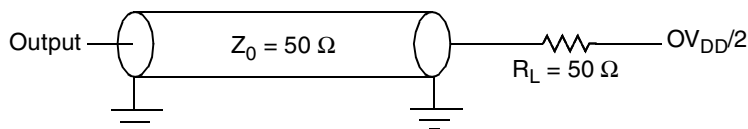

Figure 14. Local Bus C Test Load

Table 34. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol ¹	Min	Max	Unit
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b ⁴	300	ns
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns
Setup time for STOP condition	t _{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	0.1 × OV _{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	0.2 × OV _{DD}	—	V

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- MPC8323E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_B = capacitance of one bus line in pF.

Figure 23 provides the AC test load for the I²C.

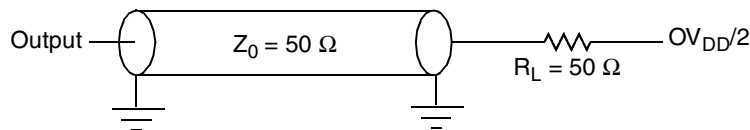
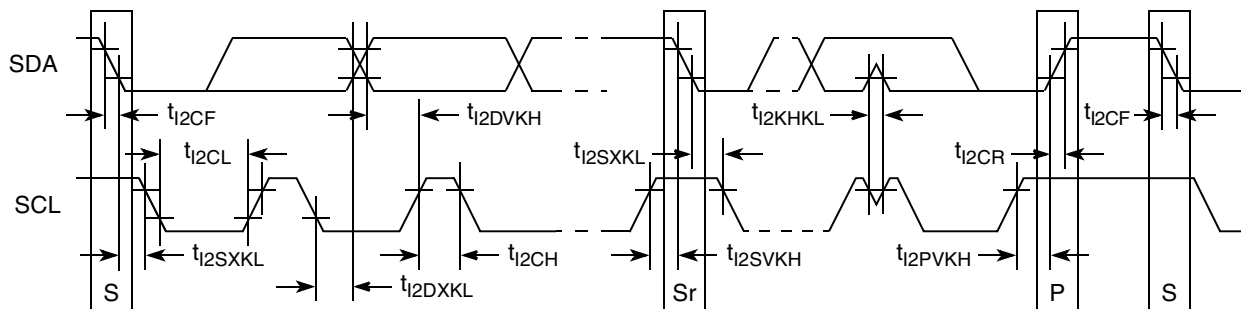

Figure 23. I²C AC Test Load

Figure 24 shows the AC timing diagram for the I²C bus.


Figure 24. I²C Bus AC Timing Diagram

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8323E.

12.1 PCI DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the PCI interface of the MPC8323E.

Table 35. PCI DC Electrical Characteristics^{1,2}

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL} \text{ (max)}$	-0.3	0.8	V
High-level output voltage	V_{OH}	$OV_{DD} = \text{min},$ $I_{OH} = -100 \mu\text{A}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	$OV_{DD} = \text{min},$ $I_{OL} = 100 \mu\text{A}$	—	0.2	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

Notes:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.
- Ranges listed do not meet the full range of the DC specifications of the *PCI 2.3 Local Bus Specifications*.

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8323E. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8323E is configured as a host or agent device. Table 36 shows the PCI AC timing specifications at 66 MHz.

Table 36. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.

Figure 27 shows the PCI output AC timing conditions.

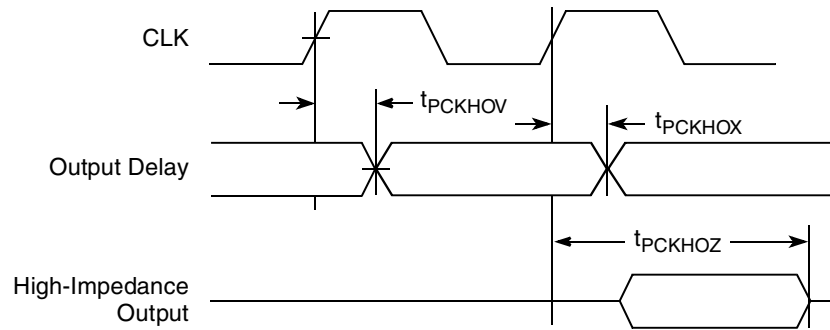


Figure 27. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8323E.

13.1 Timer DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the MPC8323E timer pins, including TIN, $\overline{\text{TOUT}}$, TGATE, and RTC_CLK.

Table 38. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

13.2 Timer AC Timing Specifications

Table 39 provides the timer input and output AC timing specifications.

Table 39. Timer Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Figure 28 provides the AC test load for the timers.

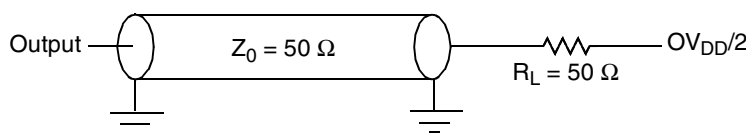


Figure 28. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8323E.

14.1 GPIO DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E GPIO.

Table 40. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA	—

Note:

1. This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

Table 41 provides the GPIO input and output AC timing specifications.

Table 41. GPIO Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Table 44. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	$t_{NIKH OV}$	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	$t_{NEKH OV}$	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{NIKH OV}$ symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 30 provides the AC test load for the SPI.

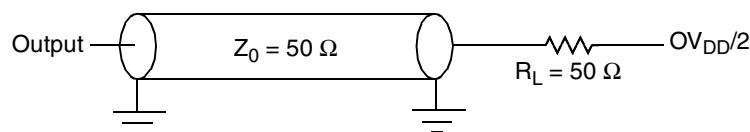


Figure 30. SPI AC Test Load

Table 46. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	—	±5	μA

17.2 TDM/SI AC Timing Specifications

Table 47 provides the TDM/SI input and output AC timing specifications.

Table 47. TDM/SI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	12	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 33 provides the AC test load for the TDM/SI.

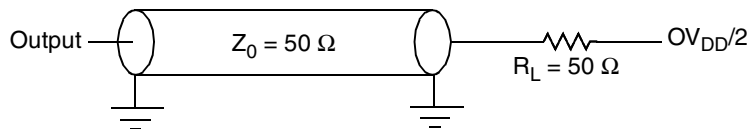
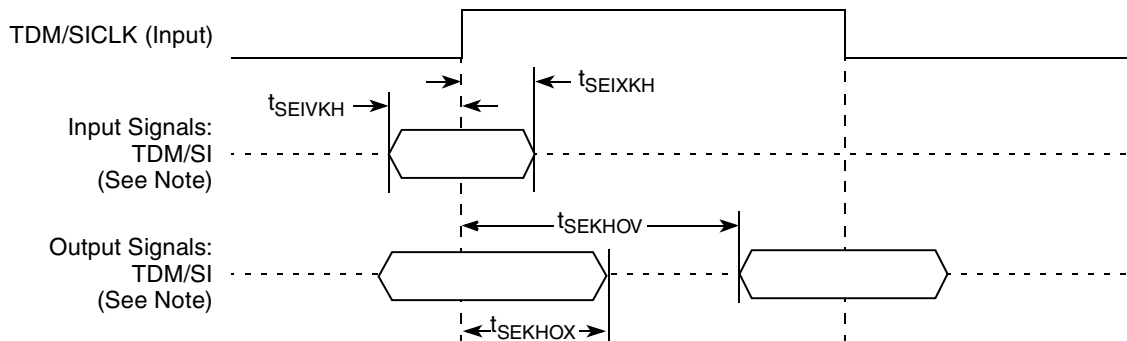

Figure 33. TDM/SI AC Test Load

Figure 34 represents the AC timing from Table 47. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on TDM/SI.

Figure 34. TDM/SI AC Timing (External Clock) Diagram

18 UTOPIA

This section describes the UTOPIA DC and AC electrical specifications of the MPC8323E.

NOTE

The MPC8321E and MPC8321 do not support UTOPIA.

18.1 UTOPIA DC Electrical Characteristics

Table 48 provides the DC electrical characteristics for the MPC8323E UTOPIA.

Table 48. UTOPIA DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

18.2 UTOPIA AC Timing Specifications

Table 49 provides the UTOPIA input and output AC timing specifications.

Table 49. UTOPIA AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
UTOPIA outputs—Internal clock delay	t_{UIKHOV}	0	5.5	ns
UTOPIA outputs—External clock delay	t_{UEKHOV}	1	8	ns
UTOPIA outputs—Internal clock high impedance	t_{UIKHOX}	0	5.5	ns
UTOPIA outputs—External clock high impedance	t_{UEKHOX}	1	8	ns
UTOPIA inputs—Internal clock input setup time	t_{UIIVKH}	8	—	ns
UTOPIA inputs—External clock input setup time	t_{UEIVKH}	4	—	ns
UTOPIA inputs—Internal clock input hold time	t_{UIIXKH}	0	—	ns
UTOPIA inputs—External clock input hold time	t_{UEIXKH}	1	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 35 provides the AC test load for the UTOPIA.

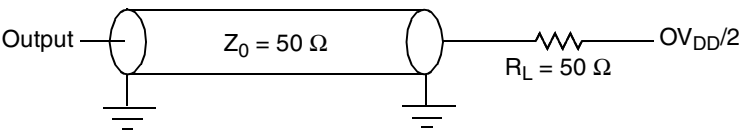


Figure 35. UTOPIA AC Test Load

Figure 36 and Figure 37 represent the AC timing from Table 49. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 36 shows the UTOPIA timing with external clock.

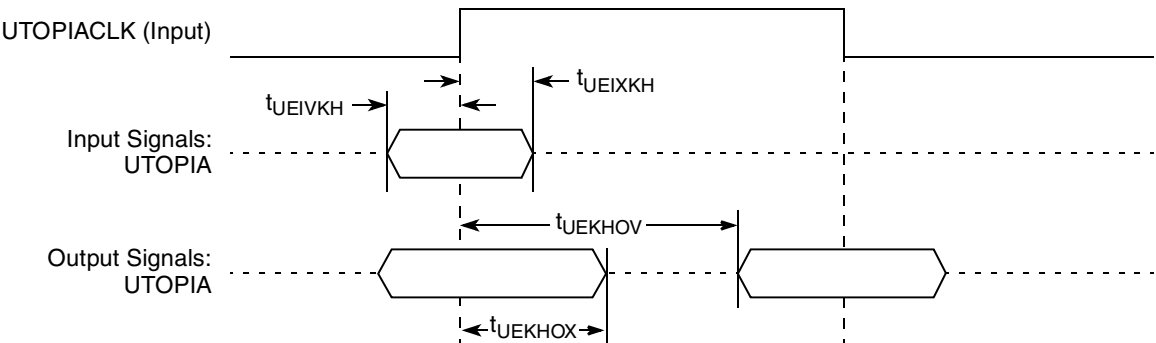


Figure 36. UTOPIA AC Timing (External Clock) Diagram

Figure 37 shows the UTOPIA timing with internal clock.

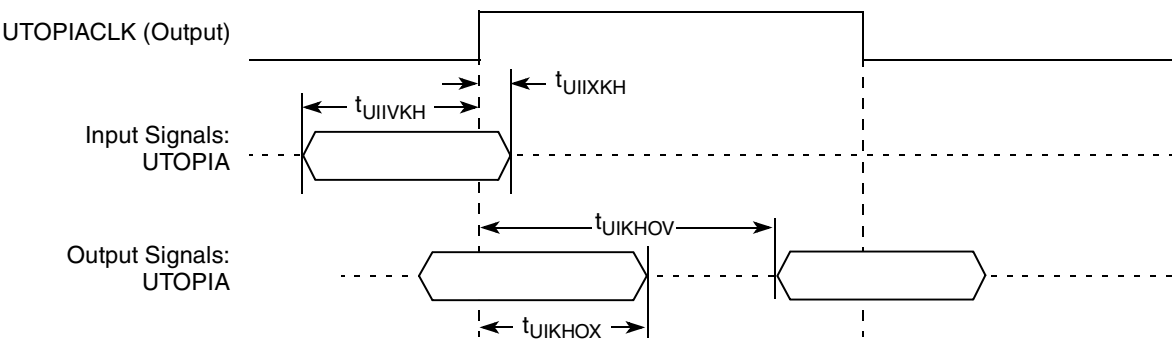


Figure 37. UTOPIA AC Timing (Internal Clock) Diagram

20 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8323E.

20.1 USB DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the USB interface.

Table 53. USB DC Electrical Characteristics¹

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V
Input current	I_{IN}	—	± 5	μA

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

20.2 USB AC Electrical Specifications

Table 54 describes the general timing parameters of the USB interface of the MPC8323E.

Table 54. USB General Timing Parameters

Parameter	Symbol ¹	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	20.83	—	ns	Full speed 48 MHz
USB clock cycle time	t_{USCK}	166.67	—	ns	Low speed 6 MHz
Skew between TXP and TXN	t_{USTSPN}	—	5	ns	—
Skew among RXP, RXN, and RXD	$t_{USRSPND}$	—	10	ns	Full speed transitions
Skew among RXP, RXN, and RXD	t_{USRPND}	—	100	ns	Low speed transitions

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(state)(signal)}$ for receive signals and $t_{(first\ two\ letters\ of\ functional\ block)(state)(signal)}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
- Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

Figure 41 provide the AC test load for the USB.

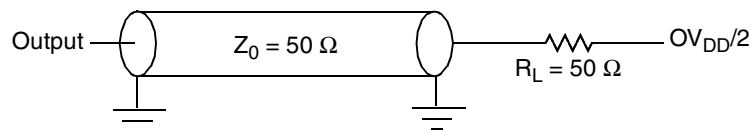


Figure 41. USB AC Test Load

21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

Table 55. MPC8323E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	AE9	IO	GV _{DD}	—
MEMC_MDQ1	AD10	IO	GV _{DD}	—
MEMC_MDQ2	AF10	IO	GV _{DD}	—
MEMC_MDQ3	AF9	IO	GV _{DD}	—
MEMC_MDQ4	AF7	IO	GV _{DD}	—
MEMC_MDQ5	AE10	IO	GV _{DD}	—
MEMC_MDQ6	AD9	IO	GV _{DD}	—
MEMC_MDQ7	AF8	IO	GV _{DD}	—
MEMC_MDQ8	AE6	IO	GV _{DD}	—
MEMC_MDQ9	AD7	IO	GV _{DD}	—
MEMC_MDQ10	AF6	IO	GV _{DD}	—
MEMC_MDQ11	AC7	IO	GV _{DD}	—
MEMC_MDQ12	AD8	IO	GV _{DD}	—
MEMC_MDQ13	AE7	IO	GV _{DD}	—
MEMC_MDQ14	AD6	IO	GV _{DD}	—
MEMC_MDQ15	AF5	IO	GV _{DD}	—
MEMC_MDQ16	AD18	IO	GV _{DD}	—
MEMC_MDQ17	AE19	IO	GV _{DD}	—
MEMC_MDQ18	AF17	IO	GV _{DD}	—
MEMC_MDQ19	AF19	IO	GV _{DD}	—
MEMC_MDQ20	AF18	IO	GV _{DD}	—
MEMC_MDQ21	AE18	IO	GV _{DD}	—
MEMC_MDQ22	AF20	IO	GV _{DD}	—
MEMC_MDQ23	AD19	IO	GV _{DD}	—
MEMC_MDQ24	AD21	IO	GV _{DD}	—
MEMC_MDQ25	AF22	IO	GV _{DD}	—
MEMC_MDQ26	AC21	IO	GV _{DD}	—
MEMC_MDQ27	AF21	IO	GV _{DD}	—
MEMC_MDQ28	AE21	IO	GV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE/GPIO				
GPIO_PA0/SER1_TXD[0]/TDMA_TXD[0]/USBTXN	G3	IO	OV _{DD}	—
GPIO_PA1/SER1_TXD[1]/TDMA_TXD[1]/USBTXP	F3	IO	OV _{DD}	—
GPIO_PA2/SER1_TXD[2]/TDMA_TXD[2]	F2	IO	OV _{DD}	—
GPIO_PA3/SER1_TXD[3]/TDMA_TXD[3]	E3	IO	OV _{DD}	—
GPIO_PA4/SER1_RXD[0]/TDMA_RXD[0]/USBRXP	E2	IO	OV _{DD}	—
GPIO_PA5/SER1_RXD[1]/TDMA_RXD[1]/USBRXN	E1	IO	OV _{DD}	—
GPIO_PA6/SER1_RXD[2]/TDMA_RXD[2]/USBRXD	D3	IO	OV _{DD}	—
GPIO_PA7/SER1_RXD[3]/TDMA_RXD[3]	D2	IO	OV _{DD}	—
GPIO_PA8/SER1_CD/TDMA_REQ/ $\overline{\text{USBOE}}$	D1	IO	OV _{DD}	—
GPIO_PA9 TDMA_CLKO	C3	IO	OV _{DD}	—
GPIO_PA10/SER1_CTS/TDMA_RSYNC	C2	IO	OV _{DD}	—
GPIO_PA11/TDMA_STROBE	C1	IO	OV _{DD}	—
GPIO_PA12/SER1_RTS/TDMA_TSYNC	B1	IO	OV _{DD}	—
GPIO_PA13/CLK9/BRGO9	H4	IO	OV _{DD}	—
GPIO_PA14/CLK11/BRGO10	G4	IO	OV _{DD}	—
GPIO_PA15/BRGO7	J4	IO	OV _{DD}	—
GPIO_PA16/ LA0 (LBIU)	K24	IO	OV _{DD}	—
GPIO_PA17/ LA1 (LBIU)	K26	IO	OV _{DD}	—
GPIO_PA18/Enet2_TXD[0]/SER2_TXD[0]/TDMB_TXD[0]/LA2 (LBIU)	G25	IO	OV _{DD}	—
GPIO_PA19/Enet2_TXD[1]/SER2_TXD[1]/TDMB_TXD[1]/LA3 (LBIU)	G26	IO	OV _{DD}	—
GPIO_PA20/Enet2_TXD[2]/SER2_TXD[2]/TDMB_TXD[2]/LA4 (LBIU)	H25	IO	OV _{DD}	—
GPIO_PA21/Enet2_TXD[3]/SER2_TXD[3]/TDMB_TXD[3]/LA5 (LBIU)	H26	IO	OV _{DD}	—
GPIO_PA22/Enet2_RXD[0]/SER2_RXD[0]/TDMB_RXD[0]/LA6 (LBIU)	C25	IO	OV _{DD}	—
GPIO_PA23/Enet2_RXD[1]/SER2_RXD[1]/TDMB_RXD[1]/LA7 (LBIU)	C26	IO	OV _{DD}	—
GPIO_PA24/Enet2_RXD[2]/SER2_RXD[2]/TDMB_RXD[2]/LA8 (LBIU)	D25	IO	OV _{DD}	—
GPIO_PA25/Enet2_RXD[3]/SER2_RXD[3]/TDMB_RXD[3]/LA9 (LBIU)	D26	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PA26/Enet2_RX_ER/SER2_CD/TDMB_REQ/LA10 (LBIU)	E26	IO	OV _{DD}	—
GPIO_PA27/Enet2_TX_ER/TDMB_CLKO/LA11 (LBIU)	F25	IO	OV _{DD}	—
GPIO_PA28/Enet2_RX_DV/SER2_CTS/TDMB_RSYNC/LA12 (LBIU)	E25	IO	OV _{DD}	—
GPIO_PA29/Enet2_COL/RXD[4]/SER2_RXD[4]/TDMB_STROBE/LA13 (LBIU)	J25	IO	OV _{DD}	—
GPIO_PA30/Enet2_TX_EN/SER2_RTS/TDMB_TSYNC/LA14 (LBIU)	F26	IO	OV _{DD}	—
GPIO_PA31/Enet2_CRS/SDET LA15 (LBIU)	J26	IO	OV _{DD}	—
GPIO_PB0/Enet3_TXD[0]/SER3_TXD[0]/TDMC_TXD[0]	A13	IO	OV _{DD}	—
GPIO_PB1/Enet3_TXD[1]/SER3_TXD[1]/TDMC_TXD[1]	B13	IO	OV _{DD}	—
GPIO_PB2/Enet3_TXD[2]/SER3_TXD[2]/TDMC_TXD[2]	A14	IO	OV _{DD}	—
GPIO_PB3/Enet3_TXD[3]/SER3_TXD[3]/TDMC_TXD[3]	B14	IO	OV _{DD}	—
GPIO_PB4/Enet3_RXD[0]/SER3_RXD[0]/TDMC_RXD[0]	B8	IO	OV _{DD}	—
GPIO_PB5/Enet3_RXD[1]/SER3_RXD[1]/TDMC_RXD[1]	A8	IO	OV _{DD}	—
GPIO_PB6/Enet3_RXD[2]/SER3_RXD[2]/TDMC_RXD[2]	A9	IO	OV _{DD}	—
GPIO_PB7/Enet3_RXD[3]/SER3_RXD[3]/TDMC_RXD[3]	B9	IO	OV _{DD}	—
GPIO_PB8/Enet3_RX_ER/SER3_CD/TDMC_REQ	A11	IO	OV _{DD}	—
GPIO_PB9/Enet3_TX_ER/TDMC_CLKO	B11	IO	OV _{DD}	—
GPIO_PB10/Enet3_RX_DV/SER3_CTS/TDMC_RSYNC	A10	IO	OV _{DD}	—
GPIO_PB11/Enet3_COL/RXD[4]/SER3_RXD[4]/TDMC_STROBE	A15	IO	OV _{DD}	—
GPIO_PB12/Enet3_TX_EN/SER3_RTS/TDMC_TSYNC	B12	IO	OV _{DD}	—
GPIO_PB13/Enet3_CRS/SDET	B15	IO	OV _{DD}	—
GPIO_PB14/CLK12	D9	IO	OV _{DD}	—
GPIO_PB15 UPC1_TxADDR[4]	D14	IO	OV _{DD}	—
GPIO_PB16 UPC1_RxADDR[4]	B16	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PB17/BRGO1/CE_EXT_REQ1	D10	IO	OV _{DD}	—
GPIO_PB18/Enet4_TXD[0]/SER4_TXD[0]/TDMD_TXD[0]	C10	IO	OV _{DD}	—
GPIO_PB19/Enet4_TXD[1]/SER4_TXD[1]/TDMD_TXD[1]	C9	IO	OV _{DD}	—
GPIO_PB20/Enet4_TXD[2]/SER4_TXD[2]/TDMD_TXD[2]	D8	IO	OV _{DD}	—
GPIO_PB21/Enet4_TXD[3]/SER4_TXD[3]/TDMD_TXD[3]	C8	IO	OV _{DD}	—
GPIO_PB22/Enet4_RXD[0]/SER4_RXD[0]/TDMD_RXD[0]	C15	IO	OV _{DD}	—
GPIO_PB23/Enet4_RXD[1]/SER4_RXD[1]/TDMD_RXD[1]	C14	IO	OV _{DD}	—
GPIO_PB24/Enet4_RXD[2]/SER4_RXD[2]/TDMD_RXD[2]	D13	IO	OV _{DD}	—
GPIO_PB25/Enet4_RXD[3]/SER4_RXD[3]/TDMD_RXD[3]	C13	IO	OV _{DD}	—
GPIO_PB26/Enet4_RX_ER/SER4_CD/TDMD_REQ	C12	IO	OV _{DD}	—
GPIO_PB27/Enet4_TX_ER/TDMD_CLKO	D11	IO	OV _{DD}	—
GPIO_PB28/Enet4_RX_DV/SER4_CTS/TDMD_RSYNC	D12	IO	OV _{DD}	—
GPIO_PB29/Enet4_COL/RXD[4]/SER4_RXD[4]/TDMD_STROBE	D7	IO	OV _{DD}	—
GPIO_PB30/Enet4_TX_EN/SER4_RTS/TDMD_TSYNC	C11	IO	OV _{DD}	—
GPIO_PB31/Enet4_CRS/SDET	C7	IO	OV _{DD}	—
GPIO_PC0/UPC1_TxDATA[0]/SER5_TXD[0]	A18	IO	OV _{DD}	—
GPIO_PC1/UPC1_TxDATA[1]/SER5_TXD[1]	A19	IO	OV _{DD}	—
GPIO_PC2/UPC1_TxDATA[2]/SER5_TXD[2]	B18	IO	OV _{DD}	—
GPIO_PC3/UPC1_TxDATA[3]/SER5_TXD[3]	B19	IO	OV _{DD}	—
GPIO_PC4/UPC1_TxDATA[4]	A24	IO	OV _{DD}	—
GPIO_PC5/UPC1_TxDATA[5]	B24	IO	OV _{DD}	—
GPIO_PC6/UPC1_TxDATA[6]	A23	IO	OV _{DD}	—
GPIO_PC7/UPC1_TxDATA[7]	B26	IO	OV _{DD}	—
GPIO_PC8/UPC1_RxDATA[0]/SER5_RXD[0]	A21	IO	OV _{DD}	—
GPIO_PC9/UPC1_RxDATA[1]/SER5_RXD[1]	B20	IO	OV _{DD}	—

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

24.7 Pull-Up Resistor Requirements

The MPC8323E requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins including I²C pins, Ethernet Management MDIO pin, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see AN3361, “MPC8321E/MPC8323E PowerQUICC Design Checklist,” Rev. 1.

25 Ordering Information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in [Section 25.1, “Part Numbers Fully Addressed by This Document.”](#)

25.1 Part Numbers Fully Addressed by This Document

[Table 66](#) provides the Freescale part numbering nomenclature for the MPC8323E family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

Table 66. Part Numbering Nomenclature

MPC	nnnn	E	C	VR	AF	D	C	A
Product Code	Part Identifier	Encryption Acceleration	Temperature Range ¹	Package ²	e300 Core Frequency ³	DDR Frequency	QUICC Engine Frequency	Revision Level
MPC	8323	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	VR = Pb-free PBGA ZQ = Pb PBGA	AD = 266 MHz AF = 333 MHz	D = 266 MHz	C = 200 MHz	Contact local Freescale sales office

Notes:

1. Contact local Freescale office on availability of parts with C temperature range.
2. See [Section 21, “Package and Pin Listings,”](#) for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.