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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8321ecvraddc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTE

The QUICC Engine block can also support a UTOPIA level 2 capable of supporting 31 multi-PHY (MPC8323E- and MPC8323-specific).

The MPC8323E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In summary, the MPC8323E family provides users with a highly integrated, fully programmable communications processor. This helps ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

1.1 MPC8323E Features

Major features of the MPC8323E are as follows:

- High-performance, low-power, and cost-effective single-chip data-plane/control-plane solution for ATM or IP/Ethernet packet processing (or both).
- MPC8323E QUICC Engine block offers a future-proof solution for next generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards.
- Single platform architecture supports the convergence of IP packet networks and ATM networks.
- DDR1/DDR2 memory controller—one 32-bit interface at up to 266 MHz supporting both DDR1 and DDR2.
- An e300c2 core built on Power Architecture technology with 16-Kbyte instruction and data caches, and dual integer units.
- Peripheral interfaces such as 32-bit PCI (2.2) interface up to 66-MHz operation, 16-bit local bus interface up to 66-MHz operation, and USB 2.0 (full-/low-speed).
- Security engine provides acceleration for control and data plane security protocols.
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration.

1.1.1 Protocols

The protocols are as follows:

- ATM SAR up to 155 Mbps (OC-3) full duplex, with ATM traffic shaping (ATF TM4.1)
- Support for ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- Support for IMA and ATM transmission convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- Support for 64 channels of HDLC/transparent



Electrical Characteristics

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV _{DD} = 3.3 V
PCI signals	25	
DDR1 signal	18	GV _{DD} = 2.5 V
DDR2 signal	18	GV _{DD} = 1.8 V
DUART, system control, I2C, SPI, JTAG	42	OV _{DD} = 3.3 V
GPIO signals	42	OV _{DD} = 3.3 V

Table 3. Output Drive Capability

2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input capacitance for all pins except CLKIN	CI	6	8	pF	_
Input capacitance for CLKIN	C _{ICLKIN}	10		pF	1

Note:

1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and IO supply voltages (GV_{DD}) and $OV_{DD})$ to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}) and OV_{DD} and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD}) and OV_{DD} do not have any ordering requirements with respect to one another.



Parameter/Condition	Min	Max	Unit	Notes
HRESET/SRESET assertion (output)	512	_	t _{PCI_SYNC_IN}	1
HRESET negation to SRESET negation (output)	16		t _{PCI_SYNC_IN}	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8323E is in PCI host mode	4	_	^t CLKIN	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8323E is in PCI agent mode	4	_	^t PCI_SYNC_IN	1
Input hold time for POR config signals with respect to negation of HRESET	0	_	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of $\overrightarrow{\text{HRESET}}$	_	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of HRESET	1	_	^t PCI_SYNC_IN	1, 3

Table 9. RESET Initialization Timing Specifications (continued)

Notes:

1. t_{PCI_SYNC_IN} is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.

 t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual for more details.

3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Мах	Unit	Notes
PLL lock times		100	μs	_

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V	1
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V	1
Input low voltage	V _{IL}	_	-0.3	0.8	V	_



DDR1 and DDR2 SDRAM

Figure 4 shows the input timing diagram for the DDR controller.



Figure 4. DDR Input Timing Diagram

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

Table 19 provides the output AC timing specifications for the DDR1 and DDR2 SDRAM interfaces.

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with Dn_GV_{DD} of (1.8 or 2.5 V) \pm 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK cycle time, (MCK/MCK crossing)	t _{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	^t DDKHAS	2.5 3.5		ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t _{DDKHAX}	2.5 3.5		ns	3
MCS output setup with respect to MCK 266 MHz 200 MHz	t _{DDKHCS}	2.5 3.5		ns	3
MCS output hold with respect to MCK 266 MHz 200 MHz	^t DDKHCX	2.5 3.5		ns	3
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4



Local Bus

Figure 13 shows the MII management AC timing diagram.



Figure 13. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8323E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
High-level output voltage, I _{OH} = −100 μA	V _{OH}	OV _{DD} – 0.2	—	V
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V
Input current	I _{IN}	—	±5	μA

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8323E.

Table 30. Local Bus General Timing Parameters

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	15	—	ns	2
Input setup to local bus clock (LCLKn)	t _{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLKn)	t _{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT1}	1.5	—	ns	5



Parameter	Symbol ¹	Min	Мах	Unit	Notes
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3	_	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	_	ns	7
Local bus clock (LCLKn) to output valid	t _{LBKHOV}	—	3	ns	3
Local bus clock (LCLKn) to output high impedance for LAD/LDP	t _{LBKHOZ}	—	4	ns	8
Local bus clock (LCLKn) duty cycle	t _{LBDC}	47	53	%	_
Local bus clock (LCLKn) jitter specification	t _{LBRJ}	—	400	ps	_
Delay between the input clock (PCI_SYNC_IN) of local bus output clock (LCLK <i>n</i>)	t _{LBCDL}	—	1.7	ns	_

Table 30. Local Bus General Timing Parameters (continued)

Notes:

The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).

2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).

All signals are measured from OV_{DD}/2 of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.

4. Input timings are measured at the pin.

5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.

 t_{LBOTOT2} should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.

7. t_{LBOTOT3} should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.

8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 14 provides the AC test load for the local bus.



Figure 14. Local Bus C Test Load



Figure 15 through Figure 17 show the local bus signals.





Table 32. JTAG AC Timing Specifications (Independent of CLKIN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{JTKLDZ} t _{JTKLOZ}	2 2	19 9	ns	5, 6 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

- 2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K)} going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4. Non-JTAG signal input timing with respect to t_{TCLK}.

- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design and characterization.

Figure 18 provides the AC test load for TDO and the boundary-scan outputs of the MPC8323E.



Figure 18. AC Test Load for the JTAG Interface

Figure 19 provides the JTAG clock input timing diagram.



Figure 19. JTAG Clock Input Timing Diagram

Figure 20 provides the TRST timing diagram.





1²C

Table 34. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol ¹	Min	Мах	Unit
Rise time of both SDA and SCL signals	t _{l2CR}	20 + 0.1 C _b ⁴	300	ns
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns
Setup time for STOP condition	t _{I2PVKH}	0.6		μs
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3		μs
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	Ι	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times \text{OV}_{\text{DD}}$	_	V

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

- MPC8323E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

4. C_B = capacitance of one bus line in pF.

Figure 23 provides the AC test load for the I^2C .



Figure 23. I²C AC Test Load

Figure 24 shows the AC timing diagram for the I^2C bus.



Figure 24. I²C Bus AC Timing Diagram



Figure 28 provides the AC test load for the timers.



14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8323E.

14.1 GPIO DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E GPIO.

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V	1
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V	1
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V	1
Input low voltage	V _{IL}	—	-0.3	0.8	V	—
Input current	I _{IN}	$0 \ V \leq V_{IN} \leq OV_{DD}$	_	±5	μA	—

Table 40. GPIO DC Electrical Characteristics

Note:

1. This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

Table 41 provides the GPIO input and output AC timing specifications.

Table 41. GPIO Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.



Figure 29 provides the AC test load for the GPIO.



15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8323E.

15.1 IPIC DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the external interrupt pins of the MPC8323E.

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	—	±5	μA
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

Table 42. IPIC DC Electrical Characteristics^{1,2}

Notes:

1. This table applies for pins IRQ[0:7], IRQ_OUT, MCP_OUT, and CE ports Interrupts.

2. IRQ_OUT and MCP_OUT are open drain pins, thus V_{OH} is not relevant for those pins.

15.2 IPIC AC Timing Specifications

Table 43 provides the IPIC input and output AC timing specifications.

Table 43. IPIC Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any
external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working
in edge triggered mode.



18 UTOPIA

This section describes the UTOPIA DC and AC electrical specifications of the MPC8323E.

NOTE

The MPC8321E and MPC8321 do not support UTOPIA.

18.1 UTOPIA DC Electrical Characteristics

Table 48 provides the DC electrical characteristics for the MPC8323E UTOPIA.

Table 48. UTOPIA DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

18.2 UTOPIA AC Timing Specifications

Table 49 provides the UTOPIA input and output AC timing specifications.

Table 49. UTOPIA AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
UTOPIA outputs—Internal clock delay	^t UIKHOV	0	5.5	ns
UTOPIA outputs—External clock delay	t _{UEKHOV}	1	8	ns
UTOPIA outputs—Internal clock high impedance	tuikhox	0	5.5	ns
UTOPIA outputs—External clock high impedance	t _{UEKHOX}	1	8	ns
UTOPIA inputs—Internal clock input setup time	t _{UIIVKH}	8	—	ns
UTOPIA inputs—External clock input setup time	t _{UEIVKH}	4	—	ns
UTOPIA inputs—Internal clock input hold time	t _{∪IIXKH}	0	—	ns
UTOPIA inputs—External clock input hold time	t _{UEIXKH}	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).}}

HDLC, BISYNC, Transparent, and Synchronous UART

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications¹ (continued)

Characteristic	Symbol ²	Min	Мах	Unit
Inputs—External clock input hold time	t _{HEIXKH}	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).}

Table 52. Synchronous UART AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock delay	t _{UAIKHOV}	0	5.5	ns
Outputs—External clock delay	t _{UAEKHOV}	1	10	ns
Outputs—Internal clock high impedance	t _{UAIKHOX}	0	5.5	ns
Outputs—External clock high impedance	t _{UAEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t _{UAIIVKH}	6	—	ns
Inputs—External clock input setup time	t _{UAEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t _{UAIIXKH}	0	—	ns
Inputs—External clock input hold time	t _{UAEIXKH}	1	—	ns

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{UAIKHOX} symbolizes the outputs internal timing (UAI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub>

Figure 38 provides the AC test load.



Figure 38. AC Test Load

Figure 39 and Figure 40 represent the AC timing from Table 51. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Package and Pin Listings



Notes:

1.All dimensions are in millimeters.

2.Dimensions and tolerances per ASME Y14.5M-1994.

3.Maximum solder ball diameter measured parallel to datum A.

4.Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 42. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8323E PBGA



21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

Table 55. MPC8323E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Men	nory Controller Interface			
MEMC_MDQ0	AE9	IO	GV _{DD}	—
MEMC_MDQ1	AD10	IO	GV _{DD}	—
MEMC_MDQ2	AF10	IO	GV _{DD}	—
MEMC_MDQ3	AF9	IO	GV _{DD}	—
MEMC_MDQ4	AF7	IO	GV _{DD}	—
MEMC_MDQ5	AE10	IO	GV _{DD}	—
MEMC_MDQ6	AD9	IO	GV _{DD}	—
MEMC_MDQ7	AF8	IO	GV _{DD}	—
MEMC_MDQ8	AE6	IO	GV _{DD}	—
MEMC_MDQ9	AD7	IO	GV _{DD}	—
MEMC_MDQ10	AF6	IO	GV _{DD}	—
MEMC_MDQ11	AC7	IO	GV _{DD}	—
MEMC_MDQ12	AD8	IO	GV _{DD}	—
MEMC_MDQ13	AE7	IO	GV _{DD}	—
MEMC_MDQ14	AD6	IO	GV _{DD}	—
MEMC_MDQ15	AF5	IO	GV _{DD}	—
MEMC_MDQ16	AD18	IO	GV _{DD}	—
MEMC_MDQ17	AE19	IO	GV _{DD}	—
MEMC_MDQ18	AF17	IO	GV _{DD}	—
MEMC_MDQ19	AF19	IO	GV _{DD}	—
MEMC_MDQ20	AF18	IO	GV _{DD}	—
MEMC_MDQ21	AE18	IO	GV _{DD}	—
MEMC_MDQ22	AF20	Ю	GV _{DD}	—
MEMC_MDQ23	AD19	IO	GV _{DD}	—
MEMC_MDQ24	AD21	IO	GV _{DD}	—
MEMC_MDQ25	AF22	IO	GV _{DD}	—
MEMC_MDQ26	AC21	IO	GV _{DD}	—
MEMC_MDQ27	AF21	IO	GV _{DD}	—
MEMC_MDQ28	AE21	IO	GV _{DD}	



Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ3	J2	1	OV _{DD}	—
IRQ4	J1	I	OV _{DD}	—
IRQ5	AE26	I	OV _{DD}	—
IRQ6/CKSTOP_OUT	AE25	IO	OV _{DD}	—
IRQ7/CKSTOP_IN	AF25	I	OV _{DD}	—
CFG_CLKIN_DIV	F1	I	OV _{DD}	—
CFG_LBIU_MUX_EN	M23	I	OV _{DD}	—
	JTAG		•	
тск	W26	I	OV _{DD}	—
TDI	Y26	I	OV _{DD}	4
TDO	AA26	0	OV _{DD}	3
TMS	AB26	I	OV _{DD}	4
TRST	AC26	I	OV _{DD}	4
	TEST		•	
TEST_MODE	N23	I	OV _{DD}	6
	РМС		•	
QUIESCE	T23	0	OV _{DD}	—
	System Control			
HRESET	AC23	IO	OV _{DD}	1
PORESET	AD23	I	OV _{DD}	—
SRESET	AD24	IO	OV _{DD}	2
	Clocks			
CLKIN	R3	I	OV _{DD}	_
CLKIN	P4	0	OV _{DD}	—
PCI_SYNC_OUT	V1	0	OV _{DD}	3
RTC_PIT_CLOCK	U23	I	OV _{DD}	—
PCI_SYNC_IN/PCI_CLK	V2	I	OV _{DD}	—
PCI_CLK0/clkpd_cerisc1_ipg_clkout/DPTC_OSC	ТЗ	0	OV _{DD}	—
PCI_CLK1/clkpd_half_cemb4ucc1_ipg_clkout/ CLOCK_XLB_CLOCK_OUT	U2	0	OV _{DD}	—
PCI_CLK2/clkpd_third_cesog_ipg_clkout/ cecl_ipg_ce_clock	R4	0	OV _{DD}	

Table 55. MPC8323E PBGA Pinout Listing (continued)



Characteristic ¹	Max Operating Frequency	Unit
DDR1/DDR2 memory bus frequency (MCLK) ²	133	MHz
Local bus frequency (LCLKn) ³	66	MHz
PCI input frequency (CLKIN or PCI_CLK)	66	MHz

Table 57. Operating Frequencies for PBGA (continued)

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.

² The DDR1/DDR2 data rate is 2× the DDR1/DDR2 memory bus frequency.

³ The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

22.4 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = $2 \times (CSB \text{ frequency}) \times (System PLL VCO divider})$.

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 300–600 MHz.

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111-1111	Reserved

Table 58. System PLL Multiplication Factors

As described in Section 22, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59



Clocking

22.6 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. Table 61 shows the multiplication factor encodings for the QUICC Engine PLL.

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF)
00000-00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

Table 61. QUICC Engine PLL Multiplication Factors

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in Table 62.

Table 62. QUICC Engine PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

 $ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$

QUICC Engine VCO Frequency = $ce_clk \times VCO$ divider $\times (1 + CEPDF)$



NP

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 44 shows the PLL power supply filter circuit.



Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8323E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8323E system, and the MPC8323E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , and GV_{DD} pins of the MPC8323E. These decoupling capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , OV_{DD} , and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , or GV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , OV_{DD} , and GND pins of the MPC8323E.

24.5 Output Buffer DC Impedance

The MPC8323E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The

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