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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8321evrafdc

1.1.2 Serial Interfaces

The MPC8323E serial interfaces are as follows:

- Support for one UL2 interface with 31 multi-PHY addresses (MPC8323E and MPC8323 only)
- Support for up to three 10/100 Mbps Ethernet interfaces using MII or RMII
- Support for up to four T1/E1/J1/E3 or DS-3 serial interfaces (TDM)
- Support for dual UART and SPI interfaces and a single I²C interface

1.2 QUICC Engine Block

The QUICC Engine block is a versatile communications complex that integrates several communications peripheral controllers. It provides on-chip system design for a variety of applications, particularly in communications and networking systems. The QUICC Engine block has the following features:

- One 32-bit RISC controller for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
 - 10/100 Mbps Ethernet/IEEE 802.3® standard
 - IP support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
 - ATM protocol through UTOPIA interface (note that the MPC8321 and MPC8321E do not support the UTOPIA interface)
 - HDLC /transparent up to 70-Mbps full-duplex
 - HDLC bus up to 10 Mbps
 - Asynchronous HDLC
 - UART
 - BISYNC up to 2 Mbps
 - QUICC multi-channel controller (QMC) for 64 TDM channels
- One UTOPIA interface (UPC1) supporting 31 multi-PHYs (MPC8323E- and MPC8323-specific)
- Two serial peripheral interfaces (SPI). SPI2 is dedicated to Ethernet PHY management.
- Four TDM interfaces
- Thirteen independent baud rate generators and 19 input clock pins for supplying clocks to UCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

The UCCs are similar to the PowerQUICC II peripherals: SCC (BISYNC, UART, and HDLC bus) and FCC (fast Ethernet, HDLC, transparent, and ATM).

1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i™ standard, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8323E DDR1/DDR2 memory controller includes the following features:

- Single 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266-MHz data rate
- Support for two ×16 devices
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O
- Support for 1 chip select only
- FCRAM, ECC, hardware/software calibration, bit deskew, QIN stage, or atomic logic are not supported.

1.5 PCI Controller

The MPC8323E PCI controller includes the following features:

- *PCI Specification Revision 2.3* compatible
- Single 32-bit data PCI interface operates up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

1.6 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 35 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

Table 7. CLKIN DC Electrical Characteristics (continued)

CLKIN input current	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	± 5	μA
PCI_SYNC_IN input current	$0\text{ V} \leq V_{IN} \leq 0.5\text{ V}$ or $OV_{DD} - 0.5\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	± 5	μA
PCI_SYNC_IN input current	$0.5\text{ V} \leq V_{IN} \leq OV_{DD} - 0.5\text{ V}$	I_{IN}	—	± 50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 8 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the MPC8323E.

Table 8. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	25	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN rise and fall time	t_{KH}, t_{KL}	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	± 150	ps	4, 5

Notes:

- Caution:** The system, core, security, and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

5 RESET Initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8323E. Table 9 provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of \overline{HRESET} or \overline{SRESET} (input) to activate reset flow	32	—	$t_{PCI_SYNC_IN}$	1
Required assertion time of $\overline{PORESET}$ with stable clock applied to CLKIN when the MPC8323E is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{PORESET}$ with stable clock applied to PCI_SYNC_IN when the MPC8323E is in PCI agent mode	32	—	$t_{PCI_SYNC_IN}$	1

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR1 and DDR2 SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM ($Dn_GV_{DD}(typ) = 1.8\text{ V}$).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with Dn_GV_{DD} of $1.8 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MVREFn_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MVREFn_{REF} + 0.25$	—	V	—

Table 17 provides the input AC timing specifications for the DDR1 SDRAM ($Dn_GV_{DD}(typ) = 2.5\text{ V}$).

Table 17. DDR1 SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with Dn_GV_{DD} of $2.5 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MVREFn_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MVREFn_{REF} + 0.31$	—	V	—

Table 18 provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 18. DDR1 and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with Dn_GV_{DD} of $(1.8\text{ or }2.5\text{ V}) \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
	266 MHz	–750	750		
	200 MHz	–1250	1250		

Notes:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

Figure 5 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

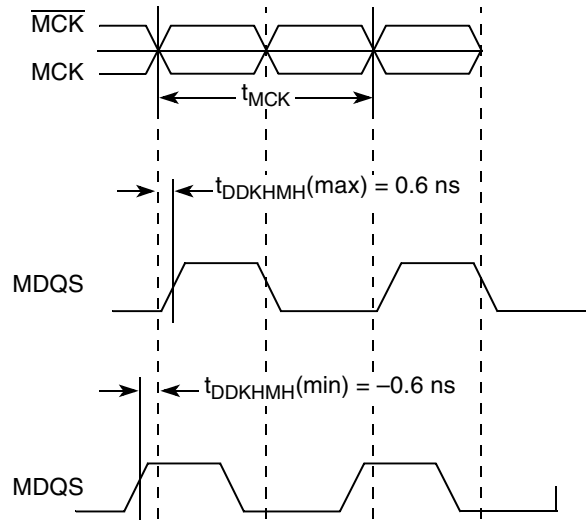


Figure 5. Timing Diagram for t_{DDKHMH}

Figure 6 shows the DDR1 and DDR2 SDRAM output timing diagram.

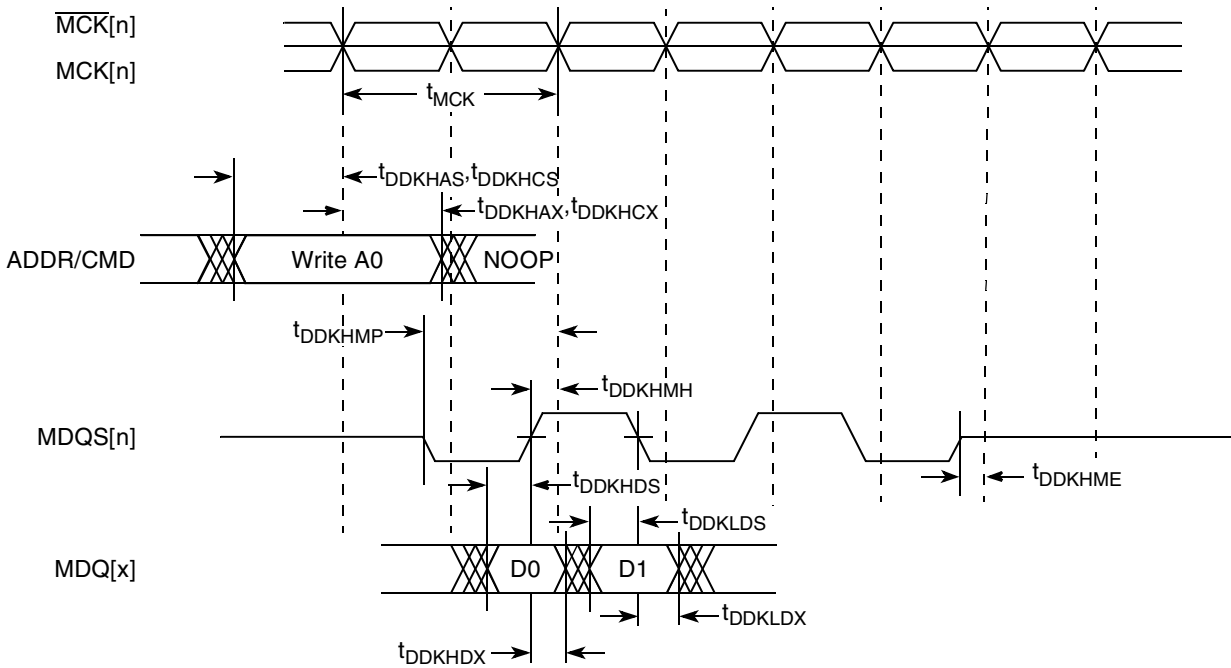


Figure 6. DDR1 and DDR2 SDRAM Output Timing Diagram

Table 23. MII Transmit AC Timing Specifications (continued)

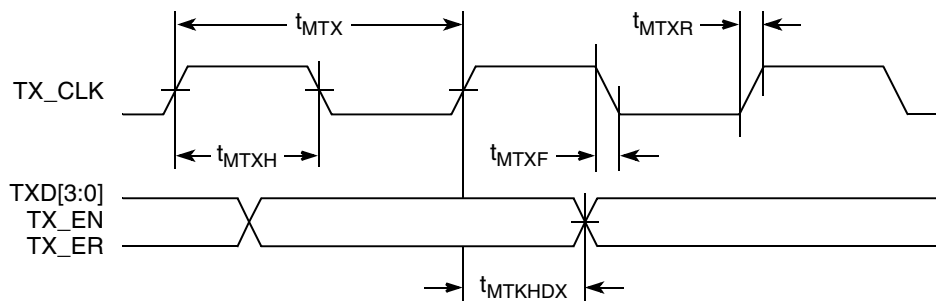
 At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
TX_CLK data clock fall time	t_{MTXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 7 shows the MII transmit AC timing diagram.


Figure 7. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

 At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time	t_{MRXR}	1.0	—	4.0	ns

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
RX_CLK clock fall time	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

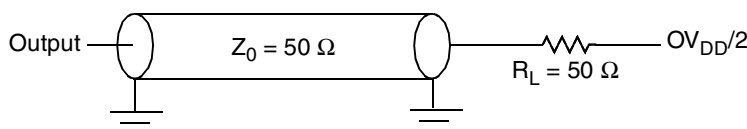


Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

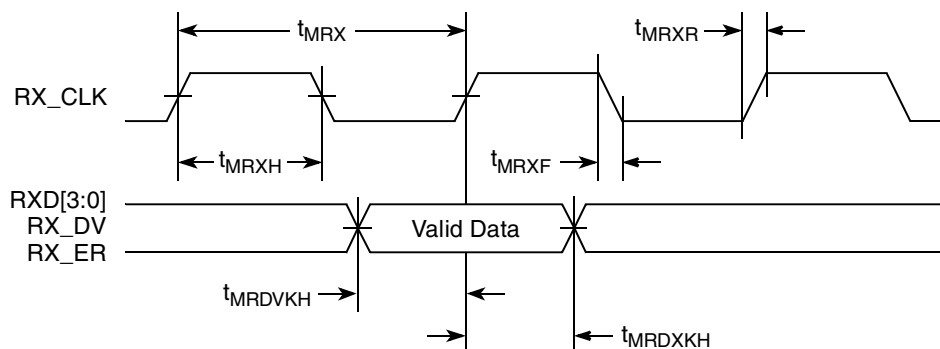


Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMI Transmit AC Timing Specifications

Table 23 provides the RMI transmit AC timing specifications.

Table 25. RMI Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMI data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{RMXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMI transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMI(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the RMI transmit AC timing diagram.

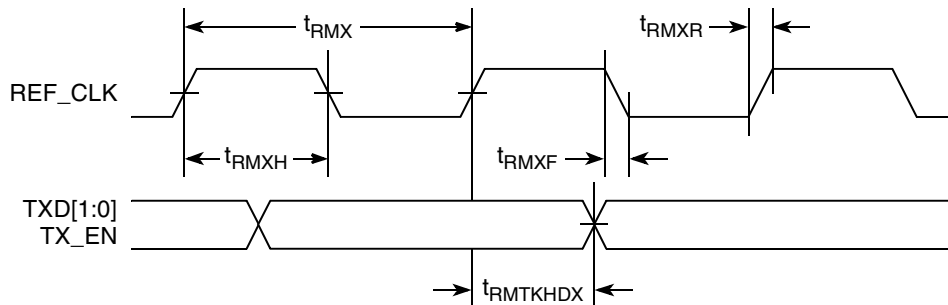


Figure 10. RMI Transmit AC Timing Diagram

8.2.2.2 RMI Receive AC Timing Specifications

Table 24 provides the RMI receive AC timing specifications.

Table 26. RMI Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{RMXR}	1.0	—	4.0	ns

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 27](#).

Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—	2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$ $OV_{DD} = \text{Min}$	2.10	$OV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$ $OV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	2.00	—	V
Input low voltage	V_{IL}	—	—	0.80	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

8.3.2 MII Management AC Electrical Specifications

[Table 28](#) provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDVVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDXVKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDVVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

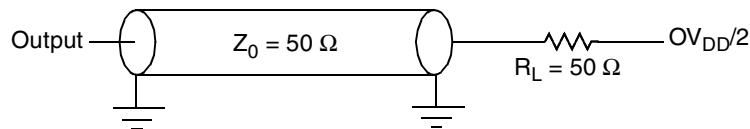
Table 30. Local Bus General Timing Parameters (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock (LCLK n) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK n) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8
Local bus clock (LCLK n) duty cycle	t_{LBDC}	47	53	%	—
Local bus clock (LCLK n) jitter specification	t_{LBRJ}	—	400	ps	—
Delay between the input clock (PCI_SYNC_IN) of local bus output clock (LCLK n)	t_{LBCDL}	—	1.7	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
- All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
- All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
- Input timings are measured at the pin.
- $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
- For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 14 provides the AC test load for the local bus.


Figure 14. Local Bus C Test Load

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

Table 33. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t_{I2KLV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0\text{ V} \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 5	μA	4

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I²C interface of the MPC8323E.

Table 34. I²C AC Electrical Specifications

All values refer to $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ levels (see Table 33).

Parameter	Symbol ¹	Min	Max	Unit	
SCL clock frequency	f_{I2C}	0	400	kHz	
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	
High period of the SCL clock	t_{I2CH}	0.6	—	μs	
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	
Data setup time	t_{I2DVKH}	100	—	ns	
Data hold time:	CBUS compatible masters I ² C bus devices	t_{I2DXKL}	— 0^2	— 0.9^3	μs

Table 37 shows the PCI AC timing specifications at 33 MHz.

Table 37. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 25 provides the AC test load for PCI.

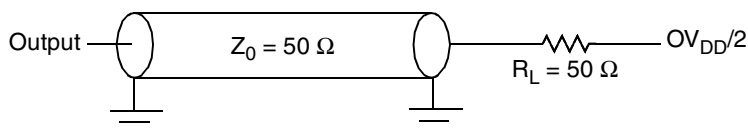


Figure 25. PCI AC Test Load

Figure 26 shows the PCI input AC timing conditions.

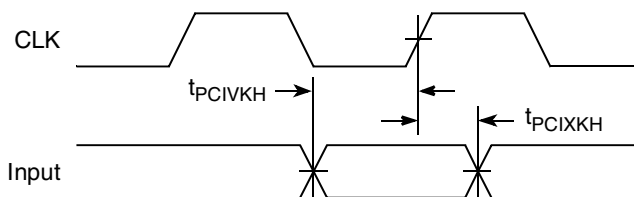


Figure 26. PCI Input AC Timing Measurement Conditions

21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

Table 55. MPC8323E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	AE9	IO	GV _{DD}	—
MEMC_MDQ1	AD10	IO	GV _{DD}	—
MEMC_MDQ2	AF10	IO	GV _{DD}	—
MEMC_MDQ3	AF9	IO	GV _{DD}	—
MEMC_MDQ4	AF7	IO	GV _{DD}	—
MEMC_MDQ5	AE10	IO	GV _{DD}	—
MEMC_MDQ6	AD9	IO	GV _{DD}	—
MEMC_MDQ7	AF8	IO	GV _{DD}	—
MEMC_MDQ8	AE6	IO	GV _{DD}	—
MEMC_MDQ9	AD7	IO	GV _{DD}	—
MEMC_MDQ10	AF6	IO	GV _{DD}	—
MEMC_MDQ11	AC7	IO	GV _{DD}	—
MEMC_MDQ12	AD8	IO	GV _{DD}	—
MEMC_MDQ13	AE7	IO	GV _{DD}	—
MEMC_MDQ14	AD6	IO	GV _{DD}	—
MEMC_MDQ15	AF5	IO	GV _{DD}	—
MEMC_MDQ16	AD18	IO	GV _{DD}	—
MEMC_MDQ17	AE19	IO	GV _{DD}	—
MEMC_MDQ18	AF17	IO	GV _{DD}	—
MEMC_MDQ19	AF19	IO	GV _{DD}	—
MEMC_MDQ20	AF18	IO	GV _{DD}	—
MEMC_MDQ21	AE18	IO	GV _{DD}	—
MEMC_MDQ22	AF20	IO	GV _{DD}	—
MEMC_MDQ23	AD19	IO	GV _{DD}	—
MEMC_MDQ24	AD21	IO	GV _{DD}	—
MEMC_MDQ25	AF22	IO	GV _{DD}	—
MEMC_MDQ26	AC21	IO	GV _{DD}	—
MEMC_MDQ27	AF21	IO	GV _{DD}	—
MEMC_MDQ28	AE21	IO	GV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE/GPIO				
GPIO_PA0/SER1_TXD[0]/TDMA_TXD[0]/USBTXN	G3	IO	OV _{DD}	—
GPIO_PA1/SER1_TXD[1]/TDMA_TXD[1]/USBTXP	F3	IO	OV _{DD}	—
GPIO_PA2/SER1_TXD[2]/TDMA_TXD[2]	F2	IO	OV _{DD}	—
GPIO_PA3/SER1_TXD[3]/TDMA_TXD[3]	E3	IO	OV _{DD}	—
GPIO_PA4/SER1_RXD[0]/TDMA_RXD[0]/USBRXP	E2	IO	OV _{DD}	—
GPIO_PA5/SER1_RXD[1]/TDMA_RXD[1]/USBRXN	E1	IO	OV _{DD}	—
GPIO_PA6/SER1_RXD[2]/TDMA_RXD[2]/USBRXD	D3	IO	OV _{DD}	—
GPIO_PA7/SER1_RXD[3]/TDMA_RXD[3]	D2	IO	OV _{DD}	—
GPIO_PA8/SER1_CD/TDMA_REQ/USBOE	D1	IO	OV _{DD}	—
GPIO_PA9 TDMA_CLKO	C3	IO	OV _{DD}	—
GPIO_PA10/SER1_CTS/TDMA_RSYNC	C2	IO	OV _{DD}	—
GPIO_PA11/TDMA_STROBE	C1	IO	OV _{DD}	—
GPIO_PA12/SER1_RTS/TDMA_TSYNC	B1	IO	OV _{DD}	—
GPIO_PA13/CLK9/BRGO9	H4	IO	OV _{DD}	—
GPIO_PA14/CLK11/BRGO10	G4	IO	OV _{DD}	—
GPIO_PA15/BRGO7	J4	IO	OV _{DD}	—
GPIO_PA16/ LA0 (LBIU)	K24	IO	OV _{DD}	—
GPIO_PA17/ LA1 (LBIU)	K26	IO	OV _{DD}	—
GPIO_PA18/Enet2_TXD[0]/SER2_TXD[0]/ TDMB_TXD[0]/LA2 (LBIU)	G25	IO	OV _{DD}	—
GPIO_PA19/Enet2_TXD[1]/SER2_TXD[1]/ TDMB_TXD[1]/LA3 (LBIU)	G26	IO	OV _{DD}	—
GPIO_PA20/Enet2_TXD[2]/SER2_TXD[2]/ TDMB_TXD[2]/LA4 (LBIU)	H25	IO	OV _{DD}	—
GPIO_PA21/Enet2_TXD[3]/SER2_TXD[3]/ TDMB_TXD[3]/LA5 (LBIU)	H26	IO	OV _{DD}	—
GPIO_PA22/Enet2_RXD[0]/SER2_RXD[0]/ TDMB_RXD[0]/LA6 (LBIU)	C25	IO	OV _{DD}	—
GPIO_PA23/Enet2_RXD[1]/SER2_RXD[1]/ TDMB_RXD[1]/LA7 (LBIU)	C26	IO	OV _{DD}	—
GPIO_PA24/Enet2_RXD[2]/SER2_RXD[2]/ TDMB_RXD[2]/LA8 (LBIU)	D25	IO	OV _{DD}	—
GPIO_PA25/Enet2_RXD[3]/SER2_RXD[3]/ TDMB_RXD[3]/LA9 (LBIU)	D26	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PC10/UPC1_RxDATA[2]/SER5_RXD[2]	B21	IO	OV _{DD}	—
GPIO_PC11/UPC1_RxDATA[3]/SER5_RXD[3]	A20	IO	OV _{DD}	—
GPIO_PC12/UPC1_RxDATA[4]	D19	IO	OV _{DD}	—
GPIO_PC13/UPC1_RxDATA[5]/LSRCID0	C18	IO	OV _{DD}	—
GPIO_PC14/UPC1_RxDATA[6]/LSRCID1	D18	IO	OV _{DD}	—
GPIO_PC15/UPC1_RxDATA[7]/LSRCID2	A25	IO	OV _{DD}	—
GPIO_PC16/UPC1_TxADDR[0]	C21	IO	OV _{DD}	—
GPIO_PC17/UPC1_TxADDR[1]/LSRCID3	D22	IO	OV _{DD}	—
GPIO_PC18/UPC1_TxADDR[2]/LSRCID4	C23	IO	OV _{DD}	—
GPIO_PC19/UPC1_TxADDR[3]/LDVAL	D23	IO	OV _{DD}	—
GPIO_PC20/UPC1_RxADDR[0]	C17	IO	OV _{DD}	—
GPIO_PC21/UPC1_RxADDR[1]	D17	IO	OV _{DD}	—
GPIO_PC22/UPC1_RxADDR[2]	C16	IO	OV _{DD}	—
GPIO_PC23/UPC1_RxADDR[3]	D16	IO	OV _{DD}	—
GPIO_PC24/UPC1_RxSOC/SER5_CD	A16	IO	OV _{DD}	—
GPIO_PC25/UPC1_RxCLAV	D20	IO	OV _{DD}	—
GPIO_PC26/UPC1_RxPRTY/CE_EXT_REQ2	E23	IO	OV _{DD}	—
GPIO_PC27/UPC1_RxEN	B17	IO	OV _{DD}	—
GPIO_PC28/UPC1_TxSOC	B22	IO	OV _{DD}	—
GPIO_PC29/UPC1_TxCLAV/SER5_CTS	A17	IO	OV _{DD}	—
GPIO_PC30/UPC1_TxPRTY	A22	IO	OV _{DD}	—
GPIO_PC31/UPC1_TxEN/SER5_RTS	C20	IO	OV _{DD}	—
GPIO_PD0/SPIMOSI	A2	IO	OV _{DD}	—
GPIO_PD1/SPIMISO	B2	IO	OV _{DD}	—
GPIO_PD2/SPICLK	B3	IO	OV _{DD}	—
GPIO_PD3/SPISEL	A3	IO	OV _{DD}	—
GPIO_PD4/SPI_MDIO/CE_MUX_MDIO	A4	IO	OV _{DD}	—
GPIO_PD5/SPI_MDC/CE_MUX_MDC	B4	IO	OV _{DD}	—
GPIO_PD6/CLK8/BRGO16/CE_EXT_REQ3	F24	IO	OV _{DD}	—
GPIO_PD7/GTM1_TIN1/GTM2_TIN2/CLK5	G24	IO	OV _{DD}	—
GPIO_PD8/GTM1_TGATE1/GTM2_TGATE2/CLK6	H24	IO	OV _{DD}	—
GPIO_PD9/GTM1_TOUT1	D24	IO	OV _{DD}	—

22.1 Clocking in PCI Host Mode

When the MPC8323E is configured as a PCI host device ($RCWH[PCIHOST] = 1$), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider ($\div 2$) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexors. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

22.1.1 PCI Clock Outputs (PCI_CLK_OUT[0:2])

When the MPC8323E is configured as a PCI host, it provides three separate clock output signals, PCI_CLK_OUT[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOEn] bit. All output clocks are phase-aligned to each other.

22.2 Clocking in PCI Agent Mode

When the MPC8323E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND, and the clock output signals, PCI_CLK_OUT $_n$ and PCI_SYNC_OUT, are not used.

22.3 System Clock Domains

As shown in [Figure 43](#), the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*ce_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lb_clk*)

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = [PCI_SYNC_IN \times (1 + \sim\overline{CFG_CLKIN_DIV})] \times SPMF$$

In PCI host mode, $PCI_SYNC_IN \times (1 + \sim\overline{CFG_CLKIN_DIV})$ is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300c2 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See the “Reset Configuration” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 59. CSB Frequency Options

CFG_CLKIN_DIV_B at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	Input Clock Frequency (MHz) ²		
			25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)		
High	0010	2 : 1			133
High	0011	3 : 1		100	
High	0100	4 : 1	100	133	
High	0101	5 : 1	125		
High	0110	6 : 1			
High	0111	7 : 1			
High	1000	8 : 1			
High	1001	9 : 1			
High	1010	10 : 1			
High	1011	11 : 1			
High	1100	12 : 1			
High	1101	13 : 1			
High	1110	14 : 1			
High	1111	15 : 1			
High	0000	16 : 1			
Low	0010	2 : 1			133
Low	0011	3 : 1		100	
Low	0100	4 : 1		133	
Low	0101	5 : 1			
Low	0110	6 : 1			
Low	0111	7 : 1			
Low	1000	8 : 1			
Low	1001	9 : 1			
Low	1010	10 : 1			
Low	1011	11 : 1			
Low	1100	12 : 1			
Low	1101	13 : 1			
Low	1110	14 : 1			
Low	1111	15 : 1			
Low	0000	16 : 1			

¹ CFG_CLKIN_DIV_B is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV_B must be pulled up (high) in agent mode.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Thermal

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
 80 Commercial St.
 Concord, NH 03301
 Internet: www.aavidthermalloy.com

Alpha Novatech 408-567-8082
 473 Sapena Ct. #12
 Santa Clara, CA 95054
 Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
 413 North Moss St.
 Burbank, CA 91502
 Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
 Loroco Sites
 671 East Brokaw Road
 San Jose, CA 95112
 Internet: www.mei-thermal.com

Tyco Electronics 800-522-2800
 Chip Coolers™
 P.O. Box 3668
 Harrisburg, PA 17105-3668
 Internet: www.chipcoolers.com

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 44 shows the PLL power supply filter circuit.

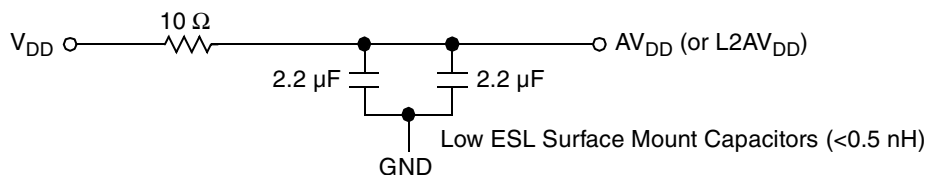


Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8323E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8323E system, and the MPC8323E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , and GV_{DD} pins of the MPC8323E. These decoupling capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , OV_{DD} , and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , or GV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , OV_{DD} , and GND pins of the MPC8323E.

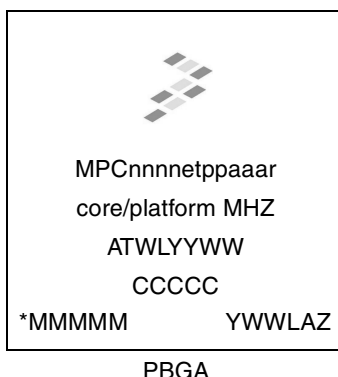
24.5 Output Buffer DC Impedance

The MPC8323E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The

25.2 Part Marking

Parts are marked as in the example shown in [Figure 46](#).



Notes:

- ATWLYYWW is the traceability code.
- CCCCC is the country code.
- MMMMM is the mask number.
- YWWLAZ is the assembly traceability code.

Figure 46. Freescale Part Marking for PBGA Devices

26 Document Revision History

[Table 67](#) provides a revision history for this hardware specification.

Table 67. Document Revision History

Rev. No.	Date	Substantive Change(s)
4	09/2010	<ul style="list-style-type: none"> • Replaced all instances of “LCCR” with “LCRR” throughout. • Added footnotes 3 and 4 in Table 2, “Recommended Operating Conditions³.” • Modified Section 8.1.1, “DC Electrical Characteristics.” • Modified Table 23, “MII Transmit AC Timing Specifications.” • Modified Table 24, “MII Receive AC Timing Specifications.” • Added footnote 7 and 8, and modified some signal names in Table 55, “MPC8323E PBGA Pinout Listing.”
3	12/2009	<ul style="list-style-type: none"> • Removed references for note 4 from Table 1. • Added Figure 2 in Section 2.1.2, “Power Supply Voltage Specification. • Added symbol T_A in Table 2. • Added footnote 2 in Table 2. • Added a note in Section 4, “Clock Input Timing for rise/fall time of QE input pins. • Modified CLKIN, PCI_CLK rise/fall time parameters in Table 8. Modified min value of t_{MCK} in Table 19. • Modified Figure 43. • Modified formula for ce_clk calculation in Section 22.3, “System Clock Domains. • Added a note in Section 22.4, “System PLL Configuration. • Removed the signal ECID_TMODE_IN from Table 55. • Removed all references of RST signals from Table 55.