



#### Welcome to E-XFL.COM

#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8321ezqaddc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



### 1.1.2 Serial Interfaces

The MPC8323E serial interfaces are as follows:

- Support for one UL2 interface with 31 multi-PHY addresses (MPC8323E and MPC8323 only)
- Support for up to three 10/100 Mbps Ethernet interfaces using MII or RMII
- Support for up to four T1/E1/J1/E3 or DS-3 serial interfaces (TDM)
- Support for dual UART and SPI interfaces and a single I<sup>2</sup>C interface

# 1.2 QUICC Engine Block

The QUICC Engine block is a versatile communications complex that integrates several communications peripheral controllers. It provides on-chip system design for a variety of applications, particularly in communications and networking systems. The QUICC Engine block has the following features:

- One 32-bit RISC controller for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
  - 10/100 Mbps Ethernet/IEEE 802.3® standard
  - IP support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
  - ATM protocol through UTOPIA interface (note that the MPC8321 and MPC8321E do not support the UTOPIA interface)
  - HDLC /transparent up to 70-Mbps full-duplex
  - HDLC bus up to 10 Mbps
  - Asynchronous HDLC
  - UART
  - BISYNC up to 2 Mbps
  - QUICC multi-channel controller (QMC) for 64 TDM channels
- One UTOPIA interface (UPC1) supporting 31 multi-PHYs (MPC8323E- and MPC8323-specific)
- Two serial peripheral interfaces (SPI). SPI2 is dedicated to Ethernet PHY management.
- Four TDM interfaces
- Thirteen independent baud rate generators and 19 input clock pins for supplying clocks to UCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

The UCCs are similar to the PowerQUICC II peripherals: SCC (BISYNC, UART, and HDLC bus) and FCC (fast Ethernet, HDLC, transparent, and ATM).





### 2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8323E. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V <sub>DD</sub>	1.0 V ± 50 mV	V	1
PLL supply voltage	AV <sub>DD</sub>	1.0 V ± 50 mV	V	1
DDR1 and DDR2 DRAM I/O voltage	GV <sub>DD</sub>	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
PCI, local bus, DUART, system control and power management, I <sup>2</sup> C, SPI, and JTAG I/O voltage	OV <sub>DD</sub>	3.3 V ± 300 mV	V	1
Junction temperature	T <sub>A</sub> /T <sub>J</sub>	0 to 105	°C	2

### Table 2. Recommended Operating Conditions<sup>3</sup>

Note:

1. GV<sub>DD</sub>, OV<sub>DD</sub>, AV<sub>DD</sub>, and V<sub>DD</sub> must track each other and must vary in the same direction—either in the positive or negative direction.

2. Minimum temperature is specified with T<sub>A</sub>; maximum temperature is specified with T<sub>J</sub>.

3. All IO pins should be interfaced with peripherals operating at same voltage level.

4. This voltage is the input to the filter discussed in Section 24.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced due to voltage drop across the filter.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8323E



Figure 2. Overshoot/Undershoot Voltage for GV<sub>DD</sub>/OV<sub>DD</sub>



Electrical Characteristics

### 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV <sub>DD</sub> = 3.3 V
PCI signals	25	
DDR1 signal	18	GV <sub>DD</sub> = 2.5 V
DDR2 signal	18	GV <sub>DD</sub> = 1.8 V
DUART, system control, I2C, SPI, JTAG	42	OV <sub>DD</sub> = 3.3 V
GPIO signals	42	OV <sub>DD</sub> = 3.3 V

Table 3. Output Drive Capability

### 2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

**Table 4. Input Capacitance Specification** 

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input capacitance for all pins except CLKIN	CI	6	8	pF	_
Input capacitance for CLKIN	C <sub>ICLKIN</sub>	10		pF	1

Note:

1. The external clock generator should be able to drive 10 pF.

## 2.2 Power Sequencing

The device does not require the core supply voltage  $(V_{DD})$  and IO supply voltages  $(GV_{DD})$  and  $OV_{DD})$  to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage  $(V_{DD})$  before the I/O voltage  $(GV_{DD})$  and  $OV_{DD}$  and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies  $(GV_{DD})$  and  $OV_{DD}$  do not have any ordering requirements with respect to one another.



CLKIN input current	$0 \ V \leq V_{IN} \leq OV_{DD}$	I <sub>IN</sub>	_	±5	μA
PCI_SYNC_IN input current	$\begin{array}{c} 0 \ V \leq V_{IN} \leq 0.5 \ V \ or \\ OV_{DD} - 0.5 \ V \leq V_{IN} \leq OV_{DD} \end{array}$	I <sub>IN</sub>	_	±5	μA
PCI_SYNC_IN input current	$0.5~V \leq V_{IN} \leq OV_{DD} - 0.5~V$	I <sub>IN</sub>	—	±50	μA

### 4.2 AC Electrical Characteristics

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI\_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 8 provides the clock input (CLKIN/PCI\_CLK) AC timing specifications for the MPC8323E.

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
CLKIN/PCI_CLK frequency	f <sub>CLKIN</sub>	25	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t <sub>CLKIN</sub>	15	—	—	ns	—
CLKIN rise and fall time	t <sub>KH</sub> , t <sub>KL</sub>	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t <sub>PCH</sub> , t <sub>PCL</sub>	0.6	0.8	1.2	ns	2
CLKIN/PCI_CLK duty cycle	t <sub>KHK</sub> /t <sub>CLKIN</sub>	40	—	60	%	3
CLKIN/PCI_CLK jitter		—	—	±150	ps	4, 5

**Table 8. CLKIN AC Timing Specifications** 

Notes:

1. **Caution:** The system, core, security, and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.

2. Rise and fall times for CLKIN/PCI\_CLK are measured at 0.4 and 2.7 V.

3. Timing is guaranteed by design and characterization.

4. This represents the total input jitter—short term and long term—and is guaranteed by design.

5. The CLKIN/PCI\_CLK driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

# 5 **RESET Initialization**

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8323E. Table 9 provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET Initialization Timir	g Specifications
-------------------------------------	------------------

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overrightarrow{\text{HRESET}}$ or $\overrightarrow{\text{SRESET}}$ (input) to activate reset flow	32	_	t <sub>PCI_SYNC_IN</sub>	1
Required assertion time of $\overrightarrow{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8323E is in PCI host mode	32		t <sub>CLKIN</sub>	2
Required assertion time of PORESET with stable clock applied to PCI_SYNC_IN when the MPC8323E is in PCI agent mode	32	_	<sup>t</sup> PCI_SYNC_IN	1



Parameter/Condition	Min	Max	Unit	Notes
HRESET/SRESET assertion (output)	512	_	t <sub>PCI_SYNC_IN</sub>	1
HRESET negation to SRESET negation (output)	16		t <sub>PCI_SYNC_IN</sub>	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8323E is in PCI host mode	4	_	<sup>t</sup> CLKIN	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8323E is in PCI agent mode	4	_	<sup>t</sup> PCI_SYNC_IN	1
Input hold time for POR config signals with respect to negation of HRESET	0	_	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of $\overrightarrow{\text{HRESET}}$	_	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of HRESET	1	_	<sup>t</sup> PCI_SYNC_IN	1, 3

### Table 9. RESET Initialization Timing Specifications (continued)

### Notes:

1. t<sub>PCI\_SYNC\_IN</sub> is the clock period of the input clock applied to PCI\_SYNC\_IN. When the MPC8323E is In PCI host mode the primary clock is applied to the CLKIN input, and PCI\_SYNC\_IN period depends on the value of CFG\_CLKIN\_DIV. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.

 t<sub>CLKIN</sub> is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual for more details.

3. POR configuration signals consists of CFG\_RESET\_SOURCE[0:2] and CFG\_CLKIN\_DIV.

### Table 10 provides the PLL lock times.

### Table 10. PLL Lock Times

Parameter/Condition	Min	Мах	Unit	Notes
PLL lock times		100	μs	_

### 5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -6.0 mA	2.4	—	V	1
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 6.0 mA	—	0.5	V	1
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	0.4	V	1
Input high voltage	V <sub>IH</sub>	—	2.0	OV <sub>DD</sub> + 0.3	V	1
Input low voltage	V <sub>IL</sub>	_	-0.3	0.8	V	_



#### **Ethernet and MII Management**

#### Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with  $\text{OV}_{\text{DD}}$  of 3.3 V  $\pm$  10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typical	Мах	Unit
RX_CLK clock fall time	t <sub>MRXF</sub>	1.0	_	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>MRDVKH</sub> symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>MRX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>MRDXKL</sub> symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>MRX</sub> clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>MRX</sub> represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>

Figure 8 provides the AC test load.



Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.



Figure 9. MII Receive AC Timing Diagram

### 8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.



# 12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8323E.

### **12.1 PCI DC Electrical Characteristics**

Table 35 provides the DC electrical characteristics for the PCI interface of the MPC8323E.

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V <sub>IH</sub>	$V_{OUT} \ge V_{OH}$ (min) or	2	OV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	$V_{OUT} \le V_{OL}$ (max)	-0.3	0.8	V
High-level output voltage	V <sub>OH</sub>	OV <sub>DD</sub> = min, I <sub>OH</sub> = −100 μA	OV <sub>DD</sub> – 0.2	_	V
Low-level output voltage	V <sub>OL</sub>	OV <sub>DD</sub> = min, I <sub>OL</sub> = 100 μA	_	0.2	V
Input current	I <sub>IN</sub>	$0 V \le V_{IN} \le OV_{DD}$	_	±5	μA

### Table 35. PCI DC Electrical Characteristics<sup>1,2</sup>

### Notes:

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1 and Table 2.

2. Ranges listed do not meet the full range of the DC specifications of the PCI 2.3 Local Bus Specifications.

# 12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8323E. Note that the PCI\_CLK or PCI\_SYNC\_IN signal is used as the PCI input clock depending on whether the MPC8323E is configured as a host or agent device. Table 36 shows the PCI AC timing specifications at 66 MHz.

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Clock to output valid	t <sub>PCKHOV</sub>	_	6.0	ns	2
Output hold from clock	t <sub>PCKHOX</sub>	1	_	ns	2
Clock to output high impedence	t <sub>PCKHOZ</sub>	_	14	ns	2, 3
Input setup to clock	t <sub>PCIVKH</sub>	3.0	_	ns	2, 4
Input hold from clock	t <sub>PCIXKH</sub>	0	—	ns	2, 4

### Table 36. PCI AC Timing Specifications at 66 MHz

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>PCIVKH</sub> symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI\_SYNC\_IN clock, t<sub>SYS</sub>, reference (K) going to the high (H) state or setup time. Also, t<sub>PCRHFV</sub> symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>

- 2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.



Figure 29 provides the AC test load for the GPIO.



# 15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8323E.

### **15.1 IPIC DC Electrical Characteristics**

Table 42 provides the DC electrical characteristics for the external interrupt pins of the MPC8323E.

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V <sub>IH</sub>	—	2.0	OV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	-0.3	0.8	V
Input current	I <sub>IN</sub>	—	—	±5	μA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 6.0 mA	—	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	0.4	V

Table 42. IPIC DC Electrical Characteristics<sup>1,2</sup>

#### Notes:

1. This table applies for pins IRQ[0:7], IRQ\_OUT, MCP\_OUT, and CE ports Interrupts.

2. IRQ\_OUT and MCP\_OUT are open drain pins, thus V<sub>OH</sub> is not relevant for those pins.

## 15.2 IPIC AC Timing Specifications

Table 43 provides the IPIC input and output AC timing specifications.

### Table 43. IPIC Input AC Timing Specifications<sup>1</sup>

Characteristic	Symbol <sup>2</sup>	Min	Unit
IPIC inputs—minimum pulse width	t <sub>PIWID</sub>	20	ns

### Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any
external synchronous logic. IPIC inputs are required to be valid for at least t<sub>PIWID</sub> ns to ensure proper operation when working
in edge triggered mode.



Figure 31 and Figure 32 represent the AC timing from Table 45. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 31 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

### Figure 31. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 32 shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 32. SPI AC Timing in Master Mode (Internal Clock) Diagram

# 17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8323E.

## 17.1 TDM/SI DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the MPC8323E TDM/SI.

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	_	0.5	V
Input high voltage	V <sub>IH</sub>	—	2.0	OV <sub>DD</sub> + 0.3	V

### Table 46. TDM/SI DC Electrical Characteristics



USB

# 20 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8323E.

# 20.1 USB DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the USB interface.

### Table 53. USB DC Electrical Characteristics<sup>1</sup>

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V <sub>IH</sub>	2	OV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \ \mu A$	V <sub>OH</sub>	OV <sub>DD</sub> – 0.2	—	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V <sub>OL</sub>	—	0.2	V
Input current	I <sub>IN</sub>	—	±5	μA

### Note:

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1 and Table 2.

# 20.2 USB AC Electrical Specifications

Table 54 describes the general timing parameters of the USB interface of the MPC8323E.

Table 54. 03D General Tilling Parameters	Table 54.	USB	General	Timing	Parameters
--	-----------	-----	---------	--------	------------

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
USB clock cycle time	t <sub>USCK</sub>	20.83	—	ns	Full speed 48 MHz
USB clock cycle time	t <sub>USCK</sub>	166.67	—	ns	Low speed 6 MHz
Skew between TXP and TXN	t <sub>USTSPN</sub>	—	5	ns	—
Skew among RXP, RXN, and RXD	t <sub>USRSPND</sub>	—	10	ns	Full speed transitions
Skew among RXP, RXN, and RXD	t <sub>USRPND</sub>	—	100	ns	Low speed transitions

### Notes:

 The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(state)(signal)</sub> for receive signals and t<sub>(first two letters of functional block)(state)(signal)</sub> for transmit signals. For example, t<sub>USRSPND</sub> symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t<sub>USTSPN</sub> symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).

2. Skew measurements are done at  $OV_{DD}/2$  of the rising or falling edge of the signals.

Figure 41 provide the AC test load for the USB.



Figure 41. USB AC Test Load



# 21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8323E is available in a thermally enhanced Plastic Ball Grid Array (PBGA); see Section 21.1, "Package Parameters for the MPC8323E PBGA," and Section 21.2, "Mechanical Dimensions of the MPC8323E PBGA," for information on the PBGA.

### 21.1 Package Parameters for the MPC8323E PBGA

The package parameters are as provided in the following list. The package type is  $27 \text{ mm} \times 27 \text{ mm}$ , 516 PBGA.

Package outline	$27 \text{ mm} \times 27 \text{ mm}$
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.6 mm

### 21.2 Mechanical Dimensions of the MPC8323E PBGA

Figure 42 shows the mechanical dimensions and bottom surface nomenclature of the MPC8323E, 516-PBGA package.



## 21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

### Table 55. MPC8323E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Men	nory Controller Interface			
MEMC_MDQ0	AE9	IO	GV <sub>DD</sub>	—
MEMC_MDQ1	AD10	IO	GV <sub>DD</sub>	—
MEMC_MDQ2	AF10	IO	GV <sub>DD</sub>	—
MEMC_MDQ3	AF9	IO	GV <sub>DD</sub>	—
MEMC_MDQ4	AF7	IO	GV <sub>DD</sub>	—
MEMC_MDQ5	AE10	IO	GV <sub>DD</sub>	—
MEMC_MDQ6	AD9	IO	GV <sub>DD</sub>	—
MEMC_MDQ7	AF8	IO	GV <sub>DD</sub>	—
MEMC_MDQ8	AE6	IO	GV <sub>DD</sub>	—
MEMC_MDQ9	AD7	IO	GV <sub>DD</sub>	—
MEMC_MDQ10	AF6	IO	GV <sub>DD</sub>	—
MEMC_MDQ11	AC7	IO	GV <sub>DD</sub>	—
MEMC_MDQ12	AD8	IO	GV <sub>DD</sub>	—
MEMC_MDQ13	AE7	IO	GV <sub>DD</sub>	—
MEMC_MDQ14	AD6	IO	GV <sub>DD</sub>	—
MEMC_MDQ15	AF5	IO	GV <sub>DD</sub>	—
MEMC_MDQ16	AD18	IO	GV <sub>DD</sub>	—
MEMC_MDQ17	AE19	IO	GV <sub>DD</sub>	—
MEMC_MDQ18	AF17	IO	GV <sub>DD</sub>	—
MEMC_MDQ19	AF19	IO	GV <sub>DD</sub>	—
MEMC_MDQ20	AF18	IO	GV <sub>DD</sub>	—
MEMC_MDQ21	AE18	IO	GV <sub>DD</sub>	—
MEMC_MDQ22	AF20	Ю	GV <sub>DD</sub>	—
MEMC_MDQ23	AD19	IO	GV <sub>DD</sub>	—
MEMC_MDQ24	AD21	IO	GV <sub>DD</sub>	—
MEMC_MDQ25	AF22	IO	GV <sub>DD</sub>	—
MEMC_MDQ26	AC21	IO	GV <sub>DD</sub>	—
MEMC_MDQ27	AF21	IO	GV <sub>DD</sub>	—
MEMC_MDQ28	AE21	IO	GV <sub>DD</sub>	



Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	0	GV <sub>DD</sub>	3
MEMC_MCK	AF14	0	GV <sub>DD</sub>	—
MEMC_MCK	AE14	0	GV <sub>DD</sub>	—
MEMC_MODT	AF11	0	GV <sub>DD</sub>	—
Local B				
LAD0	N25	IO	OV <sub>DD</sub>	7
LAD1	P26	IO	OV <sub>DD</sub>	7
LAD2	P25	IO	OV <sub>DD</sub>	7
LAD3	R26	IO	OV <sub>DD</sub>	7
LAD4	R25	IO	OV <sub>DD</sub>	7
LAD5	T26	IO	OV <sub>DD</sub>	7
LAD6	T25	IO	OV <sub>DD</sub>	7
LAD7	U25	IO	OV <sub>DD</sub>	7
LAD8	M24	IO	OV <sub>DD</sub>	7
LAD9	N24	IO	OV <sub>DD</sub>	7
LAD10	P24	IO	OV <sub>DD</sub>	7
LAD11	R24	IO	OV <sub>DD</sub>	7
LAD12	T24	IO	OV <sub>DD</sub>	7
LAD13	U24	IO	OV <sub>DD</sub>	7
LAD14	U26	IO	OV <sub>DD</sub>	7
LAD15	V26	IO	OV <sub>DD</sub>	7
LA16	K25	0	OV <sub>DD</sub>	7
LA17	L25	0	OV <sub>DD</sub>	7
LA18	L26	0	OV <sub>DD</sub>	7
LA19	L24	0	OV <sub>DD</sub>	7
LA20	M26	0	OV <sub>DD</sub>	7
LA21	M25	0	OV <sub>DD</sub>	7
LA22	N26	0	OV <sub>DD</sub>	7
LA23	AC24	0	OV <sub>DD</sub>	7
LA24	AC25	0	OV <sub>DD</sub>	7
LA25	AB23	0	OV <sub>DD</sub>	7
LCS0	AB24	0	OV <sub>DD</sub>	4

### Table 55. MPC8323E PBGA Pinout Listing (continued)



Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
LCS1	AB25	0	OV <sub>DD</sub>	4			
LCS2	AA23	0	OV <sub>DD</sub>	4			
LCS3	AA24	0	OV <sub>DD</sub>	4			
LWEO	Y23	0	OV <sub>DD</sub>	4			
LWE1	W25	0	OV <sub>DD</sub>	4			
LBCTL	V25	0	OV <sub>DD</sub>	4			
LALE	V24	0	OV <sub>DD</sub>	7			
CFG_RESET_SOURCE[0]/LSDA10/LGPL0	L23	IO	OV <sub>DD</sub>	—			
CFG_RESET_SOURCE[1]/LSDWE/LGPL1	K23	IO	OV <sub>DD</sub>	—			
LSDRAS/LGPL2/LOE	J23	0	OV <sub>DD</sub>	4			
CFG_RESET_SOURCE[2]/LSDCAS/LGPL3	H23	IO	OV <sub>DD</sub>	—			
LGPL4/LGTA/LUPWAIT/LPBSE	G23	IO	OV <sub>DD</sub>	4, 8			
LGPL5	AC22	0	OV <sub>DD</sub>	4			
LCLK0	Y24	0	OV <sub>DD</sub>	7			
LCLK1	Y25	0	OV <sub>DD</sub>	7			
	DUART			•			
UART_SOUT1/MSRCID0 (DDR ID)/LSRCID0	G1	IO	OV <sub>DD</sub>	—			
UART_SIN1/MSRCID1 (DDR ID)/LSRCID1	G2	IO	OV <sub>DD</sub>	—			
UART_CTS1/MSRCID2 (DDR ID)/LSRCID2	H3	IO	OV <sub>DD</sub>	—			
UART_RTS1/MSRCID3 (DDR ID)/LSRCID3	K3	IO	OV <sub>DD</sub>	—			
UART_SOUT2/MSRCID4 (DDR ID)/LSRCID4	H2	IO	OV <sub>DD</sub>	—			
UART_SIN2/MDVAL (DDR ID)/LDVAL	H1	IO	OV <sub>DD</sub>	—			
UART_CTS2	J3	IO	OV <sub>DD</sub>	—			
UART_RTS2	K4	IO	OV <sub>DD</sub>	—			
I <sup>2</sup> C interface							
IIC_SDA/CKSTOP_OUT	AE24	IO	OV <sub>DD</sub>	2			
IIC_SCL/CKSTOP_IN	AF24	IO	OV <sub>DD</sub>	2			
Programmable Interrupt Controller							
MCP_OUT	AD25	0	OV <sub>DD</sub>	—			
IRQ0/MCP_IN	AD26	I	OV <sub>DD</sub>	—			
IRQ1	K1	IO	OV <sub>DD</sub>	—			
IRQ2	K2	I	OV <sub>DD</sub>	—			

### Table 55. MPC8323E PBGA Pinout Listing (continued)



Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ3	J2	1	OV <sub>DD</sub>	—
IRQ4	J1	I	OV <sub>DD</sub>	—
IRQ5	AE26	I	OV <sub>DD</sub>	—
IRQ6/CKSTOP_OUT	AE25	IO	OV <sub>DD</sub>	—
IRQ7/CKSTOP_IN	AF25	I	OV <sub>DD</sub>	—
CFG_CLKIN_DIV	F1	I	OV <sub>DD</sub>	—
CFG_LBIU_MUX_EN	M23	I	OV <sub>DD</sub>	—
	JTAG		•	
тск	W26	I	OV <sub>DD</sub>	—
TDI	Y26	I	OV <sub>DD</sub>	4
TDO	AA26	0	OV <sub>DD</sub>	3
TMS	AB26	I	OV <sub>DD</sub>	4
TRST	AC26	I	OV <sub>DD</sub>	4
	TEST		•	
TEST_MODE	N23	I	OV <sub>DD</sub>	6
	РМС		•	
QUIESCE	T23	0	OV <sub>DD</sub>	—
	System Control			
HRESET	AC23	IO	OV <sub>DD</sub>	1
PORESET	AD23	I	OV <sub>DD</sub>	—
SRESET	AD24	IO	OV <sub>DD</sub>	2
	Clocks			
CLKIN	R3	I	OV <sub>DD</sub>	_
CLKIN	P4	0	OV <sub>DD</sub>	—
PCI_SYNC_OUT	V1	0	OV <sub>DD</sub>	3
RTC_PIT_CLOCK	U23	I	OV <sub>DD</sub>	—
PCI_SYNC_IN/PCI_CLK	V2	I	OV <sub>DD</sub>	—
PCI_CLK0/clkpd_cerisc1_ipg_clkout/DPTC_OSC	ТЗ	0	OV <sub>DD</sub>	—
PCI_CLK1/clkpd_half_cemb4ucc1_ipg_clkout/ CLOCK_XLB_CLOCK_OUT	U2	0	OV <sub>DD</sub>	—
PCI_CLK2/clkpd_third_cesog_ipg_clkout/ cecl_ipg_ce_clock	R4	0	OV <sub>DD</sub>	—

### Table 55. MPC8323E PBGA Pinout Listing (continued)



### Clocking

# 22 Clocking

Figure 43 shows the internal distribution of clocks within the MPC8323E.



### Figure 43. MPC8323E Clock Subsystem

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI\_CLK, depending on whether the device is configured in PCI host or PCI agent mode, respectively.



#### 22.7 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8323E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb\_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 63 shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

Conf No.	SPMF	Core PLL	CEMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0110	0	33.33	133.33	266.66	200
2	0100	0000101	1000	0	25	100	250	200
3	0010	0000100	0011	0	66.67	133.33	266.66	200
4	0100	0000101	0110	0	33.33	133.33	333.33	200
5	0101	0000101	1000	0	25	125	312.5	200
6	0010	0000101	0011	0	66.67	133.33	333.33	200

Table 63. Suggested PLL Configurations

#### 23 Thermal

This section describes the thermal specifications of the MPC8323E.

#### 23.1 **Thermal Characteristics**

Table 64 provides the package thermal characteristics for the 516  $27 \times 27$  mm PBGA of the MPC8323E.

Table 64. Package Thermal Characteristics for PBGA						
Characteristic	Board type	Symbol	Value	Unit	Notes	
Junction-to-ambient natural convection	Single-layer board (1s)	R <sub>θJA</sub>	28	°C/W	1, 2	
Junction-to-ambient natural convection	Four-layer board (2s2p)	R <sub>θJA</sub>	21	°C/W	1, 2, 3	
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	R <sub>0JMA</sub>	23	°C/W	1, 3	
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	R <sub>0JMA</sub>	18	°C/W	1, 3	
Junction-to-board	—	$R_{\theta J B}$	13	°C/W	4	
Junction-to-case	_	R <sub>θJC</sub>	9	°C/W	5	

. . ----



### Table 64. Package Thermal Characteristics for PBGA (continued)

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-package top	Natural convection	$\Psi_{JT}$	2	°C/W	6

Notes:

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
- 3. Per JEDEC JESD51-6 with the board horizontal.
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### 23.2 Thermal Management Information

For the following sections,  $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ , where  $P_{I/O}$  is the power dissipation of the I/O drivers.

### 23.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T<sub>J</sub>, can be obtained from the equation:

 $T_J = T_A + (R_{\theta JA} \times P_D)$ 

where:

 $T_J$  = junction temperature (°C)

 $T_A$  = ambient temperature for the package (°C)

 $R_{\theta JA}$  = junction-to-ambient thermal resistance (°C/W)

 $P_D$  = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity  $T_I - T_A$ ) are possible.

### 23.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter



#### System Design Information

interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

 $T_C$  = case temperature of the package (°C)  $R_{\theta JC}$  = junction-to-case thermal resistance (°C/W)  $P_D$  = power dissipation (W)

# 24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8323E.

### 24.1 System Clocking

The MPC8323E includes three PLLs.

- The system PLL (AV<sub>DD</sub>2) generates the system clock from the externally supplied CLKIN input. The frequency ratio between the system and CLKIN is selected using the system PLL ratio configuration bits as described in Section 22.4, "System PLL Configuration."
- The e300 core PLL (AV<sub>DD</sub>3) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in Section 22.5, "Core PLL Configuration."
- The QUICC Engine PLL (AV<sub>DD</sub>1) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

## 24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each  $AV_{DD}n$  pin should always be equivalent to  $V_{DD}$ , and preferably these voltages are derived directly from  $V_{DD}$  through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 44, one to each of the five  $AV_{DD}$  pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.



#### System Design Information

output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and  $R_P$  is trimmed until the voltage at the pad equals  $OV_{DD}/2$ .  $R_P$  then becomes the resistance of the pull-up devices.  $R_P$  and  $R_N$  are designed to be close to each other in value. Then,  $Z_0 = (R_P + R_N)/2$ .



Figure 45. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is  $V_1 = R_{source} \times I_{source}$ . Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value  $R_{term}$ . The measured voltage is  $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$ . Solving for the output impedance gives  $R_{source} = R_{term} \times (V_1/V_2 - 1)$ . The drive current is then  $I_{source} = V_1/R_{source}$ .

Table 65 summarizes the signal impedance targets. The driver impedance are targeted at minimum  $V_{DD}$ , nominal  $OV_{DD}$ , 105°C.

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R <sub>N</sub>	42 Target	25 Target	20 Target	Z <sub>0</sub>	W
R <sub>P</sub>	42 Target	25 Target	20 Target	Z <sub>0</sub>	W
Differential	NA	NA	NA	Z <sub>DIFF</sub>	W

**Table 65. Impedance Characteristics** 

Note: Nominal supply voltages. See Table 1,  $T_i = 105^{\circ}C$ .

### 24.6 Configuration Pin Multiplexing

The MPC8323E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k $\Omega$  on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.