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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	·
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8321vraddca

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTE

The QUICC Engine block can also support a UTOPIA level 2 capable of supporting 31 multi-PHY (MPC8323E- and MPC8323-specific).

The MPC8323E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In summary, the MPC8323E family provides users with a highly integrated, fully programmable communications processor. This helps ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

1.1 MPC8323E Features

Major features of the MPC8323E are as follows:

- High-performance, low-power, and cost-effective single-chip data-plane/control-plane solution for ATM or IP/Ethernet packet processing (or both).
- MPC8323E QUICC Engine block offers a future-proof solution for next generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards.
- Single platform architecture supports the convergence of IP packet networks and ATM networks.
- DDR1/DDR2 memory controller—one 32-bit interface at up to 266 MHz supporting both DDR1 and DDR2.
- An e300c2 core built on Power Architecture technology with 16-Kbyte instruction and data caches, and dual integer units.
- Peripheral interfaces such as 32-bit PCI (2.2) interface up to 66-MHz operation, 16-bit local bus interface up to 66-MHz operation, and USB 2.0 (full-/low-speed).
- Security engine provides acceleration for control and data plane security protocols.
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration.

1.1.1 Protocols

The protocols are as follows:

- ATM SAR up to 155 Mbps (OC-3) full duplex, with ATM traffic shaping (ATF TM4.1)
- Support for ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- Support for IMA and ATM transmission convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- Support for 64 channels of HDLC/transparent





2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8323E. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V _{DD}	1.0 V ± 50 mV	V	1
PLL supply voltage	AV _{DD}	1.0 V ± 50 mV	V	1
DDR1 and DDR2 DRAM I/O voltage	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
PCI, local bus, DUART, system control and power management, I ² C, SPI, and JTAG I/O voltage	OV _{DD}	3.3 V ± 300 mV	V	1
Junction temperature	T _A /T _J	0 to 105	°C	2

Table 2. Recommended Operating Conditions³

Note:

1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

2. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.

3. All IO pins should be interfaced with peripherals operating at same voltage level.

4. This voltage is the input to the filter discussed in Section 24.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced due to voltage drop across the filter.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8323E



Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}



Electrical Characteristics

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV _{DD} = 3.3 V
PCI signals	25	
DDR1 signal	18	GV _{DD} = 2.5 V
DDR2 signal	18	GV _{DD} = 1.8 V
DUART, system control, I2C, SPI, JTAG	42	OV _{DD} = 3.3 V
GPIO signals	42	OV _{DD} = 3.3 V

Table 3. Output Drive Capability

2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input capacitance for all pins except CLKIN	CI	6	8	pF	_
Input capacitance for CLKIN	C _{ICLKIN}	10		pF	1

Note:

1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and IO supply voltages (GV_{DD}) and $OV_{DD})$ to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}) and OV_{DD} and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD}) and OV_{DD} do not have any ordering requirements with respect to one another.







Figure 3. MPC8323E Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation for this family of MPC8323E devices is shown in Table 5.

CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Core Frequency (MHz)	Typical	Maximum	Unit	Notes
133	200	266	0.74	1.48	W	1, 2, 3
133	200	333	0.78	1.62	W	1, 2, 3

Notes:

1. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.

2. Typical power is based on a nominal voltage of V_{DD} = 1.0 V, ambient temperature, and the core running a Dhrystone

benchmark application. The measurements were taken on the MPC8323MDS evaluation board using WC process silicon.

3. Maximum power is based on a voltage of V_{DD} = 1.07 V, WC process, a junction T_J = 110°C, and an artificial smoke test.

Table 6 shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V $R_s = 20 \Omega$ $R_t = 50 \Omega$ 1 pair of clocks	266 MHz, 1 × 32 bits	0.212	0.367	_	W	_



DDR1 and DDR2 SDRAM

Table 13. DDR2 SDRAM Capacitance for Dn_GV_{DD}(typ) = 1.8 V

Delta input/output capacitance: DQ, DQS	C _{DIO}	-	0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25 °C, V_{OUT} = $Dn_GV_{DD} \div 2$,

V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR1 SDRAM component(s) of the MPC8323E when $Dn_GV_{DD}(typ) = 2.5 V.$

Parameter/Condition Symbol Min Max Unit Notes V I/O supply voltage 2.375 2.625 Dn_GV_{DD} 1 I/O reference voltage MVREF n_{REF} $0.49 \times Dn_GV_{DD}$ $0.51 \times Dn_GV_{DD}$ V 2 I/O termination voltage MVREF n_{REF} - 0.04 MVREFn_{REF} + 0.04 ٧ 3 VTT Input high voltage VIH MVREFn_{REF} + 0.15 $Dn_GV_{DD} + 0.3$ ٧ ٧ Input low voltage VIL -0.3 MVREFn_{REF} – 0.15 Output leakage current -9.9 loz -9.9 μΑ 4 Output high current (V_{OUT} = 1.95 V) -16.2 mΑ I_{OH} Output low current (V_{OUT} = 0.35 V) 16.2 mΑ I_{OL}

Table 14. DDR1 SDRAM DC Electrical Characteristics for Dn_GV_{DD}(typ) = 2.5 V

Notes:

1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.

2. MVREF n_{BEF} is expected to be equal to $0.5 \times Dn_{\text{GV}DD}$, and to track $Dn_{\text{GV}DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREF nREF may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREFn_{REF}. This rail should track variations in the DC level of MVREFn_{REF}.

4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le Dn_GV_{DD}$.

Table 15 provides the DDR1 capacitance $Dn_GV_{DD}(typ) = 2.5$ V.

Table 15. DDR1 SDRAM Capacitance for Dn_GV_{DD}(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ,DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}		0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$, f = 1 MHz, $T_A = 25^{\circ} \text{ C}$, $V_{OUT} = Dn_GV_{DD} \div 2$, V_{OUT} (peak-to-peak) = 0.2 V.



Ethernet and MII Management

(management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 DC Electrical Characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in Table 22.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage 3.3 V	OV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	I _{OH} = -4.0 mA	OV _{DD} = Min	2.40	OV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 4.0 mA	OV _{DD} = Min	GND	0.50	V
Input high voltage	V _{IH}	—	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	—	-0.3	0.90	V
Input current	I _{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

Table 22. MII and RMII DC Electrical Characteristics

8.2 MII and RMII AC Timing Specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Мах	Unit
TX_CLK clock period 10 Mbps	t _{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t _{MTX}	—	40	—	ns
TX_CLK duty cycle	t _{MTXH} /t _{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	^t мткнdх	1	5	15	ns
TX_CLK data clock rise time	t _{MTXR}	1.0	_	4.0	ns



8.2.2.1 RMII Transmit AC Timing Specifications

Table 23 provides the RMII transmit AC timing specifications.

Table 25. RMII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
REF_CLK clock	t _{RMX}	_	20	_	ns
REF_CLK duty cycle	t _{RMXH} /t _{RMX}	35	_	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTKHDX}	2	_	10	ns
REF_CLK data clock rise V _{IL} (min) to V _{IH} (max)	t _{RMXR}	1.0	_	4.0	ns
REF_CLK data clock fall $V_{IH}(max)$ to $V_{IL}(min)$	t _{RMXF}	1.0		4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first three letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{RMTKHDX} symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the RMII transmit AC timing diagram.



Figure 10. RMII Transmit AC Timing Diagram

8.2.2.2 RMII Receive AC Timing Specifications

Table 24 provides the RMII receive AC timing specifications.

Table 26. RMII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Мах	Unit
REF_CLK clock period	t _{RMX}	—	20	—	ns
REF_CLK duty cycle	t _{RMXH} /t _{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	t _{RMRDVKH}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	t _{RMRDXKH}	2.0	—	—	ns
REF_CLK clock rise VIL(min) to VIH(max)	t _{RMXR}	1.0	—	4.0	ns



Parameter	Symbol ¹	Min	Мах	Unit	Notes
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3	_	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	_	ns	7
Local bus clock (LCLKn) to output valid	t _{LBKHOV}	—	3	ns	3
Local bus clock (LCLKn) to output high impedance for LAD/LDP	t _{LBKHOZ}	—	4	ns	8
Local bus clock (LCLKn) duty cycle	t _{LBDC}	47	53	%	_
Local bus clock (LCLKn) jitter specification	t _{LBRJ}	—	400	ps	_
Delay between the input clock (PCI_SYNC_IN) of local bus output clock (LCLK <i>n</i>)	t _{LBCDL}	—	1.7	ns	_

Table 30. Local Bus General Timing Parameters (continued)

Notes:

The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).

2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).

All signals are measured from OV_{DD}/2 of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.

4. Input timings are measured at the pin.

5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.

 t_{LBOTOT2} should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.

7. t_{LBOTOT3} should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.

8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 14 provides the AC test load for the local bus.



Figure 14. Local Bus C Test Load



1²C

Table 34. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol ¹	Min	Мах	Unit
Rise time of both SDA and SCL signals	t _{l2CR}	20 + 0.1 C _b ⁴	300	ns
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns
Setup time for STOP condition	t _{I2PVKH}	0.6		μs
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3		μs
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	Ι	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times \text{OV}_{\text{DD}}$	_	V

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

- MPC8323E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

4. C_B = capacitance of one bus line in pF.

Figure 23 provides the AC test load for the I^2C .



Figure 23. I²C AC Test Load

Figure 24 shows the AC timing diagram for the I^2C bus.



Figure 24. I²C Bus AC Timing Diagram

HDLC, BISYNC, Transparent, and Synchronous UART

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications¹ (continued)

Characteristic	Symbol ²	Min	Мах	Unit
Inputs—External clock input hold time	t _{HEIXKH}	1	_	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).}

Table 52. Synchronous UART AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock delay	t _{UAIKHOV}	0	5.5	ns
Outputs—External clock delay	t _{UAEKHOV}	1	10	ns
Outputs—Internal clock high impedance	t _{UAIKHOX}	0	5.5	ns
Outputs—External clock high impedance	t _{UAEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t _{UAIIVKH}	6	—	ns
Inputs—External clock input setup time	t _{UAEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t _{UAIIXKH}	0	—	ns
Inputs—External clock input hold time	t _{UAEIXKH}	1	—	ns

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{UAIKHOX} symbolizes the outputs internal timing (UAI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub>

Figure 38 provides the AC test load.



Figure 38. AC Test Load

Figure 39 and Figure 40 represent the AC timing from Table 51. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8323E is available in a thermally enhanced Plastic Ball Grid Array (PBGA); see Section 21.1, "Package Parameters for the MPC8323E PBGA," and Section 21.2, "Mechanical Dimensions of the MPC8323E PBGA," for information on the PBGA.

21.1 Package Parameters for the MPC8323E PBGA

The package parameters are as provided in the following list. The package type is $27 \text{ mm} \times 27 \text{ mm}$, 516 PBGA.

Package outline	$27 \text{ mm} \times 27 \text{ mm}$
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.6 mm

21.2 Mechanical Dimensions of the MPC8323E PBGA

Figure 42 shows the mechanical dimensions and bottom surface nomenclature of the MPC8323E, 516-PBGA package.



Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PA26/Enet2_RX_ER/SER2_CD/TDMB_REQ/ LA10 (LBIU)	E26	IO	OV _{DD}	—
GPIO_PA27/Enet2_TX_ER/TDMB_CLKO/LA11 (LBIU)	F25	IO	OV _{DD}	—
GPIO_PA28/Enet2_RX_DV/SER2_CTS/ TDMB_RSYNC/LA12 (LBIU)	E25	IO	OV _{DD}	—
GPIO_PA29/Enet2_COL/RXD[4]/SER2_RXD[4]/ TDMB_STROBE/LA13 (LBIU)	J25	IO	OV _{DD}	—
GPIO_PA30/Enet2_TX_EN/SER2_RTS/ TDMB_TSYNC/LA14 (LBIU)	F26	IO	OV _{DD}	—
GPIO_PA31/Enet2_CRS/SDET LA15 (LBIU)	J26	IO	OV _{DD}	_
GPIO_PB0/Enet3_TXD[0]/SER3_TXD[0]/ TDMC_TXD[0]	A13	IO	OV _{DD}	—
GPIO_PB1/Enet3_TXD[1]/SER3_TXD[1]/ TDMC_TXD[1]	B13	IO	OV _{DD}	—
GPIO_PB2/Enet3_TXD[2]/SER3_TXD[2]/ TDMC_TXD[2]	A14	IO	OV _{DD}	—
GPIO_PB3/Enet3_TXD[3]/SER3_TXD[3]/ TDMC_TXD[3]	B14	IO	OV _{DD}	—
GPIO_PB4/Enet3_RXD[0]/SER3_RXD[0]/ TDMC_RXD[0]	B8	IO	OV _{DD}	—
GPIO_PB5/Enet3_RXD[1]/SER3_RXD[1]/ TDMC_RXD[1]	A8	IO	OV _{DD}	—
GPIO_PB6/Enet3_RXD[2]/SER3_RXD[2]/ TDMC_RXD[2]	A9	IO	OV _{DD}	—
GPIO_PB7/Enet3_RXD[3]/SER3_RXD[3]/ TDMC_RXD[3]	В9	IO	OV _{DD}	—
GPIO_PB8/Enet3_RX_ER/SER3_CD/TDMC_REQ	A11	IO	OV _{DD}	_
GPIO_PB9/Enet3_TX_ER/TDMC_CLKO	B11	IO	OV _{DD}	—
GPIO_PB10/Enet3_RX_DV/SER3_CTS/ TDMC_RSYNC	A10	IO	OV _{DD}	—
GPIO_PB11/Enet3_COL/RXD[4]/SER3_RXD[4]/ TDMC_STROBE	A15	IO	OV _{DD}	—
GPIO_PB12/Enet3_TX_EN/SER3_RTS/ TDMC_TSYNC	B12	IO	OV _{DD}	—
GPIO_PB13/Enet3_CRS/SDET	B15	IO	OV _{DD}	—
GPIO_PB14/CLK12	D9	IO	OV _{DD}	—
GPIO_PB15 UPC1_TxADDR[4]	D14	IO	OV _{DD}	_
GPIO_PB16 UPC1_RxADDR[4]	B16	IO	OV _{DD}	_

Table 55. MPC8323E PBGA Pinout Listing (continued)



Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V _{DD}	K10, K11, K12, K13, K14, K15, K16, K17, L10, L17, M10, M17, N10, N17, P10, P17, R10, R17, T10, T17, U10, U11, U12, U13, U14, U15, U16, U17	V _{DD}	_	_
V _{SS}	B23, E7, E11, E13, E17, E21, F11, F13, F17, F21, F23, G5, H22, K5, K6, L11, L12, L13, L14, L15, L16, L21, M11, M12, M13, M14, M15, M16, N6, N11, N12, N13, N14, N15, N16, P5, P11, P12, P13, P14, P15, P16, P21, R11, R12, R13, R14, R15, R16, R22, T6, T11, T12, T13, T14, T15, T16, U5, U21, V23, W5, W6, W21, W23, W24, Y22, AA5, AA6, AA22, AA25, AB7, AB13, AB19, AB22, AC10, AC12, AC16, AC20	V _{SS}		
	No Connect			
NC	C22	_	—	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.

2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.

3. This output is actively driven during reset rather than being three-stated during reset.

4. These JTAG and local bus pins have weak internal pull-up P-FETs that are always enabled.

5. This pin should have a weak pull up if the chip is in PCI host mode. Follow the PCI specification's recommendation.

6. This pin must always be tied to GND. 7. This pin has weak internal pull-down N-FET that is always enabled.8. Though this pin has weak internal pull-up yet it is recommended to apply an external pull-up.



Clocking

22 Clocking

Figure 43 shows the internal distribution of clocks within the MPC8323E.



Figure 43. MPC8323E Clock Subsystem

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode, respectively.



Clocking

shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

		csh clk:	Input Clo	ck Frequen	cy (MHz) ²
CFG_CLKIN_DIV_B at Reset ¹	SPMF	Input Clock	25	33.33	66.67
		Ratio	csb_cll	k Frequenc	y (MHz)
High	0010	2:1			133
High	0011	3:1		100	
High	0100	4 : 1	100	133	
High	0101	5:1	125		
High	0110	6:1			
High	0111	7:1			
High	1000	8:1			
High	1001	9:1			
High	1010	10 : 1			
High	1011	11 : 1			
High	1100	12 : 1			
High	1101	13 : 1			
High	1110	14 : 1			
High	1111	15 : 1			
High	0000	16 : 1			
Low	0010	2 : 1			133
Low	0011	3 : 1		100	
Low	0100	4 : 1		133	
Low	0101	5 : 1			
Low	0110	6:1			
Low	0111	7:1			
Low	1000	8:1			
Low	1001	9:1			
Low	1010	10 : 1			
Low	1011	11:1			
Low	1100	12 : 1			
Low	1101	13 : 1			
Low	1110	14 : 1			
Low	1111	15 : 1			
Low	0000	16 : 1			

Table 59. CSB Frequency Options

¹ CFG_CLKIN_DIV_B is only used for host mode; CLKIN must be tied low and

CFG_CLKIN_DIV_B must be pulled up (high) in agent mode.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.





22.5 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 60 shows the encodings for RCWL[COREPLL]. COREPLL values not listed in Table 60 should be considered reserved.

RCWL[COREPLL]		aara alku aab alk Patia	VCO Divider	
0-1	2-5	6	COTE_CIK : CSD_CIK HAIIO	VCO Divider
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷2
01	0001	1	1.5:1	÷4
10	0001	1	1.5:1	÷8
11	0001	1	1.5:1	÷8
00	0010	0	2:1	÷2
01	0010	0	2:1	÷4
10	0010	0	2:1	÷8
11	0010	0	2:1	÷8
00	0010	1	2.5:1	÷2
01	0010	1	2.5:1	÷4
10	0010	1	2.5:1	÷8
11	0010	1	2.5:1	÷8
00	0011	0	3:1	÷2
01	0011	0	3:1	÷4
10	0011	0	3:1	÷8
11	0011	0	3:1	÷8

Table 60. e300 Core PLL Configuration

NOTE

Core VCO frequency = core frequency \times VCO divider

VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 500–800 MHz.



Clocking

22.6 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. Table 61 shows the multiplication factor encodings for the QUICC Engine PLL.

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF)
00000-00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

Table 61. QUICC Engine PLL Multiplication Factors

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in Table 62.

Table 62. QUICC Engine PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

 $ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$

QUICC Engine VCO Frequency = $ce_clk \times VCO$ divider $\times (1 + CEPDF)$





Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102		
Interface material vendors include the following:			
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850		
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481		
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674		
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572		

23.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

23.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the



NP

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 44 shows the PLL power supply filter circuit.



Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8323E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8323E system, and the MPC8323E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , and GV_{DD} pins of the MPC8323E. These decoupling capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , OV_{DD} , and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , or GV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , OV_{DD} , and GND pins of the MPC8323E.

24.5 Output Buffer DC Impedance

The MPC8323E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The



Document Revision History

Table 67. Document Revision History

Rev. No.	Date	Substantive Change(s)
2	4/2008	 Removed Figures 2 and 3 overshoot and undershoot voltage specs from Section 2.1.2, "Power Supply Voltage Specification," and footnotes 4 and 5 from Table 1. Corrected QUIESCE signal to be an output signal in Table 55. Added column for GVDD (1.8 V) - DDR2 - to Table 6 with 0.212-W typical power dissipation. Added Figure 4 DDR input timing diagram. Removed CE_TRB* and CE_PIO* signals from Table 55. Added three local bus AC specifications to Table 30 (duty cycle, jitter, delay between input clock and local bus clock). Added row in Table 2 stating junction temperature range of 0 to 105•C. Modified Section 2.2, "Power Sequencing," to include PORESET requirement.
1	6/2007	Correction to descriptive text in Section 2.2.
0	6/2007	Initial release.