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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8321zqadc

1 Overview

The MPC8323E incorporates the e300c2 (MPC603e-based) core built on Power Architecture® technology, which includes 16 Kbytes of L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The e300c2 core does not contain a floating point unit (FPU). The MPC8323E also includes a 32-bit PCI controller, four DMA channels, a security engine, and a 32-bit DDR1/DDR2 memory controller.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8323E. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). Note that the MPC8321 and MPC8321E do not support UTOPIA. A block diagram of the MPC8323E is shown in Figure 1.

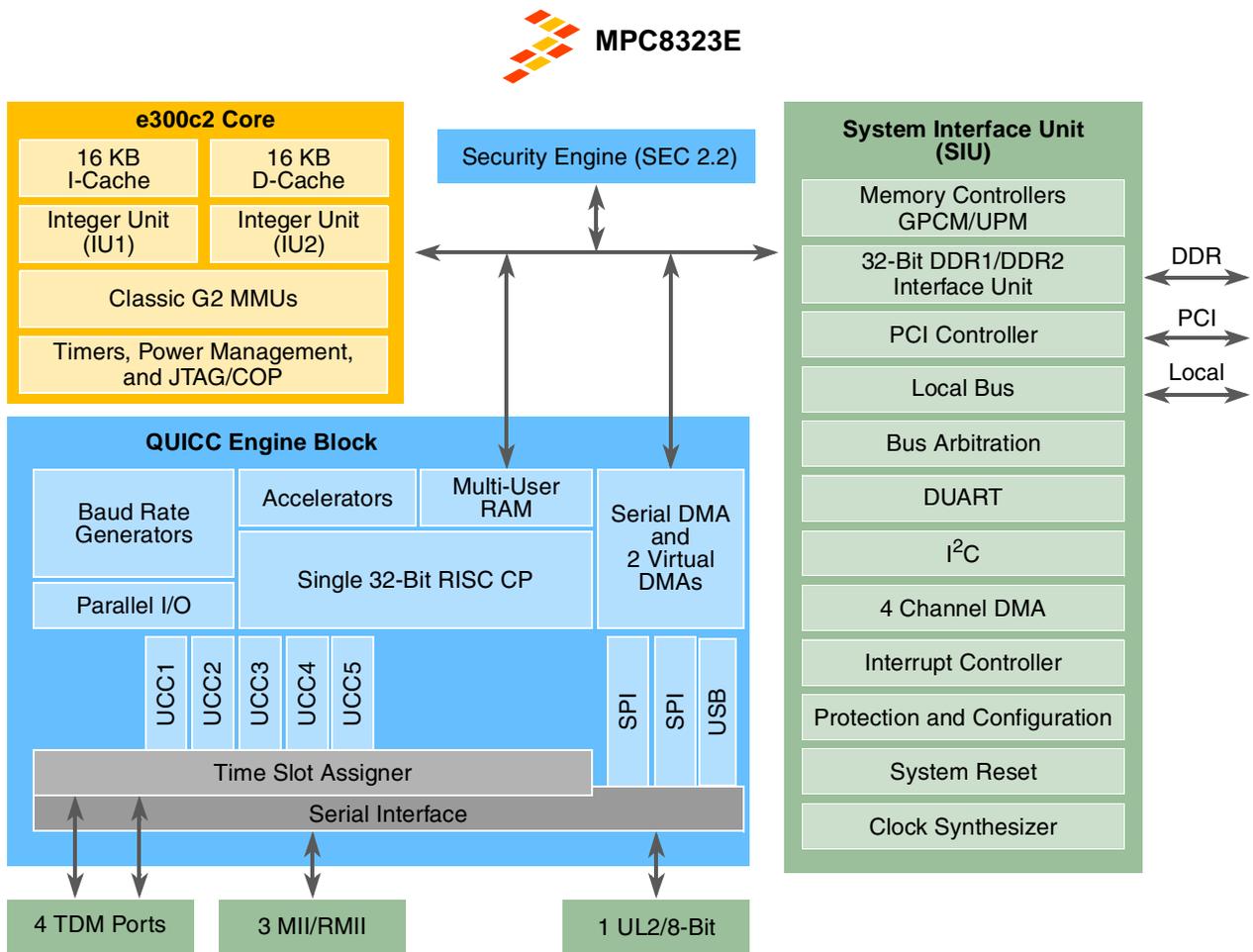


Figure 1. MPC8323E Block Diagram

Each of the five UCCs can support a variety of communication protocols: 10/100 Mbps Ethernet, serial ATM, HDLC, UART, and BISYNC—and, in the MPC8323E and MPC8323, multi-PHY ATM and ATM support for up to OC-3 speeds.

1.1.2 Serial Interfaces

The MPC8323E serial interfaces are as follows:

- Support for one UL2 interface with 31 multi-PHY addresses (MPC8323E and MPC8323 only)
- Support for up to three 10/100 Mbps Ethernet interfaces using MII or RMII
- Support for up to four T1/E1/J1/E3 or DS-3 serial interfaces (TDM)
- Support for dual UART and SPI interfaces and a single I²C interface

1.2 QUICC Engine Block

The QUICC Engine block is a versatile communications complex that integrates several communications peripheral controllers. It provides on-chip system design for a variety of applications, particularly in communications and networking systems. The QUICC Engine block has the following features:

- One 32-bit RISC controller for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
 - 10/100 Mbps Ethernet/IEEE 802.3® standard
 - IP support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
 - ATM protocol through UTOPIA interface (note that the MPC8321 and MPC8321E do not support the UTOPIA interface)
 - HDLC /transparent up to 70-Mbps full-duplex
 - HDLC bus up to 10 Mbps
 - Asynchronous HDLC
 - UART
 - BISYNC up to 2 Mbps
 - QUICC multi-channel controller (QMC) for 64 TDM channels
- One UTOPIA interface (UPC1) supporting 31 multi-PHYs (MPC8323E- and MPC8323-specific)
- Two serial peripheral interfaces (SPI). SPI2 is dedicated to Ethernet PHY management.
- Four TDM interfaces
- Thirteen independent baud rate generators and 19 input clock pins for supplying clocks to UCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

The UCCs are similar to the PowerQUICC II peripherals: SCC (BISYNC, UART, and HDLC bus) and FCC (fast Ethernet, HDLC, transparent, and ATM).

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8323E. The MPC8323E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	-0.3 to 1.26	V	—
PLL supply voltage		AV_{DDn}	-0.3 to 1.26	V	—
DDR1 and DDR2 DRAM I/O voltage		GV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	—
PCI, local bus, DUART, system control and power management, I ² C, SPI, MII, RMII, MII management, and JTAG I/O voltage		OV_{DD}	-0.3 to 3.6	V	—
Input voltage	DDR1/DDR2 DRAM signals	MV_{IN}	-0.3 to ($GV_{DD} + 0.3$)	V	2
	DDR1/DDR2 DRAM reference	MV_{REF}	-0.3 to ($GV_{DD} + 0.3$)	V	2
	Local bus, DUART, CLKIN, system control and power management, I ² C, SPI, and JTAG signals	OV_{IN}	-0.3 to ($OV_{DD} + 0.3$)	V	3
	PCI	OV_{IN}	-0.3 to ($OV_{DD} + 0.3$)	V	5
Storage temperature range		T_{STG}	-55 to 150	°C	—

Notes:

- Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	$OV_{DD} = 3.3\text{ V}$
PCI signals	25	
DDR1 signal	18	$GV_{DD} = 2.5\text{ V}$
DDR2 signal	18	$GV_{DD} = 1.8\text{ V}$
DUART, system control, I2C, SPI, JTAG	42	$OV_{DD} = 3.3\text{ V}$
GPIO signals	42	$OV_{DD} = 3.3\text{ V}$

2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input capacitance for all pins except CLKIN	C_I	6	8	pF	—
Input capacitance for CLKIN	$C_{I\text{CLKIN}}$	10	—	pF	1

Note:

1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and IO supply voltages (GV_{DD} and OV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} and OV_{DD}) and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD} and OV_{DD}) do not have any ordering requirements with respect to one another.

Table 6. Estimated Typical I/O Power Dissipation (continued)

Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 32 bits	—	—	0.12	W	—
PCI I/O load = 30 pF	66 MHz, 32 bits	—	—	0.057	W	—
QUICC Engine block and other I/Os	UTOPIA 8-bit 31 PHYs	—	—	0.041	W	Multiply by number of interfaces used.
	TDM serial	—	—	0.001	W	
	TDM nibble	—	—	0.004	W	
	HDLC/TRAN serial	—	—	0.003	W	
	HDLC/TRAN nibble	—	—	0.025	W	
	DUART	—	—	0.017	W	
	MIIs	—	—	0.009	W	
	RMII	—	—	0.009	W	
	Ethernet management	—	—	0.002	W	
	USB	—	—	0.001	W	
	SPI	—	—	0.001	W	
	Timer output	—	—	0.002	W	

NOTE

AV_{DDn} (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	$OV_{DD} + 0.3$	V
Input low voltage	—	V_{IL}	-0.3	0.4	V

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
$\overline{\text{HRESET}}/\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

- $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is in PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
- t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
- POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{\text{OH}} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$OV_{\text{DD}} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR1 and DDR2 SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM ($Dn_GV_{DD}(typ) = 1.8\text{ V}$).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with Dn_GV_{DD} of $1.8 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MVREFn_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MVREFn_{REF} + 0.25$	—	V	—

Table 17 provides the input AC timing specifications for the DDR1 SDRAM ($Dn_GV_{DD}(typ) = 2.5\text{ V}$).

Table 17. DDR1 SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with Dn_GV_{DD} of $2.5 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MVREFn_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MVREFn_{REF} + 0.31$	—	V	—

Table 18 provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 18. DDR1 and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with Dn_GV_{DD} of $(1.8\text{ or }2.5\text{ V}) \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
	266 MHz	–750	750		
	200 MHz	–1250	1250		

Notes:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

Figure 5 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

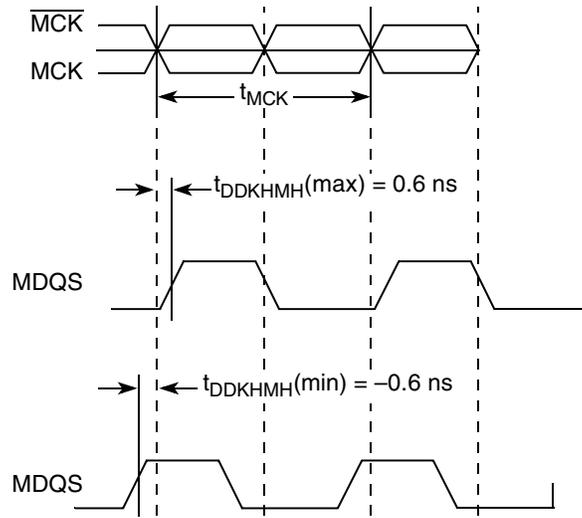


Figure 5. Timing Diagram for t_{DDKHMH}

Figure 6 shows the DDR1 and DDR2 SDRAM output timing diagram.

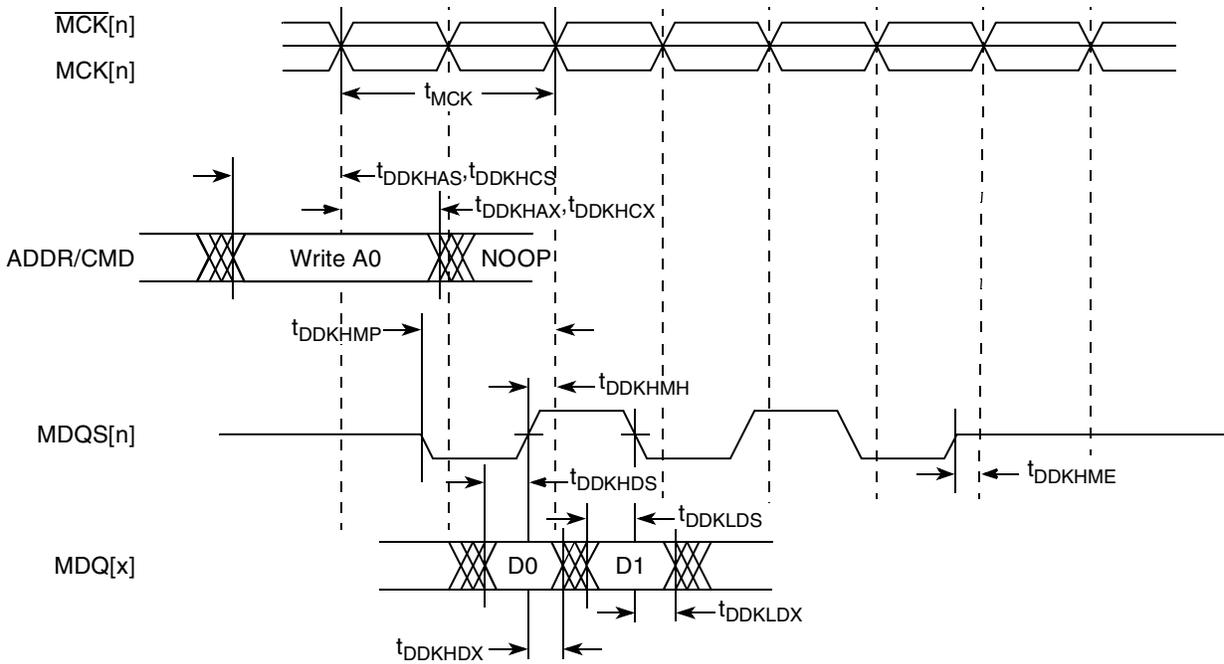


Figure 6. DDR1 and DDR2 SDRAM Output Timing Diagram

(management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in [Section 8.3, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 DC Electrical Characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in [Table 22](#).

Table 22. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$OV_{DD} = \text{Min}$	2.40	$OV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$OV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	-0.3	0.90	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$		—	± 5	μA

8.2 MII and RMII AC Timing Specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

[Table 23](#) provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3 \text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise time	t_{MTXR}	1.0	—	4.0	ns

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
RX_CLK clock fall time	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

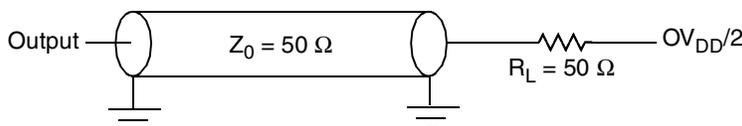


Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

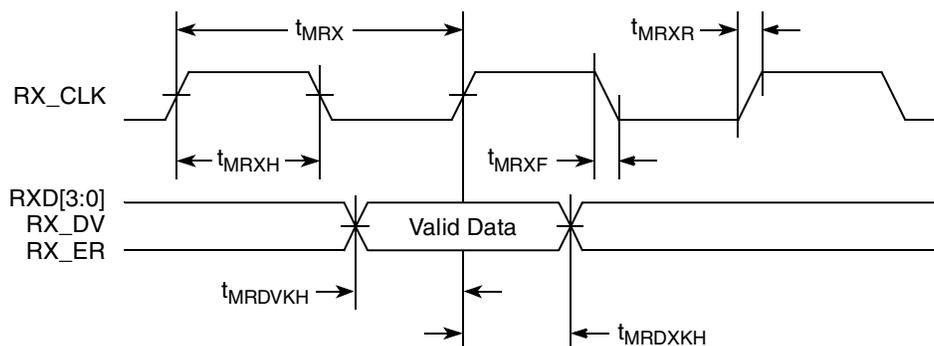


Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

Table 26. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
REF_CLK clock fall time $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load.

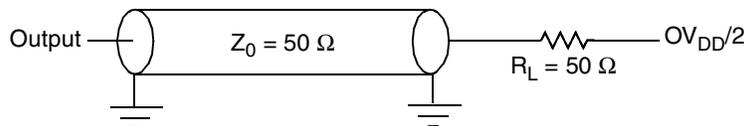


Figure 11. AC Test Load

Figure 12 shows the RMII receive AC timing diagram.

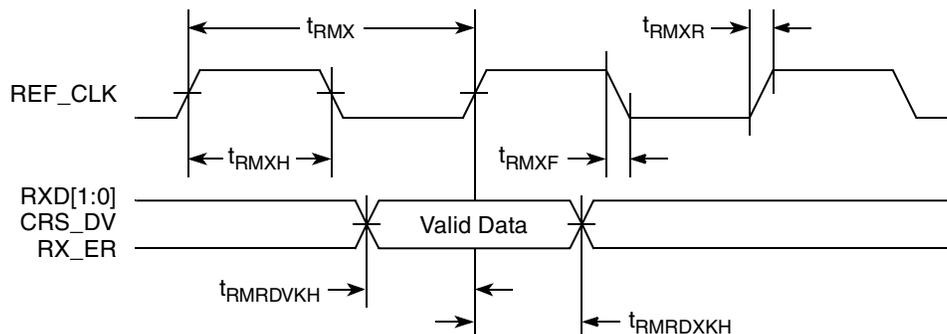


Figure 12. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in [Section 8.1, “Ethernet Controller \(10/100 Mbps\)—MII/RMII Electrical Characteristics.”](#)

Figure 15 through Figure 17 show the local bus signals.

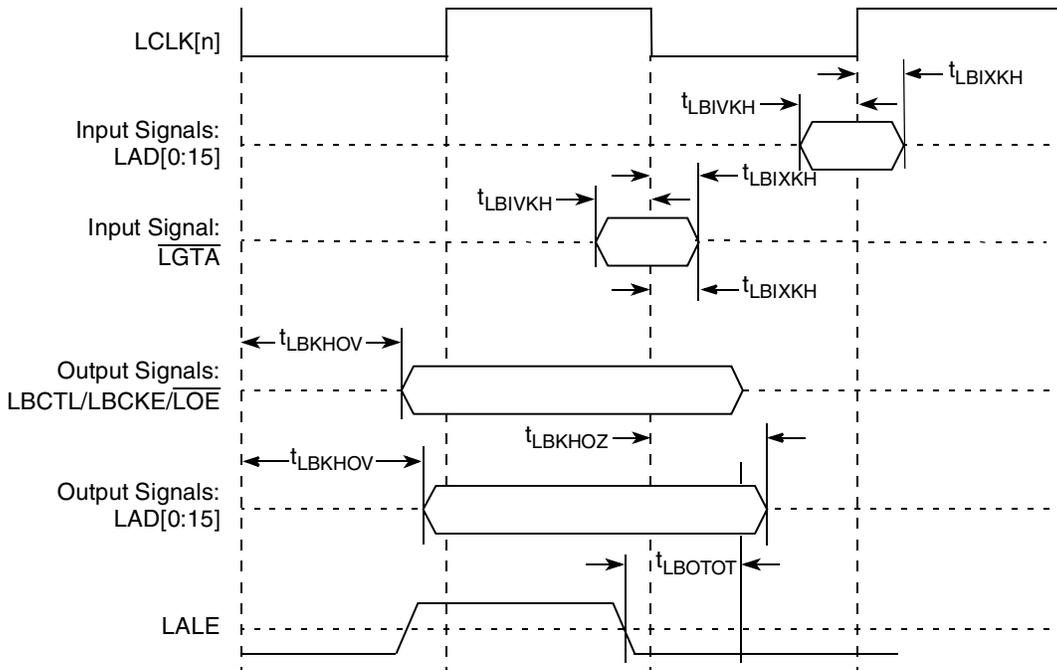


Figure 15. Local Bus Signals, Nonspecial Signals Only

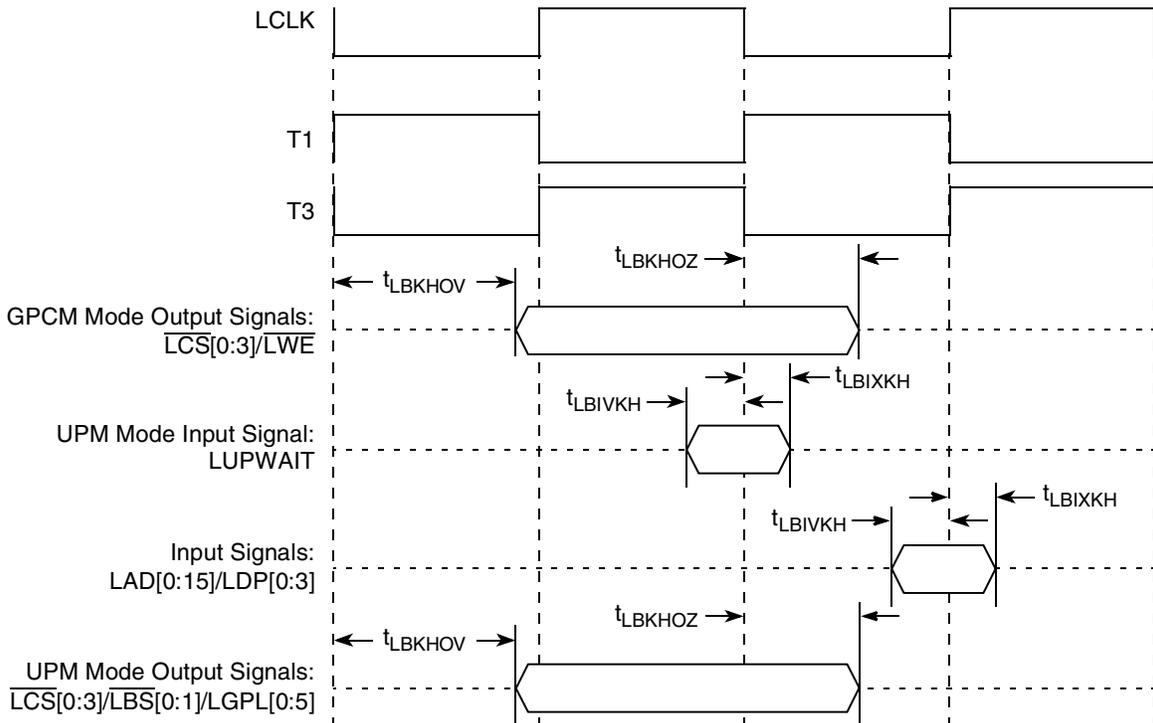


Figure 16. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

Figure 35 provides the AC test load for the UTOPIA.

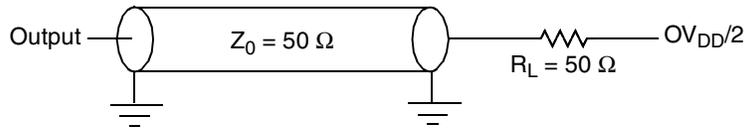


Figure 35. UTOPIA AC Test Load

Figure 36 and Figure 37 represent the AC timing from Table 49. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 36 shows the UTOPIA timing with external clock.

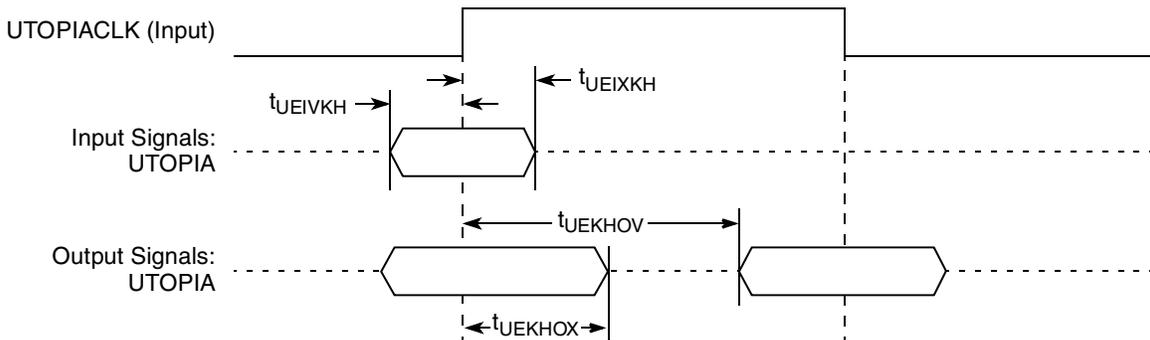


Figure 36. UTOPIA AC Timing (External Clock) Diagram

Figure 37 shows the UTOPIA timing with internal clock.

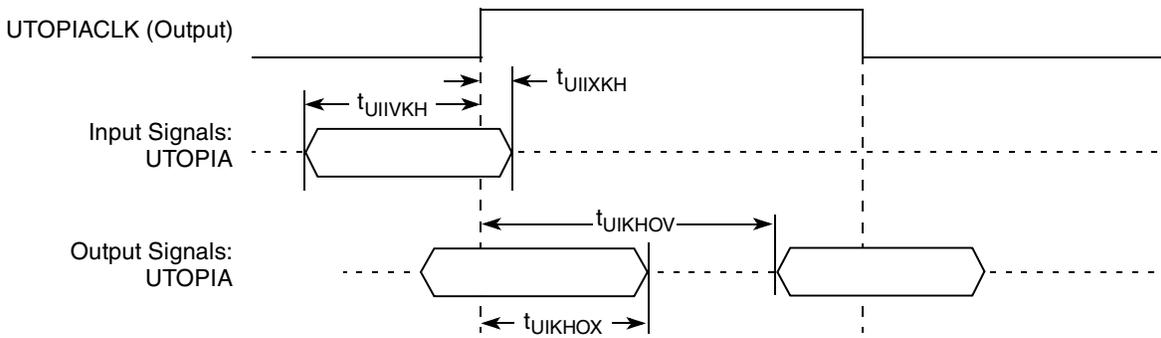


Figure 37. UTOPIA AC Timing (Internal Clock) Diagram

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	O	GV _{DD}	3
MEMC_MCK	AF14	O	GV _{DD}	—
$\overline{\text{MEMC_MCK}}$	AE14	O	GV _{DD}	—
MEMC_MODT	AF11	O	GV _{DD}	—
Local Bus Controller Interface				
LAD0	N25	IO	OV _{DD}	7
LAD1	P26	IO	OV _{DD}	7
LAD2	P25	IO	OV _{DD}	7
LAD3	R26	IO	OV _{DD}	7
LAD4	R25	IO	OV _{DD}	7
LAD5	T26	IO	OV _{DD}	7
LAD6	T25	IO	OV _{DD}	7
LAD7	U25	IO	OV _{DD}	7
LAD8	M24	IO	OV _{DD}	7
LAD9	N24	IO	OV _{DD}	7
LAD10	P24	IO	OV _{DD}	7
LAD11	R24	IO	OV _{DD}	7
LAD12	T24	IO	OV _{DD}	7
LAD13	U24	IO	OV _{DD}	7
LAD14	U26	IO	OV _{DD}	7
LAD15	V26	IO	OV _{DD}	7
LA16	K25	O	OV _{DD}	7
LA17	L25	O	OV _{DD}	7
LA18	L26	O	OV _{DD}	7
LA19	L24	O	OV _{DD}	7
LA20	M26	O	OV _{DD}	7
LA21	M25	O	OV _{DD}	7
LA22	N26	O	OV _{DD}	7
LA23	AC24	O	OV _{DD}	7
LA24	AC25	O	OV _{DD}	7
LA25	AB23	O	OV _{DD}	7
$\overline{\text{LCS0}}$	AB24	O	OV _{DD}	4

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Supplies				
AV _{DD1}	P3	I	AV _{DD1}	—
AV _{DD2}	AA1	I	AV _{DD2}	—
AV _{DD3}	AB15	I	AV _{DD3}	—
AV _{DD4}	C24	I	AV _{DD4}	—
MVREF1	AB8	I	DDR reference voltage	—
MVREF2	AB17	I	DDR reference voltage	—
PCI				
PCI_INTA /IRQ_OUT	AF2	O	OV _{DD}	2
PCI_RESET_OUT	AE2	O	OV _{DD}	—
PCI_AD0/MSRCID0 (DDR ID)	L1	IO	OV _{DD}	—
PCI_AD1/MSRCID1 (DDR ID)	L2	IO	OV _{DD}	—
PCI_AD2/MSRCID2 (DDR ID)	M1	IO	OV _{DD}	—
PCI_AD3/MSRCID3 (DDR ID)	M2	IO	OV _{DD}	—
PCI_AD4/MSRCID4 (DDR ID)	L3	IO	OV _{DD}	—
PCI_AD5/MDVAL (DDR ID)	N1	IO	OV _{DD}	—
PCI_AD6	N2	IO	OV _{DD}	—
PCI_AD7	M3	IO	OV _{DD}	—
PCI_AD8	P1	IO	OV _{DD}	—
PCI_AD9	R1	IO	OV _{DD}	—
PCI_AD10	N3	IO	OV _{DD}	—
PCI_AD11	N4	IO	OV _{DD}	—
PCI_AD12	T1	IO	OV _{DD}	—
PCI_AD13	R2	IO	OV _{DD}	—
PCI_AD14/ECID_TMODE_IN	T2	IO	OV _{DD}	—
PCI_AD15	U1	IO	OV _{DD}	—
PCI_AD16	Y2	IO	OV _{DD}	—
PCI_AD17	Y1	IO	OV _{DD}	—
PCI_AD18	AA2	IO	OV _{DD}	—
PCI_AD19	AB1	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PB17/BRGO1/CE_EXT_REQ1	D10	IO	OV _{DD}	—
GPIO_PB18/Enet4_TXD[0]/SER4_TXD[0]/TDMD_TXD[0]	C10	IO	OV _{DD}	—
GPIO_PB19/Enet4_TXD[1]/SER4_TXD[1]/TDMD_TXD[1]	C9	IO	OV _{DD}	—
GPIO_PB20/Enet4_TXD[2]/SER4_TXD[2]/TDMD_TXD[2]	D8	IO	OV _{DD}	—
GPIO_PB21/Enet4_TXD[3]/SER4_TXD[3]/TDMD_TXD[3]	C8	IO	OV _{DD}	—
GPIO_PB22/Enet4_RXD[0]/SER4_RXD[0]/TDMD_RXD[0]	C15	IO	OV _{DD}	—
GPIO_PB23/Enet4_RXD[1]/SER4_RXD[1]/TDMD_RXD[1]	C14	IO	OV _{DD}	—
GPIO_PB24/Enet4_RXD[2]/SER4_RXD[2]/TDMD_RXD[2]	D13	IO	OV _{DD}	—
GPIO_PB25/Enet4_RXD[3]/SER4_RXD[3]/TDMD_RXD[3]	C13	IO	OV _{DD}	—
GPIO_PB26/Enet4_RX_ER/SER4_CD/TDMD_REQ	C12	IO	OV _{DD}	—
GPIO_PB27/Enet4_TX_ER/TDMD_CLKO	D11	IO	OV _{DD}	—
GPIO_PB28/Enet4_RX_DV/SER4_CTS/TDMD_RSYNC	D12	IO	OV _{DD}	—
GPIO_PB29/Enet4_COL/RXD[4]/SER4_RXD[4]/TDMD_STROBE	D7	IO	OV _{DD}	—
GPIO_PB30/Enet4_TX_EN/SER4_RTS/TDMD_TSYNC	C11	IO	OV _{DD}	—
GPIO_PB31/Enet4_CRS/SDET	C7	IO	OV _{DD}	—
GPIO_PC0/UPC1_TxDATA[0]/SER5_TXD[0]	A18	IO	OV _{DD}	—
GPIO_PC1/UPC1_TxDATA[1]/SER5_TXD[1]	A19	IO	OV _{DD}	—
GPIO_PC2/UPC1_TxDATA[2]/SER5_TXD[2]	B18	IO	OV _{DD}	—
GPIO_PC3/UPC1_TxDATA[3]/SER5_TXD[3]	B19	IO	OV _{DD}	—
GPIO_PC4/UPC1_TxDATA[4]	A24	IO	OV _{DD}	—
GPIO_PC5/UPC1_TxDATA[5]	B24	IO	OV _{DD}	—
GPIO_PC6/UPC1_TxDATA[6]	A23	IO	OV _{DD}	—
GPIO_PC7/UPC1_TxDATA[7]	B26	IO	OV _{DD}	—
GPIO_PC8/UPC1_RxDATA[0]/SER5_RXD[0]	A21	IO	OV _{DD}	—
GPIO_PC9/UPC1_RxDATA[1]/SER5_RXD[1]	B20	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PD10/GTM1_TIN2/GTM2_TIN1/CLK17	J24	IO	OV _{DD}	—
GPIO_PD11/GTM1_TGATE2/GTM2_TGATE1	B25	IO	OV _{DD}	—
GPIO_PD12/GTM1_TOUT2/GTM2_TOUT1	C4	IO	OV _{DD}	—
GPIO_PD13/GTM1_TIN3/GTM2_TIN4/BRGO8	D4	IO	OV _{DD}	—
GPIO_PD14/GTM1_TGATE3/GTM2_TGATE4	D5	IO	OV _{DD}	—
GPIO_PD15/GTM1_TOUT3	A5	IO	OV _{DD}	—
GPIO_PD16/GTM1_TIN4/GTM2_TIN3	B5	IO	OV _{DD}	—
GPIO_PD17/GTM1_TGATE4/GTM2_TGATE3	C5	IO	OV _{DD}	—
GPIO_PD18/GTM1_TOUT4/GTM2_TOUT3	A6	IO	OV _{DD}	—
GPIO_PD19/CE_RISC1_INT/CE_EXT_REQ4	B6	IO	OV _{DD}	—
GPIO_PD20/CLK18/BRGO6	D21	IO	OV _{DD}	—
GPIO_PD21/CLK16/BRGO5/UPC1_CLKO	C19	IO	OV _{DD}	—
GPIO_PD22/CLK4/BRGO9/UCC2_CLKO	A7	IO	OV _{DD}	—
GPIO_PD23/CLK3/BRGO10/UCC3_CLKO	B7	IO	OV _{DD}	—
GPIO_PD24/CLK10/BRGO2/UCC4_CLKO	A12	IO	OV _{DD}	—
GPIO_PD25/CLK13/BRGO16/UCC5_CLKO	B10	IO	OV _{DD}	—
GPIO_PD26/CLK2/BRGO4/UCC1_CLKO	E4	IO	OV _{DD}	—
GPIO_PD27/CLK1/BRGO3	F4	IO	OV _{DD}	—
GPIO_PD28/CLK19/BRGO11	D15	IO	OV _{DD}	—
GPIO_PD29/CLK15/BRGO8	C6	IO	OV _{DD}	—
GPIO_PD30/CLK14	D6	IO	OV _{DD}	—
GPIO_PD31/CLK7/BRGO15	E24	IO	OV _{DD}	—
Power and Ground Supplies				
GV _{DD}	AA8, AA10, AA11, AA13, AA14, AA16, AA17, AA19, AA21, AB9, AB10, AB11, AB12, AB14, AB18, AB20, AB21, AC6, AC8, AC14, AC18	GV _{DD}	—	—
OV _{DD}	E5, E6, E8, E9, E10, E12, E14, E15, E16, E18, E19, E20, E22, F5, F6, F8, F10, F14, F16, F19, F22, G22, H5, H6, H21, J5, J22, K21, K22, L5, L6, L22, M5, M22, N5, N21, N22, P6, P22, P23, R5, R23, T5, T21, T22, U6, U22, V5, V22, W22, Y5, AB5, AB6, AC5	OV _{DD}	—	—

22 Clocking

Figure 43 shows the internal distribution of clocks within the MPC8323E.

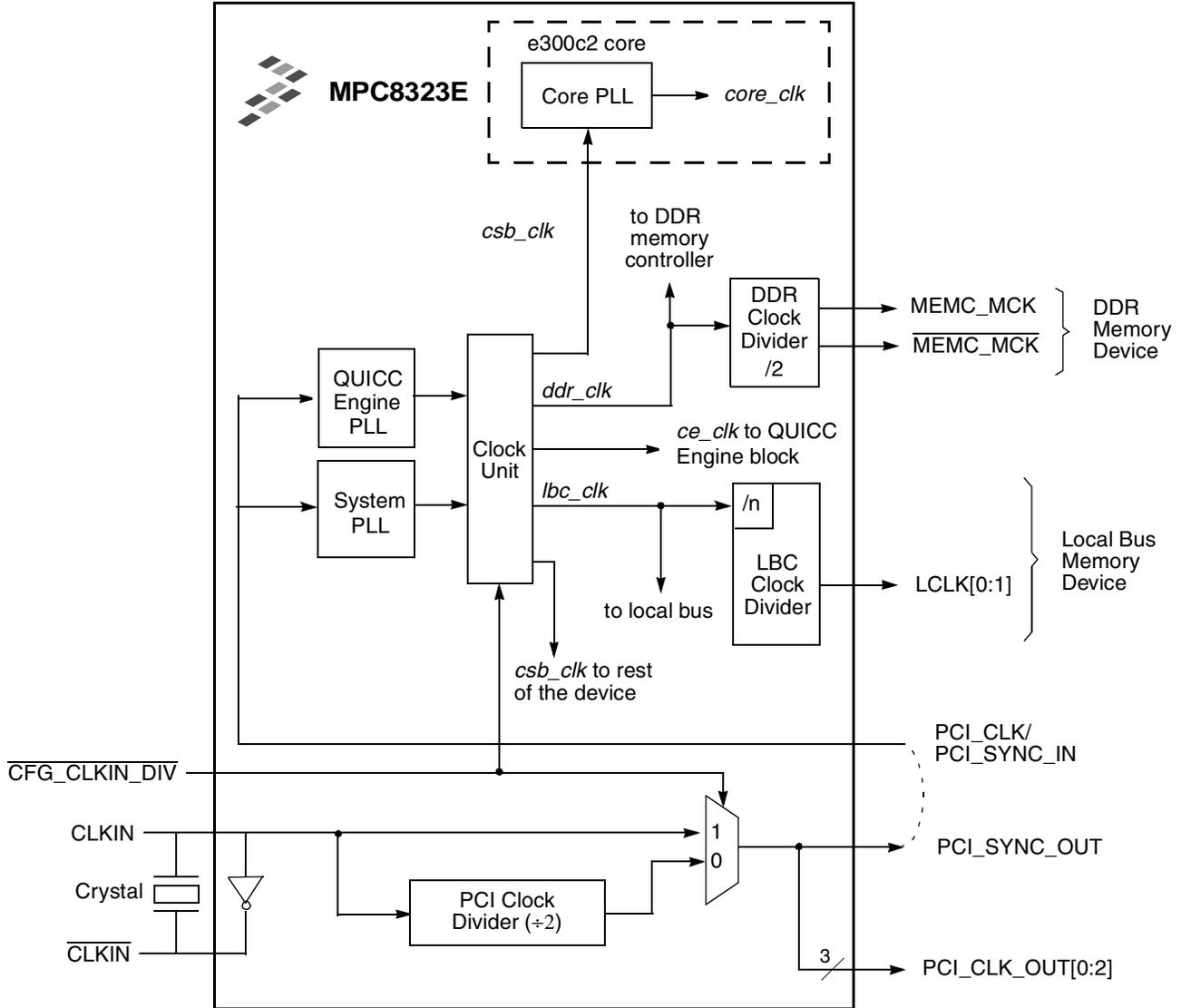


Figure 43. MPC8323E Clock Subsystem

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode, respectively.

Table 64. Package Thermal Characteristics for PBGA (continued)

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-package top	Natural convection	Ψ_{JT}	2	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

23.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

23.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

23.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$