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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8321zqafdc

1.1.2 Serial Interfaces

The MPC8323E serial interfaces are as follows:

- Support for one UL2 interface with 31 multi-PHY addresses (MPC8323E and MPC8323 only)
- Support for up to three 10/100 Mbps Ethernet interfaces using MII or RMII
- Support for up to four T1/E1/J1/E3 or DS-3 serial interfaces (TDM)
- Support for dual UART and SPI interfaces and a single I²C interface

1.2 QUICC Engine Block

The QUICC Engine block is a versatile communications complex that integrates several communications peripheral controllers. It provides on-chip system design for a variety of applications, particularly in communications and networking systems. The QUICC Engine block has the following features:

- One 32-bit RISC controller for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
 - 10/100 Mbps Ethernet/IEEE 802.3® standard
 - IP support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
 - ATM protocol through UTOPIA interface (note that the MPC8321 and MPC8321E do not support the UTOPIA interface)
 - HDLC /transparent up to 70-Mbps full-duplex
 - HDLC bus up to 10 Mbps
 - Asynchronous HDLC
 - UART
 - BISYNC up to 2 Mbps
 - QUICC multi-channel controller (QMC) for 64 TDM channels
- One UTOPIA interface (UPC1) supporting 31 multi-PHYs (MPC8323E- and MPC8323-specific)
- Two serial peripheral interfaces (SPI). SPI2 is dedicated to Ethernet PHY management.
- Four TDM interfaces
- Thirteen independent baud rate generators and 19 input clock pins for supplying clocks to UCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

The UCCs are similar to the PowerQUICC II peripherals: SCC (BISYNC, UART, and HDLC bus) and FCC (fast Ethernet, HDLC, transparent, and ATM).

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8323E. The MPC8323E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	-0.3 to 1.26	V	—
PLL supply voltage		AV_{DDn}	-0.3 to 1.26	V	—
DDR1 and DDR2 DRAM I/O voltage		GV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	—
PCI, local bus, DUART, system control and power management, I ² C, SPI, MII, RMII, MII management, and JTAG I/O voltage		OV_{DD}	-0.3 to 3.6	V	—
Input voltage	DDR1/DDR2 DRAM signals	MV_{IN}	-0.3 to ($GV_{DD} + 0.3$)	V	2
	DDR1/DDR2 DRAM reference	MV_{REF}	-0.3 to ($GV_{DD} + 0.3$)	V	2
	Local bus, DUART, CLKIN, system control and power management, I ² C, SPI, and JTAG signals	OV_{IN}	-0.3 to ($OV_{DD} + 0.3$)	V	3
	PCI	OV_{IN}	-0.3 to ($OV_{DD} + 0.3$)	V	5
Storage temperature range		T_{STG}	-55 to 150	°C	—

Notes:

- Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

Table 7. CLKIN DC Electrical Characteristics (continued)

CLKIN input current	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	± 5	μA
PCI_SYNC_IN input current	$0\text{ V} \leq V_{IN} \leq 0.5\text{ V}$ or $OV_{DD} - 0.5\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	± 5	μA
PCI_SYNC_IN input current	$0.5\text{ V} \leq V_{IN} \leq OV_{DD} - 0.5\text{ V}$	I_{IN}	—	± 50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 8 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the MPC8323E.

Table 8. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	25	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN rise and fall time	t_{KH}, t_{KL}	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	± 150	ps	4, 5

Notes:

- Caution:** The system, core, security, and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

5 RESET Initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8323E. Table 9 provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of \overline{HRESET} or \overline{SRESET} (input) to activate reset flow	32	—	$t_{PCI_SYNC_IN}$	1
Required assertion time of $\overline{PORESET}$ with stable clock applied to CLKIN when the MPC8323E is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{PORESET}$ with stable clock applied to PCI_SYNC_IN when the MPC8323E is in PCI agent mode	32	—	$t_{PCI_SYNC_IN}$	1

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
$\overline{\text{HRESET}}/\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

- $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is in PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
- t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
- POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{\text{OH}} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$\text{OV}_{\text{DD}} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
RX_CLK clock fall time	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

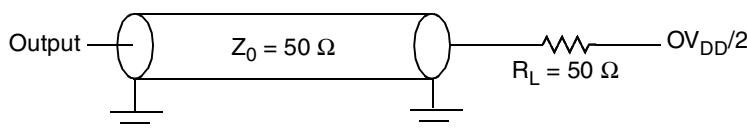


Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

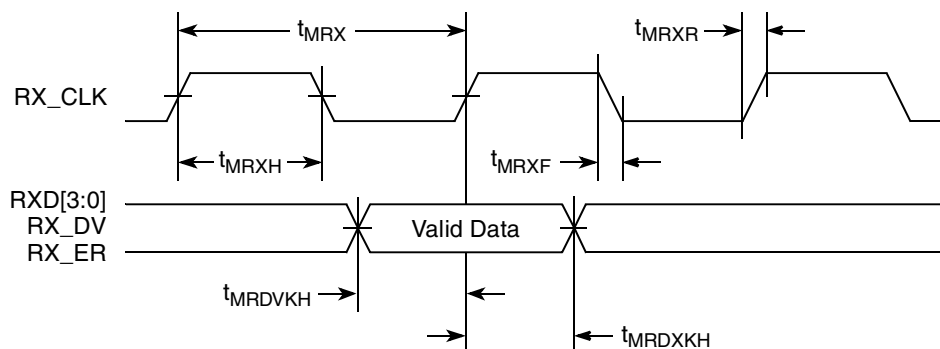


Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMI Transmit AC Timing Specifications

Table 23 provides the RMI transmit AC timing specifications.

Table 25. RMI Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMI data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{RMXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMI transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMI(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the RMI transmit AC timing diagram.

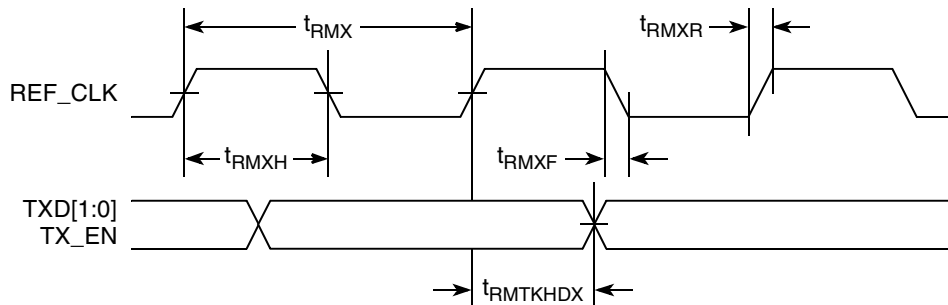


Figure 10. RMI Transmit AC Timing Diagram

8.2.2.2 RMI Receive AC Timing Specifications

Table 24 provides the RMI receive AC timing specifications.

Table 26. RMI Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{RMXR}	1.0	—	4.0	ns

Figure 13 shows the MII management AC timing diagram.

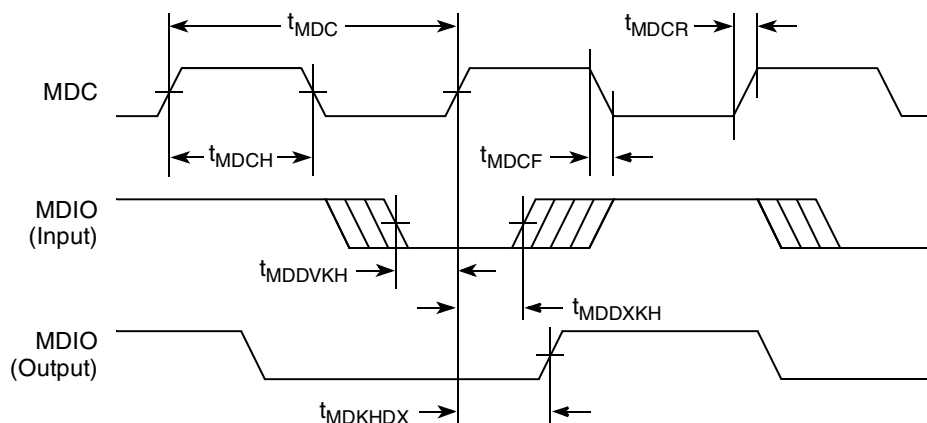


Figure 13. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8323E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V
Input current	I_{IN}	—	± 5	μA

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8323E.

Table 30. Local Bus General Timing Parameters

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK n)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK n)	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5

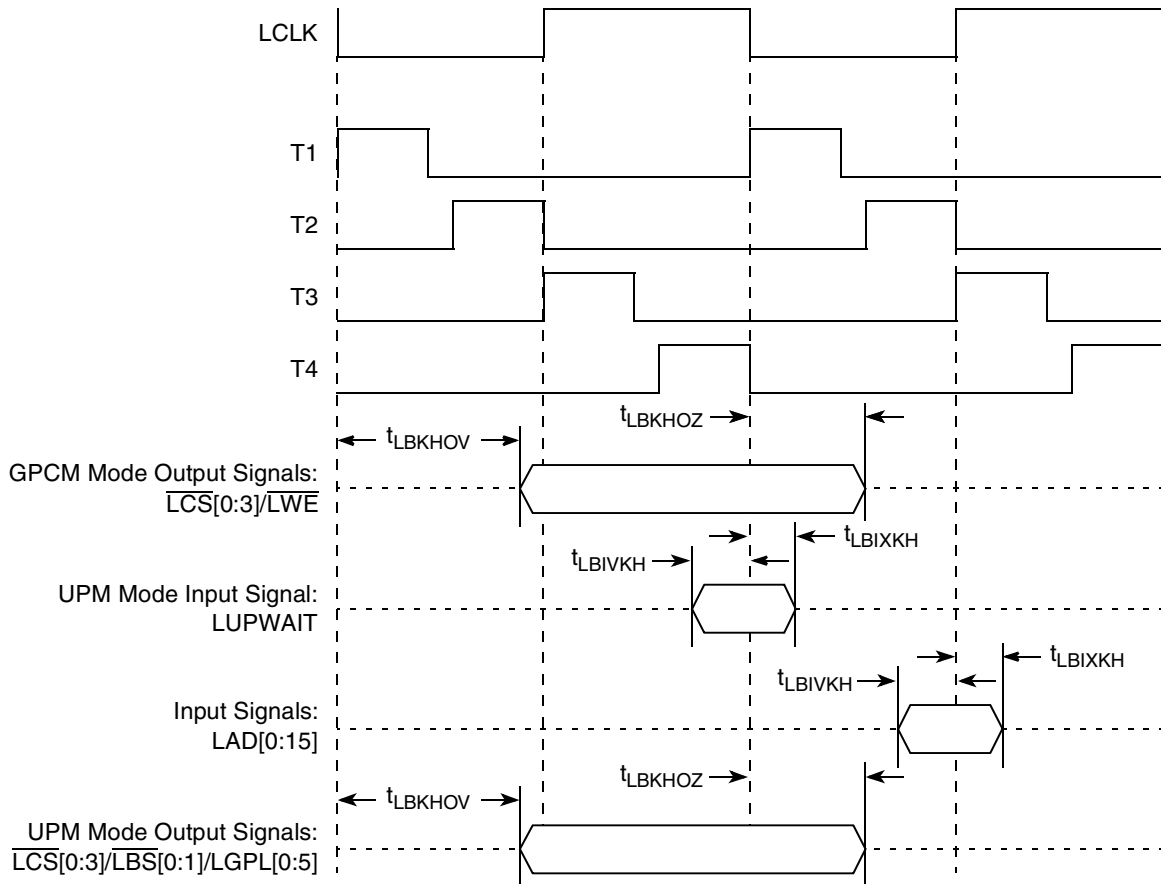


Figure 17. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8323E.

10.1 JTAG DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E.

Table 31. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.5	$OV_{DD} + 0.3$	V

Table 31. JTAG Interface DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E. [Table 32](#) provides the JTAG AC timing specifications as defined in [Figure 19](#) through [Figure 22](#).

Table 32. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see [Table 2](#)).

Parameter	Symbol ²	Min	Max	Unit	Notes	
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—	
JTAG external clock cycle time	t_{JTG}	30	—	ns	—	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	11	—	ns	—	
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3	
Input setup times:	Boundary-scan data TMS, TDI	t_{JTDVKH}	4	—	ns	4
		t_{JTIVKH}	4	—		
Input hold times:	Boundary-scan data TMS, TDI	t_{JTDXKH}	10	—	ns	4
		t_{JTIXKH}	10	—		
Valid times:	Boundary-scan data TDO	t_{JTKLDV}	2	15	ns	5
		t_{JTKLOV}	2	15		
Output hold times:	Boundary-scan data TDO	t_{JTKLDX}	2	—	ns	5
		t_{JTKLOX}	2	—		

Figure 28 provides the AC test load for the timers.

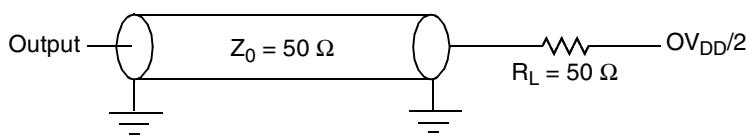


Figure 28. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8323E.

14.1 GPIO DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E GPIO.

Table 40. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA	—

Note:

1. This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

Table 41 provides the GPIO input and output AC timing specifications.

Table 41. GPIO Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 35 provides the AC test load for the UTOPIA.

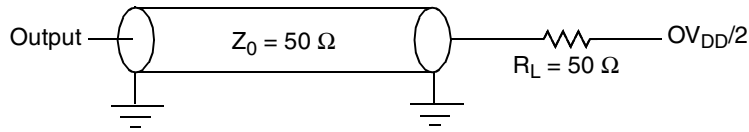


Figure 35. UTOPIA AC Test Load

Figure 36 and Figure 37 represent the AC timing from Table 49. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 36 shows the UTOPIA timing with external clock.

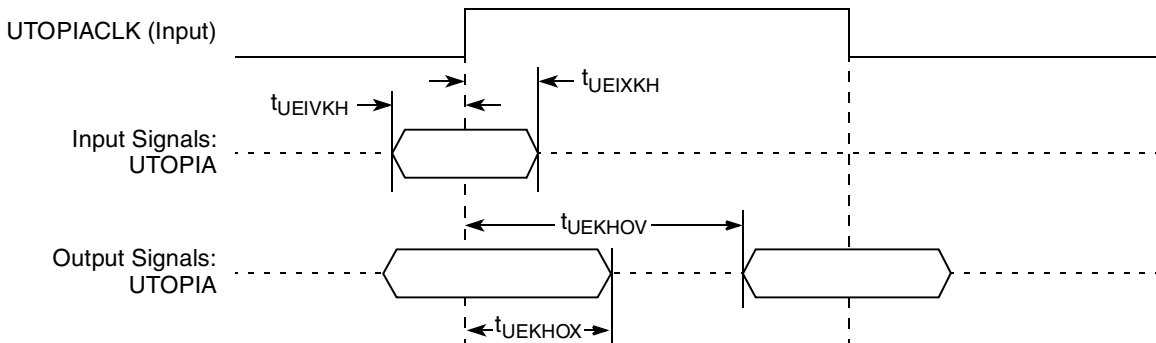


Figure 36. UTOPIA AC Timing (External Clock) Diagram

Figure 37 shows the UTOPIA timing with internal clock.

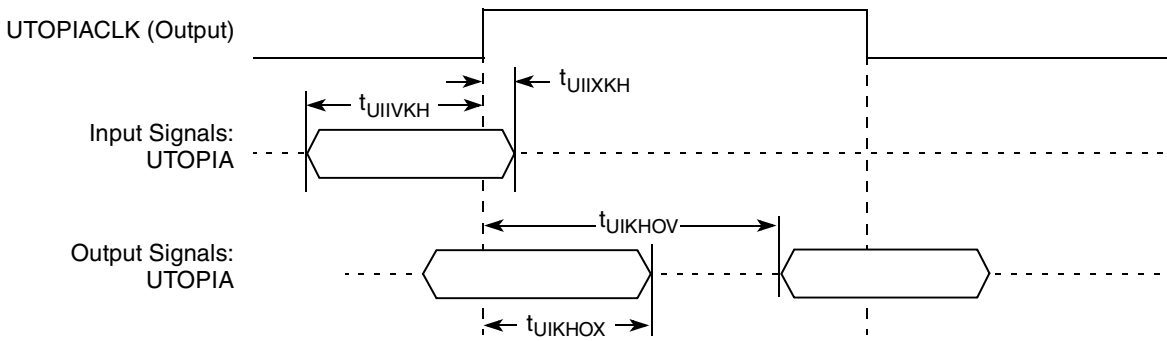


Figure 37. UTOPIA AC Timing (Internal Clock) Diagram

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications¹ (continued)

Characteristic	Symbol ²	Min	Max	Unit
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 52. Synchronous UART AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	5.5	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	10	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	5.5	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	8	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	4	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	0	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{UAIKHOX}$ symbolizes the outputs internal timing (UAI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 38 provides the AC test load.

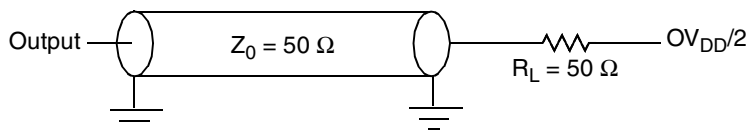

Figure 38. AC Test Load

Figure 39 and Figure 40 represent the AC timing from Table 51. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

Table 55. MPC8323E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	AE9	IO	GV _{DD}	—
MEMC_MDQ1	AD10	IO	GV _{DD}	—
MEMC_MDQ2	AF10	IO	GV _{DD}	—
MEMC_MDQ3	AF9	IO	GV _{DD}	—
MEMC_MDQ4	AF7	IO	GV _{DD}	—
MEMC_MDQ5	AE10	IO	GV _{DD}	—
MEMC_MDQ6	AD9	IO	GV _{DD}	—
MEMC_MDQ7	AF8	IO	GV _{DD}	—
MEMC_MDQ8	AE6	IO	GV _{DD}	—
MEMC_MDQ9	AD7	IO	GV _{DD}	—
MEMC_MDQ10	AF6	IO	GV _{DD}	—
MEMC_MDQ11	AC7	IO	GV _{DD}	—
MEMC_MDQ12	AD8	IO	GV _{DD}	—
MEMC_MDQ13	AE7	IO	GV _{DD}	—
MEMC_MDQ14	AD6	IO	GV _{DD}	—
MEMC_MDQ15	AF5	IO	GV _{DD}	—
MEMC_MDQ16	AD18	IO	GV _{DD}	—
MEMC_MDQ17	AE19	IO	GV _{DD}	—
MEMC_MDQ18	AF17	IO	GV _{DD}	—
MEMC_MDQ19	AF19	IO	GV _{DD}	—
MEMC_MDQ20	AF18	IO	GV _{DD}	—
MEMC_MDQ21	AE18	IO	GV _{DD}	—
MEMC_MDQ22	AF20	IO	GV _{DD}	—
MEMC_MDQ23	AD19	IO	GV _{DD}	—
MEMC_MDQ24	AD21	IO	GV _{DD}	—
MEMC_MDQ25	AF22	IO	GV _{DD}	—
MEMC_MDQ26	AC21	IO	GV _{DD}	—
MEMC_MDQ27	AF21	IO	GV _{DD}	—
MEMC_MDQ28	AE21	IO	GV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LCS1}}$	AB25	O	OV_{DD}	4
$\overline{\text{LCS2}}$	AA23	O	OV_{DD}	4
$\overline{\text{LCS3}}$	AA24	O	OV_{DD}	4
$\overline{\text{LWE0}}$	Y23	O	OV_{DD}	4
$\overline{\text{LWE1}}$	W25	O	OV_{DD}	4
LBCTL	V25	O	OV_{DD}	4
LALE	V24	O	OV_{DD}	7
CFG_RESET_SOURCE[0]/LSDA10/LGPL0	L23	IO	OV_{DD}	—
CFG_RESET_SOURCE[1]/ $\overline{\text{LSDWE}}$ /LGPL1	K23	IO	OV_{DD}	—
$\overline{\text{LSDRAS}}$ /LGPL2/ $\overline{\text{LOE}}$	J23	O	OV_{DD}	4
CFG_RESET_SOURCE[2]/ $\overline{\text{LSDCAS}}$ /LGPL3	H23	IO	OV_{DD}	—
LGPL4/ $\overline{\text{LGT\AA}}$ /LUPWAIT/LPBSE	G23	IO	OV_{DD}	4, 8
LGPL5	AC22	O	OV_{DD}	4
LCLK0	Y24	O	OV_{DD}	7
LCLK1	Y25	O	OV_{DD}	7
DUART				
UART_SOUT1/MSRCID0 (DDR ID)/LSRCID0	G1	IO	OV_{DD}	—
UART_SIN1/MSRCID1 (DDR ID)/LSRCID1	G2	IO	OV_{DD}	—
$\overline{\text{UART_CTS1}}$ /MSRCID2 (DDR ID)/LSRCID2	H3	IO	OV_{DD}	—
$\overline{\text{UART_RTS1}}$ /MSRCID3 (DDR ID)/LSRCID3	K3	IO	OV_{DD}	—
UART_SOUT2/MSRCID4 (DDR ID)/LSRCID4	H2	IO	OV_{DD}	—
UART_SIN2/MDVAL (DDR ID)/LDVAL	H1	IO	OV_{DD}	—
$\overline{\text{UART_CTS2}}$	J3	IO	OV_{DD}	—
$\overline{\text{UART_RTS2}}$	K4	IO	OV_{DD}	—
I²C interface				
$\overline{\text{IIC_SDA/CKSTOP_OUT}}$	AE24	IO	OV_{DD}	2
$\overline{\text{IIC_SCL/CKSTOP_IN}}$	AF24	IO	OV_{DD}	2
Programmable Interrupt Controller				
$\overline{\text{MCP_OUT}}$	AD25	O	OV_{DD}	—
$\overline{\text{IRQ0/MCP_IN}}$	AD26	I	OV_{DD}	—
$\overline{\text{IRQ1}}$	K1	IO	OV_{DD}	—
$\overline{\text{IRQ2}}$	K2	I	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PB17/BRGO1/CE_EXT_REQ1	D10	IO	OV _{DD}	—
GPIO_PB18/Enet4_TXD[0]/SER4_TXD[0]/TDMD_TXD[0]	C10	IO	OV _{DD}	—
GPIO_PB19/Enet4_TXD[1]/SER4_TXD[1]/TDMD_TXD[1]	C9	IO	OV _{DD}	—
GPIO_PB20/Enet4_TXD[2]/SER4_TXD[2]/TDMD_TXD[2]	D8	IO	OV _{DD}	—
GPIO_PB21/Enet4_TXD[3]/SER4_TXD[3]/TDMD_TXD[3]	C8	IO	OV _{DD}	—
GPIO_PB22/Enet4_RXD[0]/SER4_RXD[0]/TDMD_RXD[0]	C15	IO	OV _{DD}	—
GPIO_PB23/Enet4_RXD[1]/SER4_RXD[1]/TDMD_RXD[1]	C14	IO	OV _{DD}	—
GPIO_PB24/Enet4_RXD[2]/SER4_RXD[2]/TDMD_RXD[2]	D13	IO	OV _{DD}	—
GPIO_PB25/Enet4_RXD[3]/SER4_RXD[3]/TDMD_RXD[3]	C13	IO	OV _{DD}	—
GPIO_PB26/Enet4_RX_ER/SER4_CD/TDMD_REQ	C12	IO	OV _{DD}	—
GPIO_PB27/Enet4_TX_ER/TDMD_CLKO	D11	IO	OV _{DD}	—
GPIO_PB28/Enet4_RX_DV/SER4_CTS/TDMD_RSYNC	D12	IO	OV _{DD}	—
GPIO_PB29/Enet4_COL/RXD[4]/SER4_RXD[4]/TDMD_STROBE	D7	IO	OV _{DD}	—
GPIO_PB30/Enet4_TX_EN/SER4_RTS/TDMD_TSYNC	C11	IO	OV _{DD}	—
GPIO_PB31/Enet4_CRS/SDET	C7	IO	OV _{DD}	—
GPIO_PC0/UPC1_TxDATA[0]/SER5_TXD[0]	A18	IO	OV _{DD}	—
GPIO_PC1/UPC1_TxDATA[1]/SER5_TXD[1]	A19	IO	OV _{DD}	—
GPIO_PC2/UPC1_TxDATA[2]/SER5_TXD[2]	B18	IO	OV _{DD}	—
GPIO_PC3/UPC1_TxDATA[3]/SER5_TXD[3]	B19	IO	OV _{DD}	—
GPIO_PC4/UPC1_TxDATA[4]	A24	IO	OV _{DD}	—
GPIO_PC5/UPC1_TxDATA[5]	B24	IO	OV _{DD}	—
GPIO_PC6/UPC1_TxDATA[6]	A23	IO	OV _{DD}	—
GPIO_PC7/UPC1_TxDATA[7]	B26	IO	OV _{DD}	—
GPIO_PC8/UPC1_RxDATA[0]/SER5_RXD[0]	A21	IO	OV _{DD}	—
GPIO_PC9/UPC1_RxDATA[1]/SER5_RXD[1]	B20	IO	OV _{DD}	—

22.1 Clocking in PCI Host Mode

When the MPC8323E is configured as a PCI host device ($RCWH[PCIHOST] = 1$), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider ($\div 2$) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexors. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

22.1.1 PCI Clock Outputs (PCI_CLK_OUT[0:2])

When the MPC8323E is configured as a PCI host, it provides three separate clock output signals, PCI_CLK_OUT[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOEn] bit. All output clocks are phase-aligned to each other.

22.2 Clocking in PCI Agent Mode

When the MPC8323E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND, and the clock output signals, PCI_CLK_OUT n and PCI_SYNC_OUT, are not used.

22.3 System Clock Domains

As shown in [Figure 43](#), the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*ce_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lb_clk*)

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = [PCI_SYNC_IN \times (1 + \sim\overline{CFG_CLKIN_DIV})] \times SPMF$$

In PCI host mode, $PCI_SYNC_IN \times (1 + \sim\overline{CFG_CLKIN_DIV})$ is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300c2 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See the “Reset Configuration” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

22.5 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 60 shows the encodings for RCWL[COREPLL]. COREPLL values not listed in Table 60 should be considered reserved.

Table 60. e300 Core PLL Configuration

RCWL[COREPLL]			<i>core_clk</i> : <i>csb_clk</i> Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷2
01	0001	1	1.5:1	÷4
10	0001	1	1.5:1	÷8
11	0001	1	1.5:1	÷8
00	0010	0	2:1	÷2
01	0010	0	2:1	÷4
10	0010	0	2:1	÷8
11	0010	0	2:1	÷8
00	0010	1	2.5:1	÷2
01	0010	1	2.5:1	÷4
10	0010	1	2.5:1	÷8
11	0010	1	2.5:1	÷8
00	0011	0	3:1	÷2
01	0011	0	3:1	÷4
10	0011	0	3:1	÷8
11	0011	0	3:1	÷8

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 500–800 MHz.

22.7 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8323E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the `csb_clk` as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. [Table 63](#) shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

Table 63. Suggested PLL Configurations

Conf No.	SPMF	Core PLL	CEMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0110	0	33.33	133.33	266.66	200
2	0100	0000101	1000	0	25	100	250	200
3	0010	0000100	0011	0	66.67	133.33	266.66	200
4	0100	0000101	0110	0	33.33	133.33	333.33	200
5	0101	0000101	1000	0	25	125	312.5	200
6	0010	0000101	0011	0	66.67	133.33	333.33	200

23 Thermal

This section describes the thermal specifications of the MPC8323E.

23.1 Thermal Characteristics

[Table 64](#) provides the package thermal characteristics for the 516 27 × 27 mm PBGA of the MPC8323E.

Table 64. Package Thermal Characteristics for PBGA

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	21	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	23	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	13	°C/W	4
Junction-to-case	—	$R_{\theta JC}$	9	°C/W	5

interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

P_D = power dissipation (W)

24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8323E.

24.1 System Clocking

The MPC8323E includes three PLLs.

- The system PLL (AV_{DD2}) generates the system clock from the externally supplied CLKIN input. The frequency ratio between the system and CLKIN is selected using the system PLL ratio configuration bits as described in [Section 22.4, “System PLL Configuration.”](#)
- The e300 core PLL (AV_{DD3}) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in [Section 22.5, “Core PLL Configuration.”](#)
- The QUICC Engine PLL (AV_{DD1}) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each AV_{DDⁿ} pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in [Figure 44](#), one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

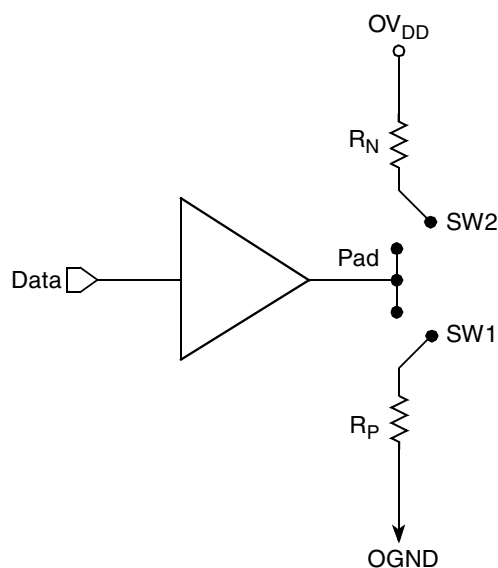


Figure 45. Driver Impedance Measurement

The value of this resistance and the strength of the driver’s current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 65 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 65. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, $T_j = 105^\circ\text{C}$.

24.6 Configuration Pin Multiplexing

The MPC8323E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.