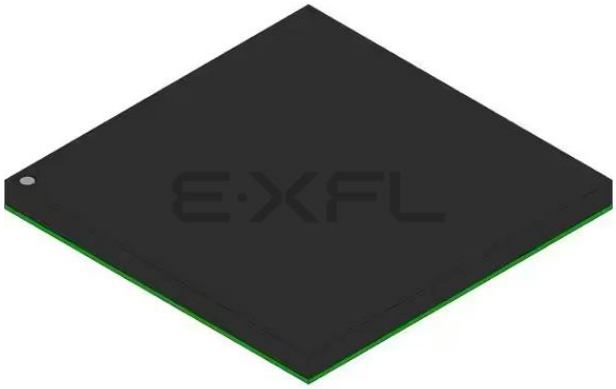

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | - |
| Number of Cores/Bus Width | - |
| Speed | - |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | - |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | - |
| Operating Temperature | - |
| Security Features | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8323cvraddca |

## 1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i™ standard, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

## 1.4 DDR Memory Controller

The MPC8323E DDR1/DDR2 memory controller includes the following features:

- Single 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266-MHz data rate
- Support for two ×16 devices
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O
- Support for 1 chip select only
- FCRAM, ECC, hardware/software calibration, bit deskew, QIN stage, or atomic logic are not supported.

## 1.5 PCI Controller

The MPC8323E PCI controller includes the following features:

- *PCI Specification Revision 2.3* compatible
- Single 32-bit data PCI interface operates up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

## 1.6 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 35 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

**Table 6. Estimated Typical I/O Power Dissipation (continued)**

| | | | | | | |
|---|---|---|---|---|---|---|
| Local bus I/O<br>load = 25 pF<br>1 pair of clocks | 66 MHz, 32 bits | — | — | 0.12 | W | — |
| PCI I/O load = 30 pF | 66 MHz, 32 bits | — | — | 0.057 | W | — |
| QUICC Engine block and other I/Os | UTOPIA 8-bit 31 PHYs | — | — | 0.041 | W | Multiply by number of interfaces used. |
| | TDM serial | — | — | 0.001 | W | |
| | TDM nibble | — | — | 0.004 | W | |
| | HDLC/TRAN serial | — | — | 0.003 | W | |
| | HDLC/TRAN nibble | — | — | 0.025 | W | |
| | DUART | — | — | 0.017 | W | |
| | MIIs | — | — | 0.009 | W | |
| | RMII | — | — | 0.009 | W | |
| | Ethernet management | — | — | 0.002 | W | |
| | USB | — | — | 0.001 | W | |
| | SPI | — | — | 0.001 | W | |
| | Timer output | — | — | 0.002 | W | |

**NOTE**

$AV_{DD}n$ (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

# 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

**NOTE**

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

## 4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

**Table 7. CLKIN DC Electrical Characteristics**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | — | $V_{IH}$ | 2.7 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | — | $V_{IL}$ | –0.3 | 0.4 | V |

## 6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR1 and DDR2 SDRAM interface.

### 6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM (D*n*_$GV_{DD}$(typ) = 1.8 V).

**Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions with D*n*_$GV_{DD}$ of 1.8 ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | MVREF$n_{REF}$ – 0.25 | V | — |
| AC input high voltage | $V_{IH}$ | MVREF$n_{REF}$ + 0.25 | — | V | — |

Table 17 provides the input AC timing specifications for the DDR1 SDRAM (D*n*_$GV_{DD}$(typ) = 2.5 V).

**Table 17. DDR1 SDRAM Input AC Timing Specifications for 2.5 V Interface**

At recommended operating conditions with D*n*_$GV_{DD}$ of 2.5 ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | MVREF$n_{REF}$ – 0.31 | V | — |
| AC input high voltage | $V_{IH}$ | MVREF$n_{REF}$ + 0.31 | — | V | — |

Table 18 provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

**Table 18. DDR1 and DDR2 SDRAM Input AC Timing Specifications**

At recommended operating conditions with D*n*_$GV_{DD}$ of (1.8 or 2.5 V) ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Controller skew for MDQS—MDQ/MDM | $t_{CISKEW}$ | | | ps | 1, 2 |
| 266 MHz | | –750 | 750 | | |
| 200 MHz | | –1250 | 1250 | | |

**Notes:**

1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called $t_{DISKEW}$. This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of $t_{CISKEW}$.

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8323E.

## 7.1 DUART DC Electrical Characteristics

Table 20 provides the DC electrical characteristics for the DUART interface of the MPC8323E.

**Table 20. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage $OV_{DD}$ | $V_{IL}$ | –0.3 | 0.8 | V |
| High-level output voltage, $I_{OH}$ = –100 µA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 µA | $V_{OL}$ | — | 0.2 | V |
| Input current (0 V ≤ $V_{IN}$ ≤ $OV_{DD}$)[1] | $I_{IN}$ | — | ±5 | µA |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 7.2 DUART AC Electrical Specifications

Table 21 provides the AC timing parameters for the DUART interface of the MPC8323E.

**Table 21. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | 256 | baud | |
| Maximum baud rate | > 1,000,000 | baud | 1 |
| Oversample rate | 16 | — | 2 |

**Notes:**
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8$^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16$^{th}$ sample.

# 8 Ethernet and MII Management

This section provides the AC and DC electrical characteristics for Ethernet and MII management.

## 8.1 Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics

The electrical characteristics specified here apply to all MII (media independent interface) and RMII (reduced media independent interface), except MDIO (management data input/output) and MDC

### 8.2.2.1 RMII Transmit AC Timing Specifications

Table 23 provides the RMII transmit AC timing specifications.

**Table 25. RMII Transmit AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| REF_CLK clock | $t_{RMX}$ | — | 20 | — | ns |
| REF_CLK duty cycle | $t_{RMXH}/t_{RMX}$ | 35 | — | 65 | % |
| REF_CLK to RMII data TXD[1:0], TX_EN delay | $t_{RMTKHDX}$ | 2 | — | 10 | ns |
| REF_CLK data clock rise $V_{IL}$(min) to $V_{IH}$(max) | $t_{RMXR}$ | 1.0 | — | 4.0 | ns |
| REF_CLK data clock fall $V_{IH}$(max) to $V_{IL}$(min) | $t_{RMXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time $t_{RMX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{RMX}$ represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the RMII transmit AC timing diagram.

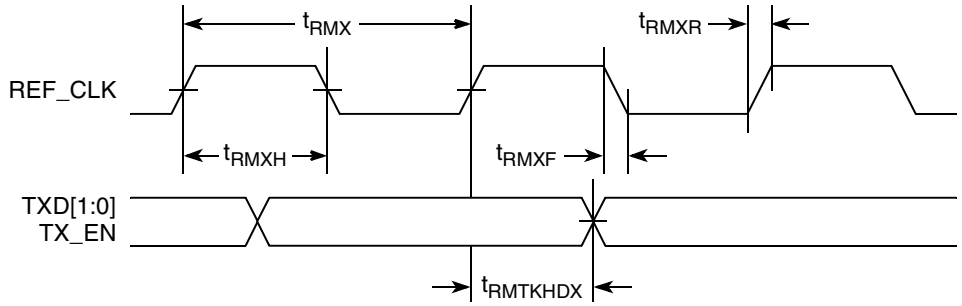



**Figure 10. RMII Transmit AC Timing Diagram**

### 8.2.2.2 RMII Receive AC Timing Specifications

Table 24 provides the RMII receive AC timing specifications.

**Table 26. RMII Receive AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| REF_CLK clock period | $t_{RMX}$ | — | 20 | — | ns |
| REF_CLK duty cycle | $t_{RMXH}/t_{RMX}$ | 35 | — | 65 | % |
| RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK | $t_{RMRDVKH}$ | 4.0 | — | — | ns |
| RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK | $t_{RMRDXKH}$ | 2.0 | — | — | ns |
| REF_CLK clock rise $V_{IL}$(min) to $V_{IH}$(max) | $t_{RMXR}$ | 1.0 | — | 4.0 | ns |

# 11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

## 11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

**Table 33. I²C DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 10%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage level | $V_{IH}$ | $0.7 \times OV_{DD}$ | $OV_{DD} + 0.3$ | V | — |
| Input low voltage level | $V_{IL}$ | –0.3 | $0.3 \times OV_{DD}$ | V | — |
| Low level output voltage | $V_{OL}$ | 0 | 0.4 | V | 1 |
| Output fall time from $V_{IH}$(min) to $V_{IL}$(max) with a bus capacitance from 10 to 400 pF | $t_{I2KLKV}$ | $20 + 0.1 \times C_B$ | 250 | ns | 2 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 3 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |
| Input current ($0 V \le V_{IN} \le OV_{DD}$) | $I_{IN}$ | — | ±5 | μA | 4 |

**Notes:**
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. $C_B$ = capacitance of one bus line in pF.
3. Refer to the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if $OV_{DD}$ is switched off.

## 11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I²C interface of the MPC8323E.

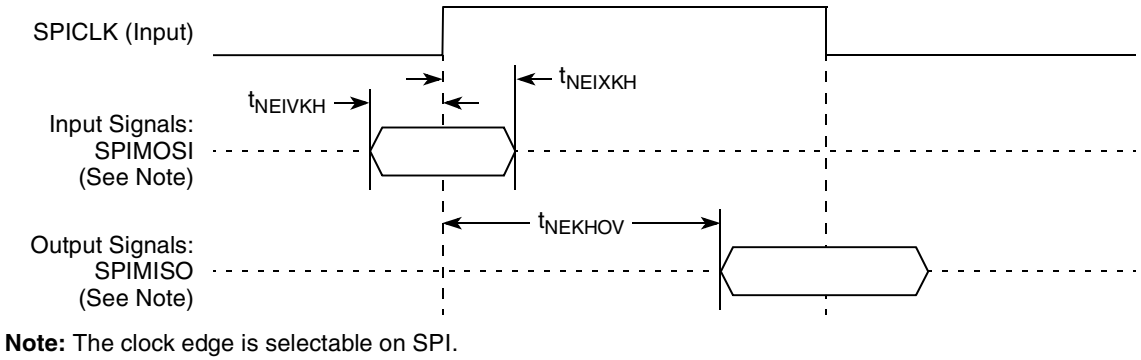
**Table 34. I²C AC Electrical Specifications**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 33).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz |
| Low period of the SCL clock | $t_{I2CL}$ | 1.3 | — | μs |
| High period of the SCL clock | $t_{I2CH}$ | 0.6 | — | μs |
| Setup time for a repeated START condition | $t_{I2SVKH}$ | 0.6 | — | μs |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6 | — | μs |
| Data setup time | $t_{I2DVKH}$ | 100 | — | ns |
| Data hold time: CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | —<br>0[2] | —<br>0.9[3] | μs |

Figure 31 and Figure 32 represent the AC timing from Table 45. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

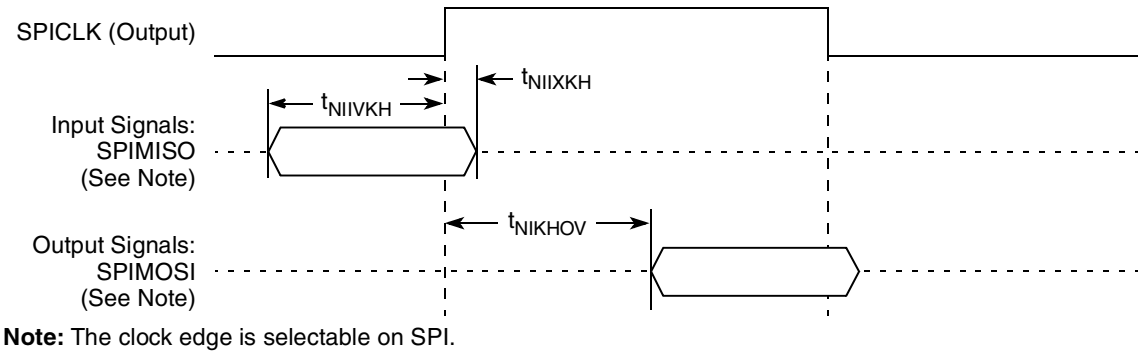
Figure 31 shows the SPI timing in slave mode (external clock).




**Note:** The clock edge is selectable on SPI.

**Figure 31. SPI AC Timing in Slave Mode (External Clock) Diagram**

Figure 32 shows the SPI timing in master mode (internal clock).




**Note:** The clock edge is selectable on SPI.

**Figure 32. SPI AC Timing in Master Mode (Internal Clock) Diagram**

# 17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8323E.

## 17.1 TDM/SI DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the MPC8323E TDM/SI.

**Table 46. TDM/SI DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –2.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.5 | V |
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |

**Table 46. TDM/SI DC Electrical Characteristics (continued)**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le OV_{DD}$ | — | ±5 | μA |

## 17.2 TDM/SI AC Timing Specifications

Table 47 provides the TDM/SI input and output AC timing specifications.

**Table 47. TDM/SI AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Max | Unit |
|---|---|---|---|---|
| TDM/SI outputs—External clock delay | $t_{SEKHOV}$ | 2 | 12 | ns |
| TDM/SI outputs—External clock High Impedance | $t_{SEKHOX}$ | 2 | 10 | ns |
| TDM/SI inputs—External clock input setup time | $t_{SEIVKH}$ | 5 | — | ns |
| TDM/SI inputs—External clock input hold time | $t_{SEIXKH}$ | 2 | — | ns |

**Notes:**
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SEKHOX}$ symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 33 provides the AC test load for the TDM/SI.

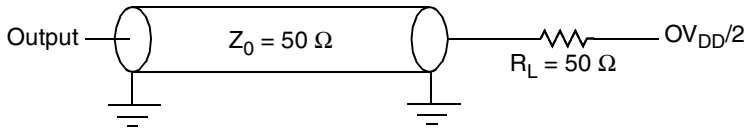
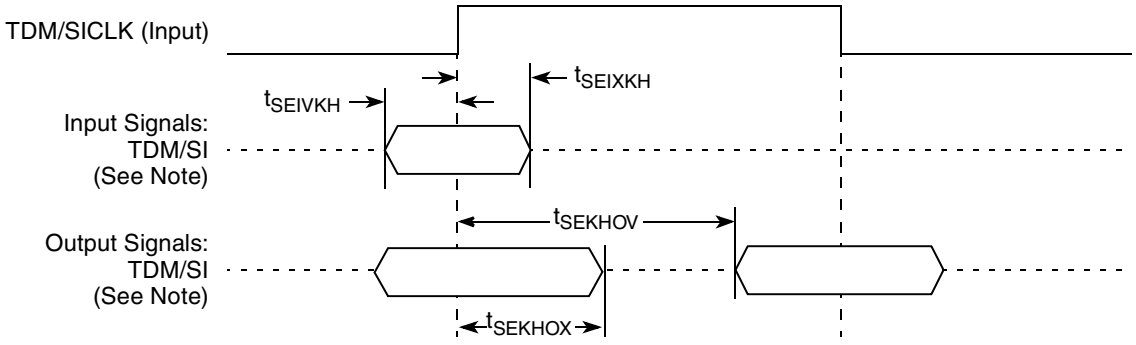



**Figure 33. TDM/SI AC Test Load**

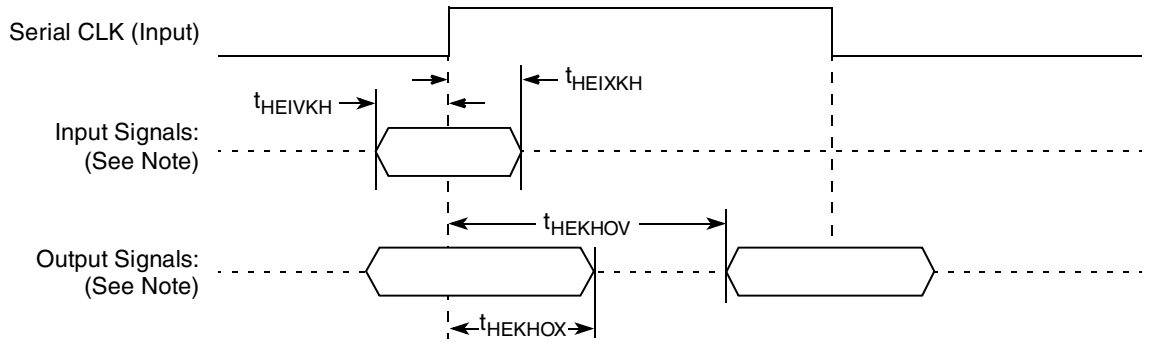
Figure 34 represents the AC timing from Table 47. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.




**Note:** The clock edge is selectable on TDM/SI.

**Figure 34. TDM/SI AC Timing (External Clock) Diagram**

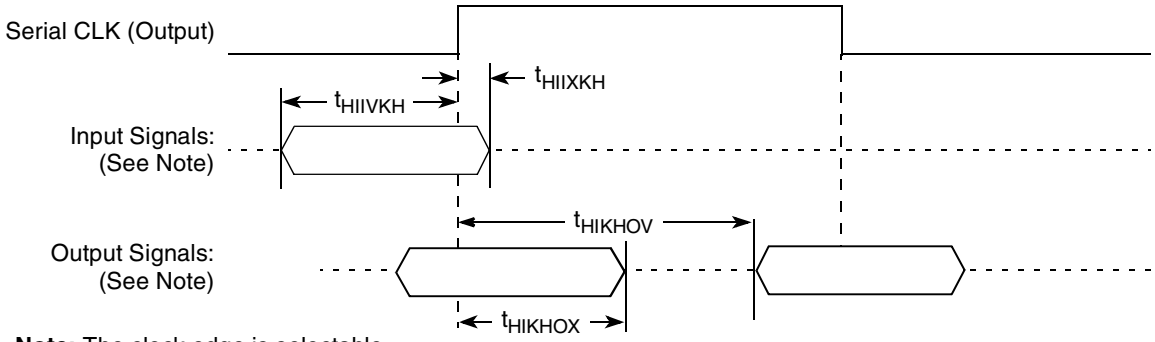
Figure 39 shows the timing with external clock.




**Note:** The clock edge is selectable.

**Figure 39. AC Timing (External Clock) Diagram**

Figure 40 shows the timing with internal clock.




**Note:** The clock edge is selectable.

**Figure 40. AC Timing (Internal Clock) Diagram**

# 20 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8323E.

## 20.1 USB DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the USB interface.

**Table 53. USB DC Electrical Characteristics[1]**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| High-level output voltage, $I_{OH}$ = –100 µA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 µA | $V_{OL}$ | — | 0.2 | V |
| Input current | $I_{IN}$ | — | ±5 | µA |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 20.2 USB AC Electrical Specifications

Table 54 describes the general timing parameters of the USB interface of the MPC8323E.

**Table 54. USB General Timing Parameters**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| USB clock cycle time | $t_{USCK}$ | 20.83 | — | ns | Full speed 48 MHz |
| USB clock cycle time | $t_{USCK}$ | 166.67 | — | ns | Low speed 6 MHz |
| Skew between TXP and TXN | $t_{USTSPN}$ | — | 5 | ns | — |
| Skew among RXP, RXN, and RXD | $t_{USRSPND}$ | — | 10 | ns | Full speed transitions |
| Skew among RXP, RXN, and RXD | $t_{USRPND}$ | — | 100 | ns | Low speed transitions |

**Notes:**
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(state)(signal)}}$ for receive signals and $t_{\text{(first two letters of functional block)(state)(signal)}}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, $t_{USTSPN}$ symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

Figure 41 provide the AC test load for the USB.

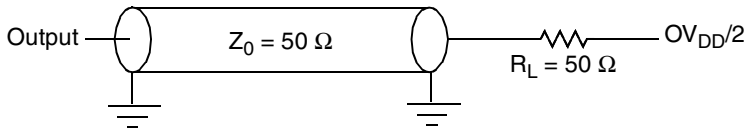



**Figure 41. USB AC Test Load**

## 21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

**Table 55. MPC8323E PBGA Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **DDR Memory Controller Interface** | | | | |
| MEMC_MDQ0 | AE9 | IO | $GV_{DD}$ | — |
| MEMC_MDQ1 | AD10 | IO | $GV_{DD}$ | — |
| MEMC_MDQ2 | AF10 | IO | $GV_{DD}$ | — |
| MEMC_MDQ3 | AF9 | IO | $GV_{DD}$ | — |
| MEMC_MDQ4 | AF7 | IO | $GV_{DD}$ | — |
| MEMC_MDQ5 | AE10 | IO | $GV_{DD}$ | — |
| MEMC_MDQ6 | AD9 | IO | $GV_{DD}$ | — |
| MEMC_MDQ7 | AF8 | IO | $GV_{DD}$ | — |
| MEMC_MDQ8 | AE6 | IO | $GV_{DD}$ | — |
| MEMC_MDQ9 | AD7 | IO | $GV_{DD}$ | — |
| MEMC_MDQ10 | AF6 | IO | $GV_{DD}$ | — |
| MEMC_MDQ11 | AC7 | IO | $GV_{DD}$ | — |
| MEMC_MDQ12 | AD8 | IO | $GV_{DD}$ | — |
| MEMC_MDQ13 | AE7 | IO | $GV_{DD}$ | — |
| MEMC_MDQ14 | AD6 | IO | $GV_{DD}$ | — |
| MEMC_MDQ15 | AF5 | IO | $GV_{DD}$ | — |
| MEMC_MDQ16 | AD18 | IO | $GV_{DD}$ | — |
| MEMC_MDQ17 | AE19 | IO | $GV_{DD}$ | — |
| MEMC_MDQ18 | AF17 | IO | $GV_{DD}$ | — |
| MEMC_MDQ19 | AF19 | IO | $GV_{DD}$ | — |
| MEMC_MDQ20 | AF18 | IO | $GV_{DD}$ | — |
| MEMC_MDQ21 | AE18 | IO | $GV_{DD}$ | — |
| MEMC_MDQ22 | AF20 | IO | $GV_{DD}$ | — |
| MEMC_MDQ23 | AD19 | IO | $GV_{DD}$ | — |
| MEMC_MDQ24 | AD21 | IO | $GV_{DD}$ | — |
| MEMC_MDQ25 | AF22 | IO | $GV_{DD}$ | — |
| MEMC_MDQ26 | AC21 | IO | $GV_{DD}$ | — |
| MEMC_MDQ27 | AF21 | IO | $GV_{DD}$ | — |
| MEMC_MDQ28 | AE21 | IO | $GV_{DD}$ | — |

**Table 55. MPC8323E PBGA Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| MEMC_MDQ29 | AD20 | IO | $GV_{DD}$ | — |
| MEMC_MDQ30 | AF23 | IO | $GV_{DD}$ | — |
| MEMC_MDQ31 | AD22 | IO | $GV_{DD}$ | — |
| MEMC_MDM0 | AC9 | O | $GV_{DD}$ | — |
| MEMC_MDM1 | AD5 | O | $GV_{DD}$ | — |
| MEMC_MDM2 | AE20 | O | $GV_{DD}$ | — |
| MEMC_MDM3 | AE22 | O | $GV_{DD}$ | — |
| MEMC_MDQS0 | AE8 | IO | $GV_{DD}$ | — |
| MEMC_MDQS1 | AE5 | IO | $GV_{DD}$ | — |
| MEMC_MDQS2 | AC19 | IO | $GV_{DD}$ | — |
| MEMC_MDQS3 | AE23 | IO | $GV_{DD}$ | — |
| MEMC_MBA0 | AD16 | O | $GV_{DD}$ | — |
| MEMC_MBA1 | AD17 | O | $GV_{DD}$ | — |
| MEMC_MBA2 | AE17 | O | $GV_{DD}$ | — |
| MEMC_MA0 | AD12 | O | $GV_{DD}$ | — |
| MEMC_MA1 | AE12 | O | $GV_{DD}$ | — |
| MEMC_MA2 | AF12 | O | $GV_{DD}$ | — |
| MEMC_MA3 | AC13 | O | $GV_{DD}$ | — |
| MEMC_MA4 | AD13 | O | $GV_{DD}$ | — |
| MEMC_MA5 | AE13 | O | $GV_{DD}$ | — |
| MEMC_MA6 | AF13 | O | $GV_{DD}$ | — |
| MEMC_MA7 | AC15 | O | $GV_{DD}$ | — |
| MEMC_MA8 | AD15 | O | $GV_{DD}$ | — |
| MEMC_MA9 | AE15 | O | $GV_{DD}$ | — |
| MEMC_MA10 | AF15 | O | $GV_{DD}$ | — |
| MEMC_MA11 | AE16 | O | $GV_{DD}$ | — |
| MEMC_MA12 | AF16 | O | $GV_{DD}$ | — |
| MEMC_MA13 | AB16 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MWE}}$ | AC17 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MRAS}}$ | AE11 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MCAS}}$ | AD11 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MCS}}$ | AC11 | O | $GV_{DD}$ | — |

**Table 55. MPC8323E PBGA Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **CE/GPIO** | | | | |
| GPIO_PA0/SER1_TXD[0]/TDMA_TXD[0]/USBTXN | G3 | IO | $OV_{DD}$ | — |
| GPIO_PA1/SER1_TXD[1]/TDMA_TXD[1]/USBTXP | F3 | IO | $OV_{DD}$ | — |
| GPIO_PA2/SER1_TXD[2]/TDMA_TXD[2] | F2 | IO | $OV_{DD}$ | — |
| GPIO_PA3/SER1_TXD[3]/TDMA_TXD[3] | E3 | IO | $OV_{DD}$ | — |
| GPIO_PA4/SER1_RXD[0]/TDMA_RXD[0]/USBRXP | E2 | IO | $OV_{DD}$ | — |
| GPIO_PA5/SER1_RXD[1]/TDMA_RXD[1]/USBRXN | E1 | IO | $OV_{DD}$ | — |
| GPIO_PA6/SER1_RXD[2]/TDMA_RXD[2]/USBRXD | D3 | IO | $OV_{DD}$ | — |
| GPIO_PA7/SER1_RXD[3]/TDMA_RXD[3] | D2 | IO | $OV_{DD}$ | — |
| GPIO_PA8/SER1_CD/TDMA_REQ/$\overline{\text{USBOE}}$ | D1 | IO | $OV_{DD}$ | — |
| GPIO_PA9 TDMA_CLKO | C3 | IO | $OV_{DD}$ | — |
| GPIO_PA10/SER1_CTS/TDMA_RSYNC | C2 | IO | $OV_{DD}$ | — |
| GPIO_PA11/TDMA_STROBE | C1 | IO | $OV_{DD}$ | — |
| GPIO_PA12/SER1_RTS/TDMA_TSYNC | B1 | IO | $OV_{DD}$ | — |
| GPIO_PA13/CLK9/BRGO9 | H4 | IO | $OV_{DD}$ | — |
| GPIO_PA14/CLK11/BRGO10 | G4 | IO | $OV_{DD}$ | — |
| GPIO_PA15/BRGO7 | J4 | IO | $OV_{DD}$ | — |
| GPIO_PA16/ LA0 (LBIU) | K24 | IO | $OV_{DD}$ | — |
| GPIO_PA17/ LA1 (LBIU) | K26 | IO | $OV_{DD}$ | — |
| GPIO_PA18/Enet2_TXD[0]/SER2_TXD[0]/ TDMB_TXD[0]/LA2 (LBIU) | G25 | IO | $OV_{DD}$ | — |
| GPIO_PA19/Enet2_TXD[1]/SER2_TXD[1]/ TDMB_TXD[1]/LA3 (LBIU) | G26 | IO | $OV_{DD}$ | — |
| GPIO_PA20/Enet2_TXD[2]/SER2_TXD[2]/ TDMB_TXD[2]/LA4 (LBIU) | H25 | IO | $OV_{DD}$ | — |
| GPIO_PA21/Enet2_TXD[3]/SER2_TXD[3]/ TDMB_TXD[3]/LA5 (LBIU) | H26 | IO | $OV_{DD}$ | — |
| GPIO_PA22/Enet2_RXD[0]/SER2_RXD[0]/ TDMB_RXD[0]/LA6 (LBIU) | C25 | IO | $OV_{DD}$ | — |
| GPIO_PA23/Enet2_RXD[1]/SER2_RXD[1]/ TDMB_RXD[1]/LA7 (LBIU) | C26 | IO | $OV_{DD}$ | — |
| GPIO_PA24/Enet2_RXD[2]/SER2_RXD[2]/ TDMB_RXD[2]/LA8 (LBIU) | D25 | IO | $OV_{DD}$ | — |
| GPIO_PA25/Enet2_RXD[3]/SER2_RXD[3]/ TDMB_RXD[3]/LA9 (LBIU) | D26 | IO | $OV_{DD}$ | — |

**Table 55. MPC8323E PBGA Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| GPIO_PD10/GTM1_TIN2/GTM2_TIN1/CLK17 | J24 | IO | $OV_{DD}$ | — |
| GPIO_PD11/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$ | B25 | IO | $OV_{DD}$ | — |
| GPIO_PD12/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$ | C4 | IO | $OV_{DD}$ | — |
| GPIO_PD13/GTM1_TIN3/GTM2_TIN4/BRGO8 | D4 | IO | $OV_{DD}$ | — |
| GPIO_PD14/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$ | D5 | IO | $OV_{DD}$ | — |
| GPIO_PD15/$\overline{\text{GTM1\_TOUT3}}$ | A5 | IO | $OV_{DD}$ | — |
| GPIO_PD16/GTM1_TIN4/GTM2_TIN3 | B5 | IO | $OV_{DD}$ | — |
| GPIO_PD17/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$ | C5 | IO | $OV_{DD}$ | — |
| GPIO_PD18/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$ | A6 | IO | $OV_{DD}$ | — |
| GPIO_PD19/CE_RISC1_INT/CE_EXT_REQ4 | B6 | IO | $OV_{DD}$ | — |
| GPIO_PD20/CLK18/BRGO6 | D21 | IO | $OV_{DD}$ | — |
| GPIO_PD21/CLK16/BRGO5/UPC1_CLKO | C19 | IO | $OV_{DD}$ | — |
| GPIO_PD22/CLK4/BRGO9/UCC2_CLKO | A7 | IO | $OV_{DD}$ | — |
| GPIO_PD23/CLK3/BRGO10/UCC3_CLKO | B7 | IO | $OV_{DD}$ | — |
| GPIO_PD24/CLK10/BRGO2/UCC4_CLKO | A12 | IO | $OV_{DD}$ | — |
| GPIO_PD25/CLK13/BRGO16/UCC5_CLKO | B10 | IO | $OV_{DD}$ | — |
| GPIO_PD26/CLK2/BRGO4/UCC1_CLKO | E4 | IO | $OV_{DD}$ | — |
| GPIO_PD27/CLK1/BRGO3 | F4 | IO | $OV_{DD}$ | — |
| GPIO_PD28/CLK19/BRGO11 | D15 | IO | $OV_{DD}$ | — |
| GPIO_PD29/CLK15/BRGO8 | C6 | IO | $OV_{DD}$ | — |
| GPIO_PD30/CLK14 | D6 | IO | $OV_{DD}$ | — |
| GPIO_PD31/CLK7/BRGO15 | E24 | IO | $OV_{DD}$ | — |
| **Power and Ground Supplies** | | | | |
| $GV_{DD}$ | AA8, AA10, AA11, AA13, AA14, AA16, AA17, AA19, AA21, AB9, AB10, AB11, AB12, AB14, AB18, AB20, AB21, AC6, AC8, AC14, AC18 | $GV_{DD}$ | — | — |
| $OV_{DD}$ | E5, E6, E8, E9, E10, E12, E14, E15, E16, E18, E19, E20, E22, F5, F6, F8, F10, F14, F16, F19, F22, G22, H5, H6, H21, J5, J22, K21, K22, L5, L6, L22, M5, M22, N5, N21, N22, P6, P22, P23, R5, R23, T5, T21, T22, U6, U22, V5, V22, W22, Y5, AB5, AB6, AC5 | $OV_{DD}$ | — | — |

**Table 55. MPC8323E PBGA Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $V_{DD}$ | K10, K11, K12, K13, K14, K15, K16, K17, L10, L17, M10, M17, N10, N17, P10, P17, R10, R17, T10, T17, U10, U11, U12, U13, U14, U15, U16, U17 | $V_{DD}$ | — | — |
| $V_{SS}$ | B23, E7, E11, E13, E17, E21, F11, F13, F17, F21, F23, G5, H22, K5, K6, L11, L12, L13, L14, L15, L16, L21, M11, M12, M13, M14, M15, M16, N6, N11, N12, N13, N14, N15, N16, P5, P11, P12, P13, P14, P15, P16, P21, R11, R12, R13, R14, R15, R16, R22, T6, T11, T12, T13, T14, T15, T16, U5, U21, V23, W5, W6, W21, W23, W24, Y22, AA5, AA6, AA22, AA25, AB7, AB13, AB19, AB22, AC10, AC12, AC16, AC20 | $V_{SS}$ | — | — |
| **No Connect** | | | | |
| NC | C22 | — | — | — |

**Notes:**
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to $OV_{DD}$.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to $OV_{DD}$.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG and local bus pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow the PCI specification's recommendation.
6. This pin must always be tied to GND. 7.This pin has weak internal pull-down N-FET that is always enabled.8.Though this pin has weak internal pull-up yet it is recommended to apply an external pull-up.

# 22 Clocking

Figure 43 shows the internal distribution of clocks within the MPC8323E.

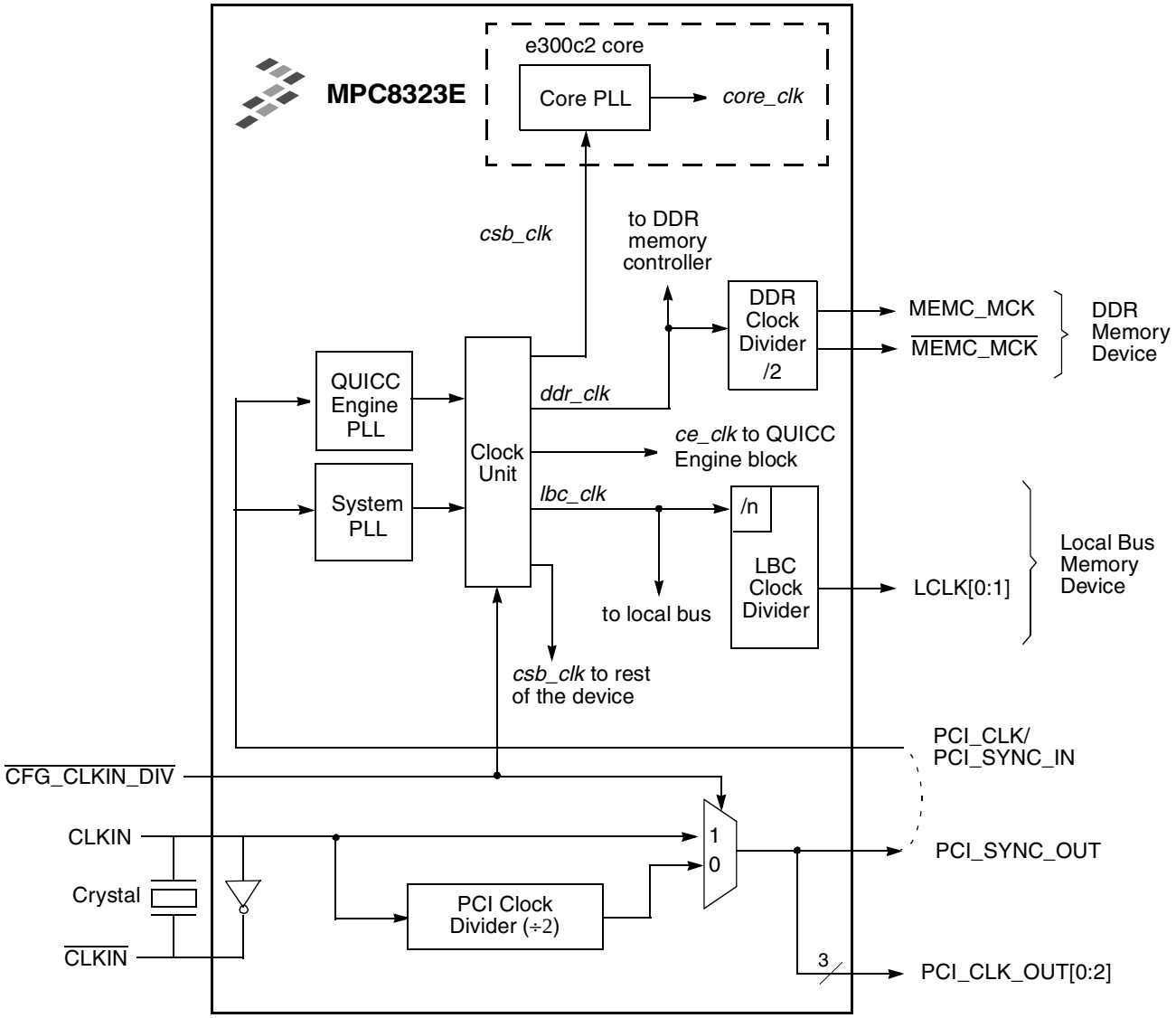



**Figure 43. MPC8323E Clock Subsystem**

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode, respectively.

**Table 57. Operating Frequencies for PBGA (continued)**

| Characteristic[1] | Max Operating Frequency | Unit |
|---|---|---|
| DDR1/DDR2 memory bus frequency (MCLK)[2] | 133 | MHz |
| Local bus frequency (LCLK*n*)[3] | 66 | MHz |
| PCI input frequency (CLKIN or PCI_CLK) | 66 | MHz |

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2 The DDR1/DDR2 data rate is 2× the DDR1/DDR2 memory bus frequency.
3 The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

## 22.4 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

**NOTE**

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 300–600 MHz.

**Table 58. System PLL Multiplication Factors**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 0000 | Reserved |
| 0001 | Reserved |
| 0010 | × 2 |
| 0011 | × 3 |
| 0100 | × 4 |
| 0101 | × 5 |
| 0110 | × 6 |
| 0111–1111 | Reserved |

As described in Section 22, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG\_CLKIN\_DIV}}$ configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59

shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

**Table 59. CSB Frequency Options**

| CFG_CLKIN_DIV_B at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio [2] | Input Clock Frequency (MHz)[2] | | |
|---|---|---|---|---|---|
| | | | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | |
| High | 0010 | 2 : 1 | | | 133 |
| High | 0011 | 3 : 1 | | 100 | |
| High | 0100 | 4 : 1 | 100 | 133 | |
| High | 0101 | 5 : 1 | 125 | | |
| High | 0110 | 6 : 1 | | | |
| High | 0111 | 7 : 1 | | | |
| High | 1000 | 8 : 1 | | | |
| High | 1001 | 9 : 1 | | | |
| High | 1010 | 10 : 1 | | | |
| High | 1011 | 11 : 1 | | | |
| High | 1100 | 12 : 1 | | | |
| High | 1101 | 13 : 1 | | | |
| High | 1110 | 14 : 1 | | | |
| High | 1111 | 15 : 1 | | | |
| High | 0000 | 16 : 1 | | | |
| Low | 0010 | 2 : 1 | | | 133 |
| Low | 0011 | 3 : 1 | | 100 | |
| Low | 0100 | 4 : 1 | | 133 | |
| Low | 0101 | 5 : 1 | | | |
| Low | 0110 | 6 : 1 | | | |
| Low | 0111 | 7 : 1 | | | |
| Low | 1000 | 8 : 1 | | | |
| Low | 1001 | 9 : 1 | | | |
| Low | 1010 | 10 : 1 | | | |
| Low | 1011 | 11 : 1 | | | |
| Low | 1100 | 12 : 1 | | | |
| Low | 1101 | 13 : 1 | | | |
| Low | 1110 | 14 : 1 | | | |
| Low | 1111 | 15 : 1 | | | |
| Low | 0000 | 16 : 1 | | | |

1 CFG_CLKIN_DIV_B is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV_B must be pulled up (high) in agent mode.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

## 22.7 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8323E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 63 shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

**Table 63. Suggested PLL Configurations**

| Conf No. | SPMF | Core PLL | CEMF | CEDF | Input Clock Frequency (MHz) | CSB Frequency (MHz) | Core Frequency (MHz) | QUICC Engine Frequency (MHz) |
|---|---|---|---|---|---|---|---|---|
| **1** | 0100 | 0000100 | 0110 | 0 | 33.33 | 133.33 | 266.66 | 200 |
| **2** | 0100 | 0000101 | 1000 | 0 | 25 | 100 | 250 | 200 |
| **3** | 0010 | 0000100 | 0011 | 0 | 66.67 | 133.33 | 266.66 | 200 |
| **4** | 0100 | 0000101 | 0110 | 0 | 33.33 | 133.33 | 333.33 | 200 |
| **5** | 0101 | 0000101 | 1000 | 0 | 25 | 125 | 312.5 | 200 |
| **6** | 0010 | 0000101 | 0011 | 0 | 66.67 | 133.33 | 333.33 | 200 |

# 23 Thermal

This section describes the thermal specifications of the MPC8323E.

## 23.1 Thermal Characteristics

Table 64 provides the package thermal characteristics for the 516 $27 \times 27$ mm PBGA of the MPC8323E.

**Table 64. Package Thermal Characteristics for PBGA**

| Characteristic | Board type | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction-to-ambient natural convection | Single-layer board (1s) | $R_{\theta JA}$ | 28 | °C/W | 1, 2 |
| Junction-to-ambient natural convection | Four-layer board (2s2p) | $R_{\theta JA}$ | 21 | °C/W | 1, 2, 3 |
| Junction-to-ambient (@200 ft/min) | Single-layer board (1s) | $R_{\theta JMA}$ | 23 | °C/W | 1, 3 |
| Junction-to-ambient (@200 ft/min) | Four-layer board (2s2p) | $R_{\theta JMA}$ | 18 | °C/W | 1, 3 |
| Junction-to-board | — | $R_{\theta JB}$ | 13 | °C/W | 4 |
| Junction-to-case | — | $R_{\theta JC}$ | 9 | °C/W | 5 |

## 25.2 Part Marking

Parts are marked as in the example shown in Figure 46.


**Notes:**
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

**Figure 46. Freescale Part Marking for PBGA Devices**

# 26 Document Revision History

Table 67 provides a revision history for this hardware specification.

**Table 67. Document Revision History**

| Rev. No. | Date | Substantive Change(s) |
|---|---|---|
| 4 | 09/2010 | • Replaced all instances of “LCCR” with “LCRR” throughout.<br>• Added footnotes 3 and 4 in Table 2, “Recommended Operating Conditions[3].”<br>• Modified Section 8.1.1, “DC Electrical Characteristics.”<br>• Modified Table 23, “MII Transmit AC Timing Specifications.”<br>• Modified Table 24, “MII Receive AC Timing Specifications.”<br>• Added footnote 7 and 8, and modified some signal names in Table 55, ”MPC8323E PBGA Pinout Listing.” |
| 3 | 12/2009 | • Removed references for note 4 from Table 1.<br>• Added Figure 2 in Section 2.1.2, “Power Supply Voltage Specification.<br>• Added symbol $T_A$ in Table 2.<br>• Added footnote 2 in Table 2.<br>• Added a note in Section 4, “Clock Input Timing for rise/fall time of QE input pins.<br>• Modified CLKIN, PCI_CLK rise/fall time parameters in Table 8. Modified min value of $t_{MCK}$ in Table 19.<br>• Modified Figure 43.<br>• Modified formula for ce_clk calculation in Section 22.3, “System Clock Domains.<br>• Added a note in Section 22.4, “System PLL Configuration.<br>• Removed the signal ECID_TMODE_IN from Table 55.<br>• Removed all references of RST signals from Table 55. |