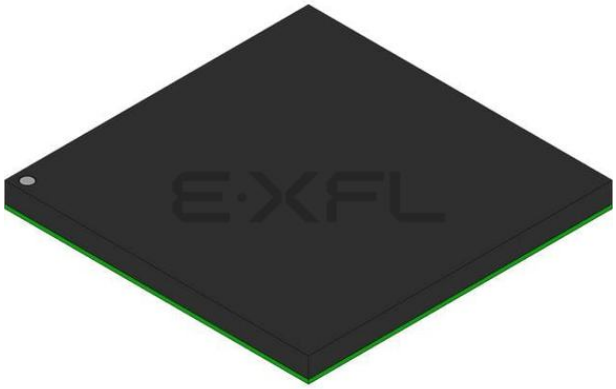

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8323ecvrafdc

1.1.2 Serial Interfaces

The MPC8323E serial interfaces are as follows:

- Support for one UL2 interface with 31 multi-PHY addresses (MPC8323E and MPC8323 only)
- Support for up to three 10/100 Mbps Ethernet interfaces using MII or RMII
- Support for up to four T1/E1/J1/E3 or DS-3 serial interfaces (TDM)
- Support for dual UART and SPI interfaces and a single I^2C interface

1.2 QUICC Engine Block

The QUICC Engine block is a versatile communications complex that integrates several communications peripheral controllers. It provides on-chip system design for a variety of applications, particularly in communications and networking systems. The QUICC Engine block has the following features:

- One 32-bit RISC controller for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
  - 10/100 Mbps Ethernet/IEEE 802.3® standard
  - IP support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
  - ATM protocol through UTOPIA interface (note that the MPC8321 and MPC8321E do not support the UTOPIA interface)
  - HDLC /transparent up to 70-Mbps full-duplex
  - HDLC bus up to 10 Mbps
  - Asynchronous HDLC
  - UART
  - BISYNC up to 2 Mbps
  - QUICC multi-channel controller (QMC) for 64 TDM channels
- One UTOPIA interface (UPC1) supporting 31 multi-PHYs (MPC8323E- and MPC8323-specific)
- Two serial peripheral interfaces (SPI). SPI2 is dedicated to Ethernet PHY management.
- Four TDM interfaces
- Thirteen independent baud rate generators and 19 input clock pins for supplying clocks to UCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

The UCCs are similar to the PowerQUICC II peripherals: SCC (BISYNC, UART, and HDLC bus) and FCC (fast Ethernet, HDLC, transparent, and ATM).

Table 6. Estimated Typical I/O Power Dissipation (continued)

Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 32 bits	—	—	0.12	W	—
PCI I/O load = 30 pF	66 MHz, 32 bits	—	—	0.057	W	—
QUICC Engine block and other I/Os	UTOPIA 8-bit 31 PHYs	—	—	0.041	W	Multiply by number of interfaces used.
	TDM serial	—	—	0.001	W	
	TDM nibble	—	—	0.004	W	
	HDLC/TRAN serial	—	—	0.003	W	
	HDLC/TRAN nibble	—	—	0.025	W	
	DUART	—	—	0.017	W	
	MIIs	—	—	0.009	W	
	RMII	—	—	0.009	W	
	Ethernet management	—	—	0.002	W	
	USB	—	—	0.001	W	
	SPI	—	—	0.001	W	
	Timer output	—	—	0.002	W	

NOTE

$AV_{DD}n$ (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
HRESET/SRESET assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
HRESET negation to SRESET negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8323E is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of HRESET	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of HRESET	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of HRESET	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—

Table 11. Reset Signals DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3 V supply.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR1 and DDR2 SDRAM interface of the MPC8323E. Note that DDR1 SDRAM is D*n*_GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is D*n*_GV_{DD}(typ) = 1.8 V. The AC electrical specifications are the same for DDR1 and DDR2 SDRAM.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8323E when D*n*_GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for D*n*_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MVREFn_{REF}	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	MVREFn_{REF} – 0.04	MVREFn_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MVREFn_{REF} + 0.125	D*n*_GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREFn_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.35 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. MVREFn_{REF} is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREFn_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREFn_{REF}. This rail should track variations in the DC level of MVREFn_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le$ D*n*_GV_{DD}.

Table 13 provides the DDR2 capacitance when D*n*_GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for D*n*_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1

Table 26. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load.

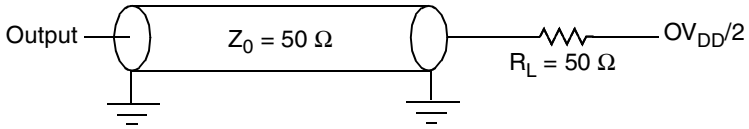


Figure 11. AC Test Load

Figure 12 shows the RMII receive AC timing diagram.

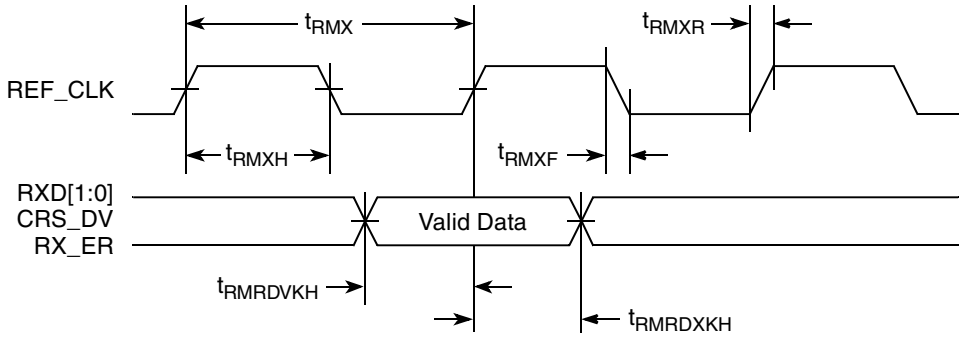


Figure 12. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, “Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics.”

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.10	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII Management AC Electrical Specifications

Table 28 provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 30. Local Bus General Timing Parameters (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock (LCLK*n*) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK*n*) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8
Local bus clock (LCLK*n*) duty cycle	t_{LBDC}	47	53	%	—
Local bus clock (LCLK*n*) jitter specification	t_{LBRJ}	—	400	ps	—
Delay between the input clock (PCI_SYNC_IN) of local bus output clock (LCLK*n*)	t_{LBCDL}	—	1.7	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 14 provides the AC test load for the local bus.

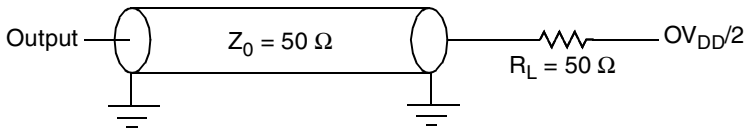


Figure 14. Local Bus C Test Load

Figure 15 through Figure 17 show the local bus signals.

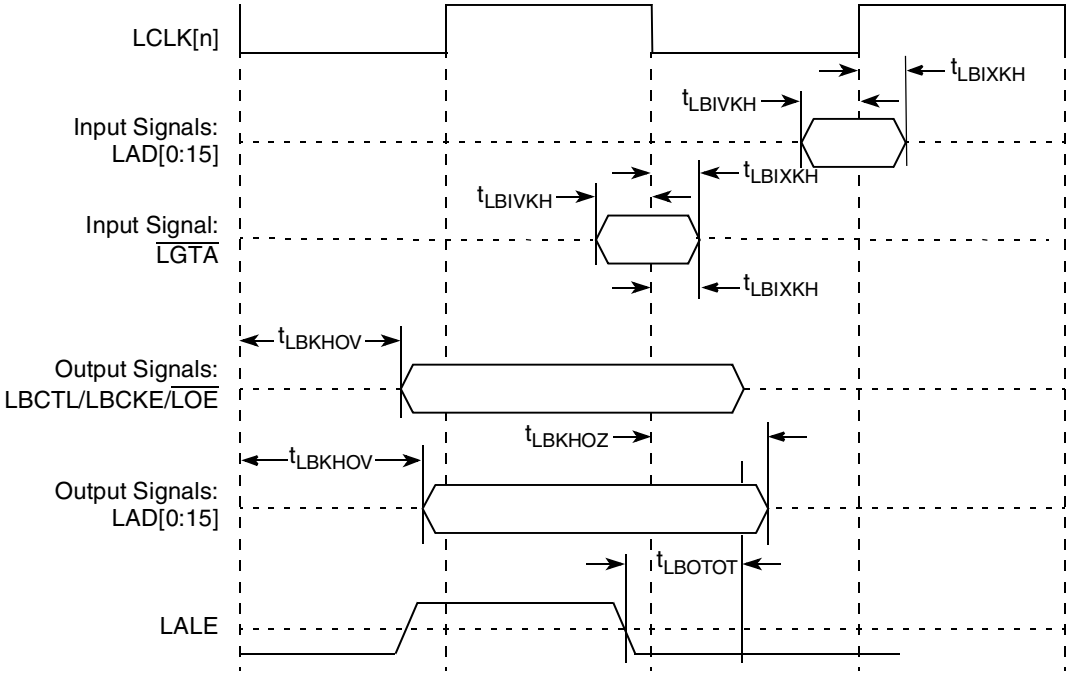


Figure 15. Local Bus Signals, Nonspecial Signals Only

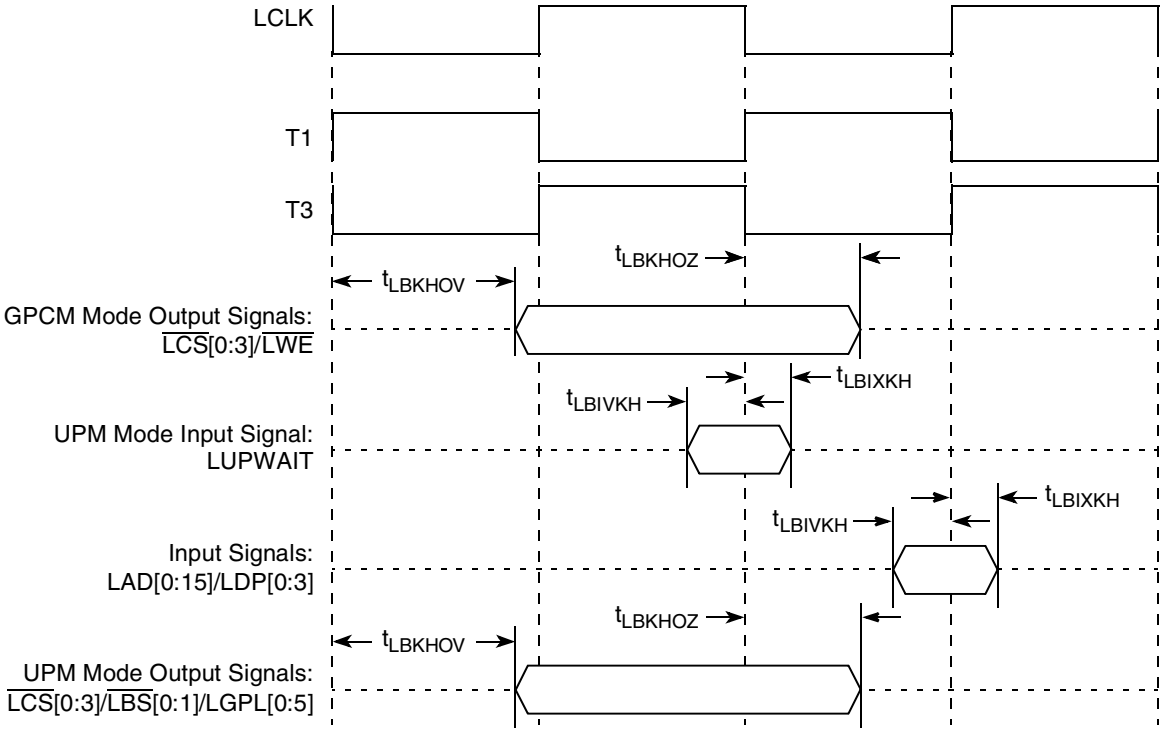


Figure 16. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

Table 33. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I²C interface of the MPC8323E.

Table 34. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0[2]	— 0.9[3]	μs

Table 34. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol[1]	Min	Max	Unit
Rise time of both SDA and SCL signals	t_{I2CR}	20 + 0.1 C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_b[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8323E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

Figure 23 provides the AC test load for the I²C.

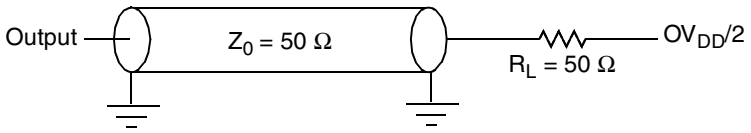


Figure 23. I²C AC Test Load

Figure 24 shows the AC timing diagram for the I²C bus.

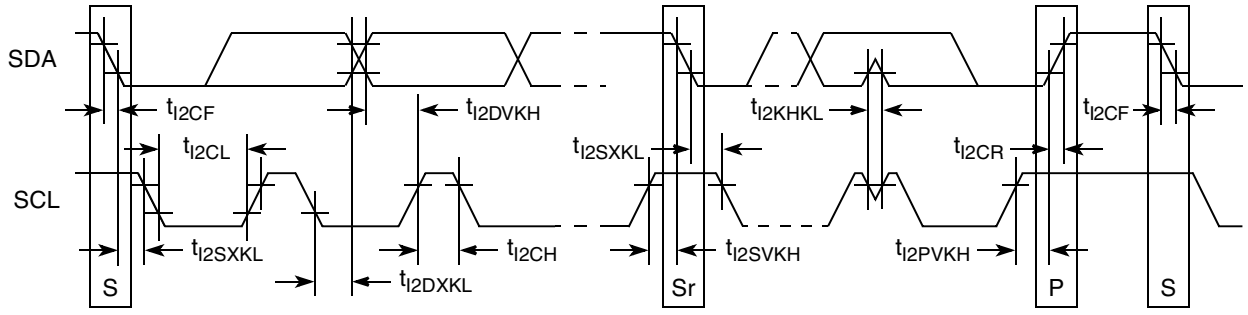


Figure 24. I²C Bus AC Timing Diagram

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Table 44. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 30 provides the AC test load for the SPI.

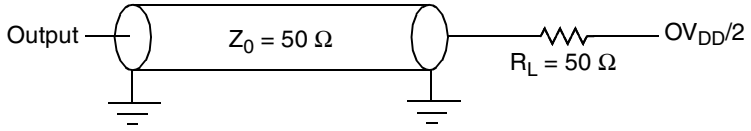


Figure 30. SPI AC Test Load

19 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART of the MPC8323E.

19.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Table 50 provides the DC electrical characteristics for the MPC8323E HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 50. HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

19.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Table 51 provides the input and output AC timing specifications for HDLC, BISYNC, and transparent UART protocols.

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	5.5	ns
Outputs—External clock delay	t_{HEKHOV}	1	10	ns
Outputs—Internal clock high impedance	t_{HIKHOX}	0	5.5	ns
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns

21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8323E is available in a thermally enhanced Plastic Ball Grid Array (PBGA); see Section 21.1, "Package Parameters for the MPC8323E PBGA," and Section 21.2, "Mechanical Dimensions of the MPC8323E PBGA," for information on the PBGA.

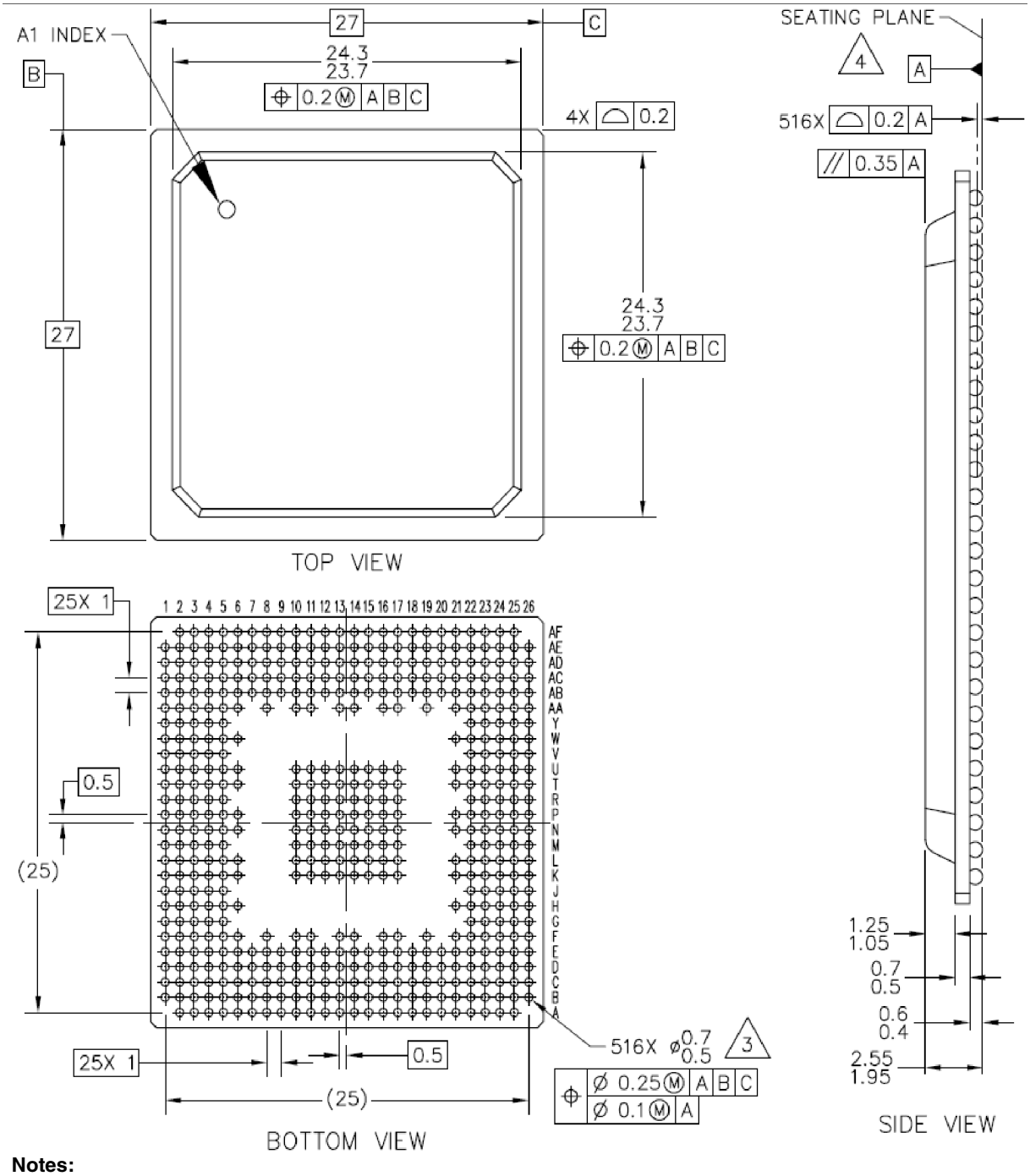
21.1 Package Parameters for the MPC8323E PBGA

The package parameters are as provided in the following list. The package type is 27 mm × 27 mm, 516 PBGA.

Package outline	27 mm × 27 mm
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.6 mm

21.2 Mechanical Dimensions of the MPC8323E PBGA

Figure 42 shows the mechanical dimensions and bottom surface nomenclature of the MPC8323E, 516-PBGA package.



Notes:

1.All dimensions are in millimeters.

2.Dimensions and tolerances per ASME Y14.5M-1994.

3.Maximum solder ball diameter measured parallel to datum A.

4.Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 42. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8323E PBGA

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	O	GV_{DD}	3
MEMC_MCK	AF14	O	GV_{DD}	—
$\overline{\text{MEMC\_MCK}}$	AE14	O	GV_{DD}	—
MEMC_MODT	AF11	O	GV_{DD}	—
Local Bus Controller Interface				
LAD0	N25	IO	OV_{DD}	7
LAD1	P26	IO	OV_{DD}	7
LAD2	P25	IO	OV_{DD}	7
LAD3	R26	IO	OV_{DD}	7
LAD4	R25	IO	OV_{DD}	7
LAD5	T26	IO	OV_{DD}	7
LAD6	T25	IO	OV_{DD}	7
LAD7	U25	IO	OV_{DD}	7
LAD8	M24	IO	OV_{DD}	7
LAD9	N24	IO	OV_{DD}	7
LAD10	P24	IO	OV_{DD}	7
LAD11	R24	IO	OV_{DD}	7
LAD12	T24	IO	OV_{DD}	7
LAD13	U24	IO	OV_{DD}	7
LAD14	U26	IO	OV_{DD}	7
LAD15	V26	IO	OV_{DD}	7
LA16	K25	O	OV_{DD}	7
LA17	L25	O	OV_{DD}	7
LA18	L26	O	OV_{DD}	7
LA19	L24	O	OV_{DD}	7
LA20	M26	O	OV_{DD}	7
LA21	M25	O	OV_{DD}	7
LA22	N26	O	OV_{DD}	7
LA23	AC24	O	OV_{DD}	7
LA24	AC25	O	OV_{DD}	7
LA25	AB23	O	OV_{DD}	7
$\overline{\text{LCS0}}$	AB24	O	OV_{DD}	4

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_AD20	AB2	IO	OV_{DD}	—
PCI_AD21	Y4	IO	OV_{DD}	—
PCI_AD22	AC1	IO	OV_{DD}	—
PCI_AD23	AA3	IO	OV_{DD}	—
PCI_AD24	AA4	IO	OV_{DD}	—
PCI_AD25	AD1	IO	OV_{DD}	—
PCI_AD26	AD2	IO	OV_{DD}	—
PCI_AD27	AB3	IO	OV_{DD}	—
PCI_AD28	AB4	IO	OV_{DD}	—
PCI_AD29	AE1	IO	OV_{DD}	—
PCI_AD30	AC3	IO	OV_{DD}	—
PCI_AD31	AC4	IO	OV_{DD}	—
PCI_C_$\overline{BE0}$	M4	IO	OV_{DD}	—
PCI_C_$\overline{BE1}$	T4	IO	OV_{DD}	—
PCI_C_$\overline{BE2}$	Y3	IO	OV_{DD}	—
PCI_C_$\overline{BE3}$	AC2	IO	OV_{DD}	—
PCI_PAR	U3	IO	OV_{DD}	—
$\overline{PCI\_FRAME}$	W1	IO	OV_{DD}	5
$\overline{PCI\_TRDY}$	W4	IO	OV_{DD}	5
$\overline{PCI\_IRDY}$	W2	IO	OV_{DD}	5
$\overline{PCI\_STOP}$	V4	IO	OV_{DD}	5
$\overline{PCI\_DEVSEL}$	W3	IO	OV_{DD}	5
PCI_IDSEL	P2	I	OV_{DD}	—
$\overline{PCI\_SERR}$	U4	IO	OV_{DD}	5
$\overline{PCI\_PERR}$	V3	IO	OV_{DD}	5
$\overline{PCI\_REQ0}$	AD4	IO	OV_{DD}	—
$\overline{PCI\_REQ1}$/CPCI_HS_ES	AE3	I	OV_{DD}	—
$\overline{PCI\_REQ2}$	AF3	I	OV_{DD}	—
$\overline{PCI\_GNT0}$	AD3	IO	OV_{DD}	—
$\overline{PCI\_GNT1}$/CPCI_HS_LED	AE4	O	OV_{DD}	—
$\overline{PCI\_GNT2}$/CPCI_HS_ENUM	AF4	O	OV_{DD}	—
M66EN	L4	I	OV_{DD}	—

22 Clocking

Figure 43 shows the internal distribution of clocks within the MPC8323E.

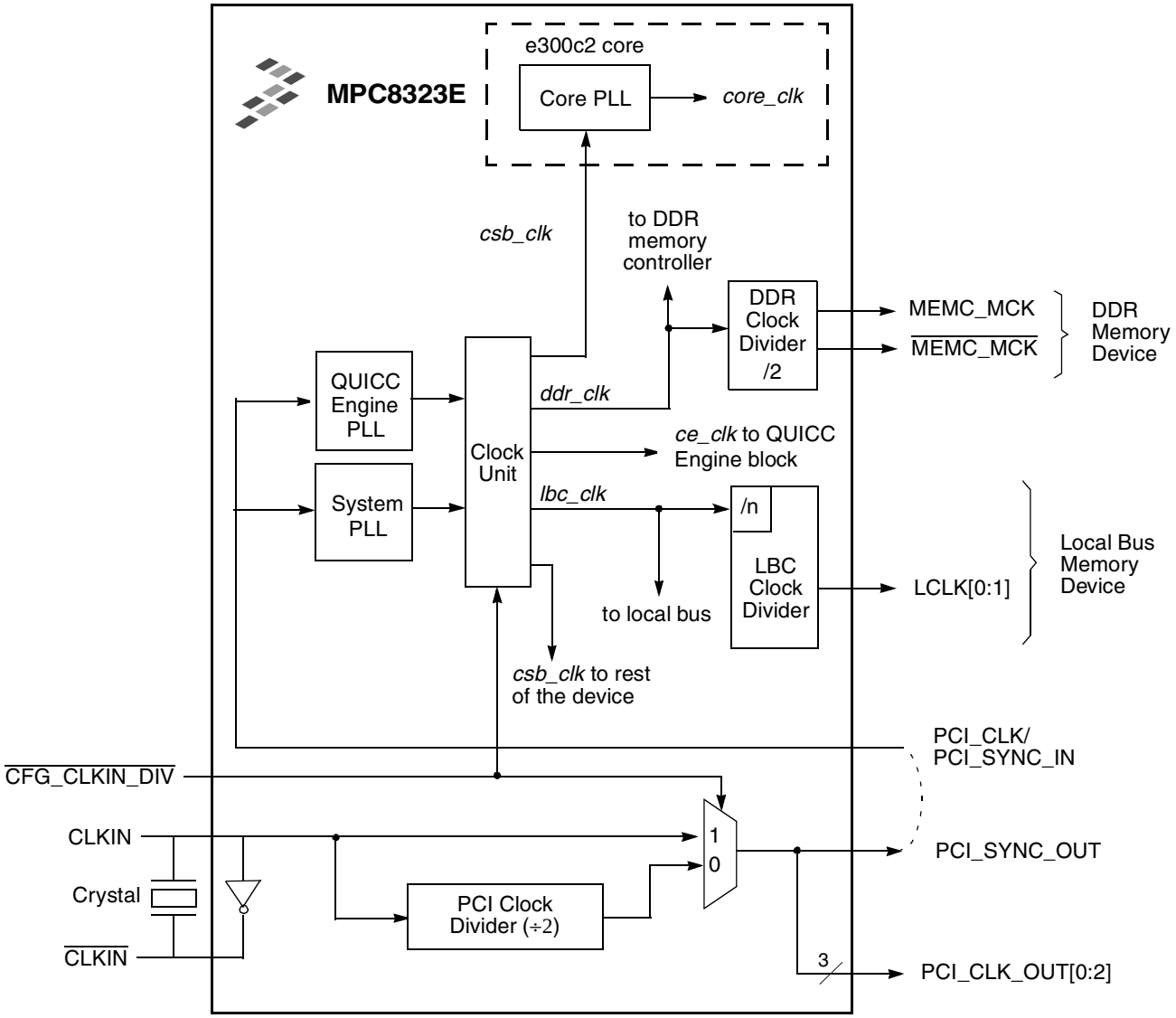


Figure 43. MPC8323E Clock Subsystem

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode, respectively.

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_C = case temperature of the package (°C)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
P_D = power dissipation (W)

24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8323E.

24.1 System Clocking

The MPC8323E includes three PLLs.

- The system PLL ($AV_{DD}2$) generates the system clock from the externally supplied CLKIN input. The frequency ratio between the system and CLKIN is selected using the system PLL ratio configuration bits as described in Section 22.4, “System PLL Configuration.”
- The e300 core PLL ($AV_{DD}3$) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in Section 22.5, “Core PLL Configuration.”
- The QUICC Engine PLL ($AV_{DD}1$) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each $AV_{DD}n$ pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 44, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

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Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
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