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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8323eczqaddc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong







Figure 3. MPC8323E Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation for this family of MPC8323E devices is shown in Table 5.

CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Core Frequency (MHz)	Typical	Maximum	Unit	Notes
133	200	266	0.74	1.48	W	1, 2, 3
133	200	333	0.78	1.62	W	1, 2, 3

Notes:

1. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.

2. Typical power is based on a nominal voltage of V_{DD} = 1.0 V, ambient temperature, and the core running a Dhrystone

benchmark application. The measurements were taken on the MPC8323MDS evaluation board using WC process silicon.

3. Maximum power is based on a voltage of V_{DD} = 1.07 V, WC process, a junction T_J = 110°C, and an artificial smoke test.

Table 6 shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V $R_s = 20 \Omega$ $R_t = 50 \Omega$ 1 pair of clocks	266 MHz, 1×32 bits	0.212	0.367	_	W	_



DDR1 and DDR2 SDRAM

Table 11. Reset Signals DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Input current	I _{IN}	$0 \ V \leq V_{IN} \leq OV_{DD}$		±5	μA	—

Note:

1. This specification applies when operating from 3.3 V supply.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR1 and DDR2 SDRAM interface of the MPC8323E. Note that DDR1 SDRAM is $Dn_GV_{DD}(typ) = 2.5$ V and DDR2 SDRAM is $Dn_GV_{DD}(typ) = 1.8$ V. The AC electrical specifications are the same for DDR1 and DDR2 SDRAM.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8323E when $Dn_GV_{DD}(typ) = 1.8 \text{ V}$.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	D <i>n_</i> GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MVREF <i>n</i> REF	$0.49 \times Dn_GV_{DD}$	$0.51 \times Dn_GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MVREFn _{REF} – 0.04	MVREF <i>n</i> _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MVREFn _{REF} + 0.125	D <i>n_</i> GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MVREFn _{REF} – 0.125	V	—
Output leakage current	I _{OZ}	-9.9	9.9	μA	4
Output high current (V _{OUT} = 1.35 V)	I _{ОН}	-13.4	—	mA	—
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	—

Table 12. DDR2 SDRAM DC Electrical Characteristics for Dn_GV_{DD}(typ) = 1.8 V

Notes:

1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.

- 2. MVREF *n*_{REF} is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF *n*_{REF} may not exceed ±2% of the DC value.
- 3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF*n*_{REF}. This rail should track variations in the DC level of MVREF*n*_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq Dn_GV_{DD}.

Table 13 provides the DDR2 capacitance when $Dn_GV_{DD}(typ) = 1.8$ V.

Table 13. DDR2 SDRAM Capacitance for Dn_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1



Ethernet and MII Management

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Мах	Unit
RX_CLK clock fall time	t _{MRXF}	1.0	_	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 8 provides the AC test load.



Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.



Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.



8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	OV _{DD} = Min	2.10	OV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	OV _{DD} = Min	GND	0.50	V
Input high voltage	V _{IH}	-	—		—	V
Input low voltage	V _{IL}	—		—	0.80	V
Input current	I _{IN}	0 V ≤ V _{II}	$0 V \le V_{IN} \le OV_{DD}$		±5	μA

Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V

8.3.2 MII Management AC Electrical Specifications

Table 28 provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Мах	Unit	Notes
MDC frequency	f _{MDC}	—	2.5	—	MHz	_
MDC period	t _{MDC}	—	400	—	ns	_
MDC clock pulse width high	t _{MDCH}	32	—	—	ns	_
MDC to MDIO delay	t _{MDKHDX}	10	—	70	ns	_
MDIO to MDC setup time	t _{MDDVKH}	5	—	—	ns	_
MDIO to MDC hold time	t _{MDDXKH}	0	—	—	ns	_
MDC rise time	t _{MDCR}	—	—	10	ns	_
MDC fall time	t _{MDHF}	—	—	10	ns	

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>



Local Bus

Figure 13 shows the MII management AC timing diagram.



Figure 13. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8323E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
High-level output voltage, I _{OH} = −100 μA	V _{OH}	OV _{DD} – 0.2	—	V
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V
Input current	I _{IN}	—	±5	μA

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8323E.

Table 30. Local Bus General Timing Parameters

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	15	—	ns	2
Input setup to local bus clock (LCLKn)	t _{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLKn)	t _{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT1}	1.5	—	ns	5



Parameter	Symbol ¹	Min	Мах	Unit	Notes
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3	_	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	_	ns	7
Local bus clock (LCLKn) to output valid	t _{LBKHOV}	—	3	ns	3
Local bus clock (LCLKn) to output high impedance for LAD/LDP	t _{LBKHOZ}	—	4	ns	8
Local bus clock (LCLKn) duty cycle	t _{LBDC}	47	53	%	_
Local bus clock (LCLKn) jitter specification	t _{LBRJ}	—	400	ps	_
Delay between the input clock (PCI_SYNC_IN) of local bus output clock (LCLK <i>n</i>)	t _{LBCDL}	—	1.7	ns	_

Table 30. Local Bus General Timing Parameters (continued)

Notes:

The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).

2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).

All signals are measured from OV_{DD}/2 of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.

4. Input timings are measured at the pin.

5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.

6. t_{LBOTOT2} should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.

7. t_{LBOTOT3} should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.

8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 14 provides the AC test load for the local bus.



Figure 14. Local Bus C Test Load



11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

Table 33. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V \pm 10%.

Parameter	Symbol	Min	Мах	Unit	Notes
Input high voltage level	V _{IH}	$0.7 imes OV_{DD}$	OV _{DD} + 0.3	V	
Input low voltage level	V _{IL}	-0.3	$0.3\times\text{OV}_{\text{DD}}$	V	_
Low level output voltage	V _{OL}	0	0.4	V	1
Output fall time from $V_{IH}(min)$ to $V_{IL}(max)$ with a bus capacitance from 10 to 400 pF	^t I2KLKV	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	Cl	_	10	pF	_
Input current (0 V \leq V _{IN} \leq OV _{DD})	I _{IN}	—	±5	μA	4

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. C_B = capacitance of one bus line in pF.

3. Refer to the MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual for information on the digital filter used.

4. I/O pins obstructs the SDA and SCL lines if $\ensuremath{\mathsf{OV}_{\mathsf{DD}}}$ is switched off.

11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I^2C interface of the MPC8323E.

Table 34. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol ¹	Min	Мах	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL}	1.3	—	μs
High period of the SCL clock		0.6	—	μs
Setup time for a repeated START condition		0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)		0.6	_	μs
Data setup time	t _{i2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	$\overline{0^2}$	 0.9 ³	μs

Figure 27 shows the PCI output AC timing conditions.



Figure 27. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8323E.

13.1 Timer DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the MPC8323E timer pins, including TIN, TOUT, TGATE, and RTC_CLK.

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	-	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 \text{ V} \leq \text{V}_{\text{IN}} \leq \text{OV}_{\text{DD}}$	—	±5	μA

Table 38. Timer DC Electrical Characteristics

13.2 Timer AC Timing Specifications

Table 39 provides the timer input and output AC timing specifications.

Table 39. Timer Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.



SPI

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 \ V \le V_{IN} \le OV_{DD}$	—	±5	μA

Table 44. SPI DC Electrical Characteristics

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
SPI outputs—Master mode (internal clock) delay	t _{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t _{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t _{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t _{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t _{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
</sub></sub>

Figure 30 provides the AC test load for the SPI.



Figure 30. SPI AC Test Load



Figure 39 shows the timing with external clock.





Figure 40 shows the timing with internal clock.



Figure 40. AC Timing (Internal Clock) Diagram



This section details package parameters, pin assignments, and dimensions. The MPC8323E is available in a thermally enhanced Plastic Ball Grid Array (PBGA); see Section 21.1, "Package Parameters for the MPC8323E PBGA," and Section 21.2, "Mechanical Dimensions of the MPC8323E PBGA," for information on the PBGA.

21.1 Package Parameters for the MPC8323E PBGA

The package parameters are as provided in the following list. The package type is $27 \text{ mm} \times 27 \text{ mm}$, 516 PBGA.

Package outline	$27 \text{ mm} \times 27 \text{ mm}$
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.6 mm

21.2 Mechanical Dimensions of the MPC8323E PBGA

Figure 42 shows the mechanical dimensions and bottom surface nomenclature of the MPC8323E, 516-PBGA package.





Notes:

1.All dimensions are in millimeters.

2.Dimensions and tolerances per ASME Y14.5M-1994.

3.Maximum solder ball diameter measured parallel to datum A.

4.Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 42. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8323E PBGA



Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MDQ29	AD20	10	GV _{DD}	
MEMC_MDQ30	AF23	10	GV _{DD}	
MEMC_MDQ31	AD22	IO	GV _{DD}	—
MEMC_MDM0	AC9	0	GV _{DD}	—
MEMC_MDM1	AD5	0	GV _{DD}	—
MEMC_MDM2	AE20	0	GV _{DD}	—
MEMC_MDM3	AE22	0	GV _{DD}	—
MEMC_MDQS0	AE8	IO	GV _{DD}	—
MEMC_MDQS1	AE5	IO	GV _{DD}	—
MEMC_MDQS2	AC19	IO	GV _{DD}	—
MEMC_MDQS3	AE23	IO	GV _{DD}	—
MEMC_MBA0	AD16	0	GV _{DD}	—
MEMC_MBA1	AD17	0	GV _{DD}	—
MEMC_MBA2	AE17	0	GV _{DD}	—
MEMC_MA0	AD12	0	GV _{DD}	—
MEMC_MA1	AE12	0	GV _{DD}	—
MEMC_MA2	AF12	0	GV _{DD}	—
MEMC_MA3	AC13	0	GV _{DD}	—
MEMC_MA4	AD13	0	GV _{DD}	—
MEMC_MA5	AE13	0	GV _{DD}	—
MEMC_MA6	AF13	0	GV _{DD}	—
MEMC_MA7	AC15	0	GV _{DD}	—
MEMC_MA8	AD15	0	GV _{DD}	—
MEMC_MA9	AE15	0	GV _{DD}	—
MEMC_MA10	AF15	0	GV _{DD}	—
MEMC_MA11	AE16	0	GV _{DD}	—
MEMC_MA12	AF16	0	GV _{DD}	—
MEMC_MA13	AB16	0	GV _{DD}	—
MEMC_MWE	AC17	0	GV _{DD}	—
MEMC_MRAS	AE11	0	GV _{DD}	[_
MEMC_MCAS	AD11	0	GV _{DD}	[_
MEMC_MCS	AC11	0	GV _{DD}	_

Table 55. MPC8323E PBGA Pinout Listing (continued)



Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PB17/BRGO1/CE_EXT_REQ1	D10	IO	OV _{DD}	
GPIO_PB18/Enet4_TXD[0]/SER4_TXD[0]/ TDMD_TXD[0]	C10	IO	OV _{DD}	—
GPIO_PB19/Enet4_TXD[1]/SER4_TXD[1]/ TDMD_TXD[1]	C9	IO	OV _{DD}	—
GPIO_PB20/Enet4_TXD[2]/SER4_TXD[2]/ TDMD_TXD[2]	D8	IO	OV _{DD}	—
GPIO_PB21/Enet4_TXD[3]/SER4_TXD[3]/ TDMD_TXD[3]	C8	IO	OV _{DD}	—
GPIO_PB22/Enet4_RXD[0]/SER4_RXD[0]/ TDMD_RXD[0]	C15	IO	OV _{DD}	—
GPIO_PB23/Enet4_RXD[1]/SER4_RXD[1]/ TDMD_RXD[1]	C14	IO	OV _{DD}	—
GPIO_PB24/Enet4_RXD[2]/SER4_RXD[2]/ TDMD_RXD[2]	D13	IO	OV _{DD}	—
GPIO_PB25/Enet4_RXD[3]/SER4_RXD[3]/ TDMD_RXD[3]	C13	IO	OV _{DD}	—
GPIO_PB26/Enet4_RX_ER/SER4_CD/TDMD_REQ	C12	IO	OV _{DD}	
GPIO_PB27/Enet4_TX_ER/TDMD_CLKO	D11	IO	OV _{DD}	
GPIO_PB28/Enet4_RX_DV/SER4_CTS/ TDMD_RSYNC	D12	IO	OV _{DD}	—
GPIO_PB29/Enet4_COL/RXD[4]/SER4_RXD[4]/ TDMD_STROBE	D7	IO	OV _{DD}	_
GPIO_PB30/Enet4_TX_EN/SER4_RTS/ TDMD_TSYNC	C11	IO	OV _{DD}	—
GPIO_PB31/Enet4_CRS/SDET	C7	IO	OV _{DD}	_
GPIO_PC0/UPC1_TxDATA[0]/SER5_TXD[0]	A18	Ю	OV_{DD}	_
GPIO_PC1/UPC1_TxDATA[1]/SER5_TXD[1]	A19	Ю	OV_{DD}	_
GPIO_PC2/UPC1_TxDATA[2]/SER5_TXD[2]	B18	Ю	OV _{DD}	—
GPIO_PC3/UPC1_TxDATA[3]/SER5_TXD[3]	B19	Ю	OV _{DD}	_
GPIO_PC4/UPC1_TxDATA[4]	A24	Ю	OV_{DD}	_
GPIO_PC5/UPC1_TxDATA[5]	B24	Ю	OV _{DD}	—
GPIO_PC6/UPC1_TxDATA[6]	A23	Ю	OV_{DD}	_
GPIO_PC7/UPC1_TxDATA[7]	B26	IO	OV _{DD}	
GPIO_PC8/UPC1_RxDATA[0]/SER5_RXD[0]	A21	IO	OV _{DD}	
GPIO_PC9/UPC1_RxDATA[1]/SER5_RXD[1]	B20	IO	OV _{DD}	



Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PC10/UPC1_RxDATA[2]/SER5_RXD[2]	B21	IO	OV _{DD}	—
GPIO_PC11/UPC1_RxDATA[3]/SER5_RXD[3]	A20	IO	OV _{DD}	—
GPIO_PC12/UPC1_RxDATA[4]	D19	IO	OV _{DD}	—
GPIO_PC13/UPC1_RxDATA[5]/LSRCID0	C18	IO	OV _{DD}	—
GPIO_PC14/UPC1_RxDATA[6]/LSRCID1	D18	IO	OV _{DD}	—
GPIO_PC15/UPC1_RxDATA[7]/LSRCID2	A25	IO	OV _{DD}	—
GPIO_PC16/UPC1_TxADDR[0]	C21	IO	OV _{DD}	—
GPIO_PC17/UPC1_TxADDR[1]/LSRCID3	D22	IO	OV _{DD}	—
GPIO_PC18/UPC1_TxADDR[2]/LSRCID4	C23	IO	OV _{DD}	—
GPIO_PC19/UPC1_TxADDR[3]/LDVAL	D23	IO	OV _{DD}	—
GPIO_PC20/UPC1_RxADDR[0]	C17	IO	OV _{DD}	—
GPIO_PC21/UPC1_RxADDR[1]	D17	IO	OV _{DD}	—
GPIO_PC22/UPC1_RxADDR[2]	C16	IO	OV _{DD}	—
GPIO_PC23/UPC1_RxADDR[3]	D16	IO	OV _{DD}	—
GPIO_PC24/UPC1_RxSOC/SER5_CD	A16	IO	OV _{DD}	—
GPIO_PC25/UPC1_RxCLAV	D20	IO	OV _{DD}	—
GPIO_PC26/UPC1_RxPRTY/CE_EXT_REQ2	E23	IO	OV _{DD}	—
GPIO_PC27/UPC1_RxEN	B17	IO	OV _{DD}	—
GPIO_PC28/UPC1_TxSOC	B22	IO	OV _{DD}	—
GPIO_PC29/UPC1_TxCLAV/SER5_CTS	A17	IO	OV _{DD}	—
GPIO_PC30/UPC1_TxPRTY	A22	IO	OV _{DD}	—
GPIO_PC31/UPC1_TxEN/SER5_RTS	C20	IO	OV _{DD}	—
GPIO_PD0/SPIMOSI	A2	IO	OV _{DD}	—
GPIO_PD1/SPIMISO	B2	IO	OV _{DD}	—
GPIO_PD2/SPICLK	B3	IO	OV _{DD}	—
GPIO_PD3/SPISEL	A3	IO	OV _{DD}	—
GPIO_PD4/SPI_MDIO/CE_MUX_MDIO	A4	IO	OV _{DD}	—
GPIO_PD5/SPI_MDC/CE_MUX_MDC	B4	IO	OV _{DD}	—
GPIO_PD6/CLK8/BRGO16/CE_EXT_REQ3	F24	IO	OV _{DD}	—
GPIO_PD7/GTM1_TIN1/GTM2_TIN2/CLK5	G24	IO	OV _{DD}	—
GPIO_PD8/GTM1_TGATE1/GTM2_TGATE2/CLK6	H24	IO	OV _{DD}	—
GPIO_PD9/GTM1_TOUT1	D24	IO	OV _{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)



22.1 Clocking in PCI Host Mode

When the MPC8323E is configured as a PCI host device (RCWH[PCIHOST] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (\div 2) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexors. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

22.1.1 PCI Clock Outputs (PCI_CLK_OUT[0:2])

When the MPC8323E is configured as a PCI host, it provides three separate clock output signals, PCI_CLK_OUT[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOEn] bit. All output clocks are phase-aligned to each other.

22.2 Clocking in PCI Agent Mode

When the MPC8323E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND, and the clock output signals, PCI_CLK_OUT*n* and PCI_SYNC_OUT, are not used.

22.3 System Clock Domains

As shown in Figure 43, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*ce_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lb_clk*)

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

 $csb_clk = [PCI_SYNC_IN \times (1 + \sim \overline{CFG_CLKIN_DIV})] \times SPMF$

In PCI host mode, PCI_SYNC_IN \times (1 + $\sim \overline{CFG}_{CLKIN}_{DIV}$) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300c2 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See the "Reset Configuration" section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.



Clocking

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

When CLKIN is the primary input clock,

 $ce_clk = (primary clock input \times CEPMF) \div (1 + CEPDF)$

When PCI_CLK is the primary input clock,

ce_clk = [primary clock input × CEPMF × $(1 + \sim CFG_CLKIN_DIV)$] ÷ (1 + CEPDF)

See the "QUICC Engine PLL Multiplication Factor" section and the "QUICC Engine PLL Division Factor" section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

The DDR SDRAM memory controller operates with a frequency equal to twice the frequency of csb_clk . Note that ddr_clk is not the external memory bus frequency; ddr_clk passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and MCK). However, the data rate is the same frequency as ddr_clk .

The local bus memory controller operates with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBC clock divider ratio is controlled by LCRR[CLKDIV]. See the "LBC Bus Clock and Clock Ratios" section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 56 specifies which units have a configurable clock frequency. Refer to the "System Clock Control Register (SCCR)" section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for a detailed description.

Table 56. Configurable Clock Units

Unit	Default Frequency	Options
Security core, I2C, SAP, TPR	csb_clk	Off, csb_clk/2, csb_clk/3
PCI and DMA complex	csb_clk	Off, csb_clk

NOTE

Setting the clock ratio of these units must be performed prior to any access to them.

Table 57 provides the operating frequencies for the 8323E PBGA under recommended operating conditions (see Table 2).

Table 57. Operating Frequencies for PBGA

Characteristic ¹	Max Operating Frequency	Unit
e300 core frequency (<i>core_clk</i>)	333	MHz
Coherent system bus frequency (<i>csb_clk</i>)	133	MHz
QUICC Engine frequency (<i>ce_clk</i>)	200	MHz



Characteristic ¹	Max Operating Frequency	Unit
DDR1/DDR2 memory bus frequency (MCLK) ²	133	MHz
Local bus frequency (LCLKn) ³	66	MHz
PCI input frequency (CLKIN or PCI_CLK)	66	MHz

Table 57. Operating Frequencies for PBGA (continued)

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.

² The DDR1/DDR2 data rate is 2× the DDR1/DDR2 memory bus frequency.

³ The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

22.4 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = $2 \times (CSB \text{ frequency}) \times (System PLL VCO divider})$.

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 300–600 MHz.

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111-1111	Reserved

Table 58. System PLL Multiplication Factors

As described in Section 22, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59



Thermal

where:

 $R_{\theta IA}$ = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers [™] P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800



NP

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 44 shows the PLL power supply filter circuit.



Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8323E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8323E system, and the MPC8323E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , and GV_{DD} pins of the MPC8323E. These decoupling capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , OV_{DD} , and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , or GV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , OV_{DD} , and GND pins of the MPC8323E.

24.5 Output Buffer DC Impedance

The MPC8323E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The