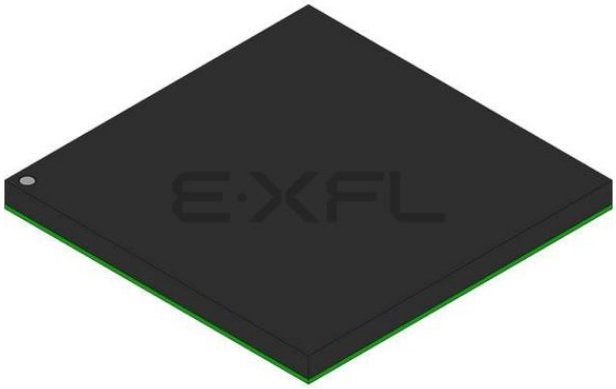


**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PowerPC e300c2 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 266MHz |
| Co-Processors/DSP | Communications; QUICC Engine, Security; SEC 2.2 |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (3) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography |
| Package / Case | 516-BBGA |
| Supplier Device Package | 516-FPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8323evraddc |

**NOTE**

The QUICC Engine block can also support a UTOPIA level 2 capable of supporting 31 multi-PHY (MPC8323E- and MPC8323-specific).

The MPC8323E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In summary, the MPC8323E family provides users with a highly integrated, fully programmable communications processor. This helps ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

## 1.1 MPC8323E Features

Major features of the MPC8323E are as follows:

- High-performance, low-power, and cost-effective single-chip data-plane/control-plane solution for ATM or IP/Ethernet packet processing (or both).
- MPC8323E QUICC Engine block offers a future-proof solution for next generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards.
- Single platform architecture supports the convergence of IP packet networks and ATM networks.
- DDR1/DDR2 memory controller—one 32-bit interface at up to 266 MHz supporting both DDR1 and DDR2.
- An e300c2 core built on Power Architecture technology with 16-Kbyte instruction and data caches, and dual integer units.
- Peripheral interfaces such as 32-bit PCI (2.2) interface up to 66-MHz operation, 16-bit local bus interface up to 66-MHz operation, and USB 2.0 (full-/low-speed).
- Security engine provides acceleration for control and data plane security protocols.
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration.

### 1.1.1 Protocols

The protocols are as follows:

- ATM SAR up to 155 Mbps (OC-3) full duplex, with ATM traffic shaping (ATF TM4.1)
- Support for ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- Support for IMA and ATM transmission convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- Support for 64 channels of HDLC/transparent

## 1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i™ standard, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

## 1.4 DDR Memory Controller

The MPC8323E DDR1/DDR2 memory controller includes the following features:

- Single 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266-MHz data rate
- Support for two ×16 devices
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O
- Support for 1 chip select only
- FCRAM, ECC, hardware/software calibration, bit deskew, QIN stage, or atomic logic are not supported.

## 1.5 PCI Controller

The MPC8323E PCI controller includes the following features:

- *PCI Specification Revision 2.3* compatible
- Single 32-bit data PCI interface operates up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

## 1.6 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 35 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

### 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

**Table 3. Output Drive Capability**

| Driver Type | Output Impedance (Ω) | Supply Voltage |
|---|---|---|
| Local bus interface utilities signals | 42 | $OV_{DD}$ = 3.3 V |
| PCI signals | 25 | |
| DDR1 signal | 18 | $GV_{DD}$ = 2.5 V |
| DDR2 signal | 18 | $GV_{DD}$ = 1.8 V |
| DUART, system control, I2C, SPI, JTAG | 42 | $OV_{DD}$ = 3.3 V |
| GPIO signals | 42 | $OV_{DD}$ = 3.3 V |

### 2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

**Table 4. Input Capacitance Specification**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input capacitance for all pins except CLKIN | $C_I$ | 6 | 8 | pF | — |
| Input capacitance for CLKIN | $C_{ICLKIN}$ | 10 | — | pF | 1 |

**Note:**
1. The external clock generator should be able to drive 10 pF.

## 2.2 Power Sequencing

The device does not require the core supply voltage ($V_{DD}$) and IO supply voltages ($GV_{DD}$ and $OV_{DD}$) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage ($V_{DD}$) before the I/O voltage ($GV_{DD}$ and $OV_{DD}$) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies ($GV_{DD}$ and $OV_{DD}$) do not have any ordering requirements with respect to one another.

**Table 6. Estimated Typical I/O Power Dissipation (continued)**

| | | | | | | |
|---|---|---|---|---|---|---|
| Local bus I/O<br>load = 25 pF<br>1 pair of clocks | 66 MHz, 32 bits | — | — | 0.12 | W | — |
| PCI I/O load = 30 pF | 66 MHz, 32 bits | — | — | 0.057 | W | — |
| QUICC Engine block and other I/Os | UTOPIA 8-bit 31 PHYs | — | — | 0.041 | W | Multiply by number of interfaces used. |
| | TDM serial | — | — | 0.001 | W | |
| | TDM nibble | — | — | 0.004 | W | |
| | HDLC/TRAN serial | — | — | 0.003 | W | |
| | HDLC/TRAN nibble | — | — | 0.025 | W | |
| | DUART | — | — | 0.017 | W | |
| | MIIs | — | — | 0.009 | W | |
| | RMII | — | — | 0.009 | W | |
| | Ethernet management | — | — | 0.002 | W | |
| | USB | — | — | 0.001 | W | |
| | SPI | — | — | 0.001 | W | |
| | Timer output | — | — | 0.002 | W | |

**NOTE**

$AV_{DD}n$ (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

# 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

**NOTE**

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

## 4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

**Table 7. CLKIN DC Electrical Characteristics**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | — | $V_{IH}$ | 2.7 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | — | $V_{IL}$ | –0.3 | 0.4 | V |

**Table 11. Reset Signals DC Electrical Characteristics (continued)**

| Characteristic | Symbol | Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le OV_{DD}$ | — | ±5 | μA | — |

**Note:**
1. This specification applies when operating from 3.3 V supply.

# 6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR1 and DDR2 SDRAM interface of the MPC8323E. Note that DDR1 SDRAM is D*n*_$GV_{DD}$(typ) = 2.5 V and DDR2 SDRAM is D*n*_$GV_{DD}$(typ) = 1.8 V. The AC electrical specifications are the same for DDR1 and DDR2 SDRAM.

## 6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8323E when D*n*_$GV_{DD}$(typ) = 1.8 V.

**Table 12. DDR2 SDRAM DC Electrical Characteristics for D*n*_$GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O supply voltage | D*n*_$GV_{DD}$ | 1.71 | 1.89 | V | 1 |
| I/O reference voltage | MVREF$n_{REF}$ | 0.49 × D*n*_$GV_{DD}$ | 0.51 × D*n*_$GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | MVREF$n_{REF}$ – 0.04 | MVREF$n_{REF}$ + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | MVREF$n_{REF}$ + 0.125 | D*n*_$GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | MVREF$n_{REF}$ – 0.125 | V | — |
| Output leakage current | $I_{OZ}$ | –9.9 | 9.9 | μA | 4 |
| Output high current ($V_{OUT}$ = 1.35 V) | $I_{OH}$ | –13.4 | — | mA | — |
| Output low current ($V_{OUT}$ = 0.280 V) | $I_{OL}$ | 13.4 | — | mA | — |

**Notes:**
1. D*n*_$GV_{DD}$ is expected to be within 50 mV of the DRAM D*n*_$GV_{DD}$ at all times.
2. MVREF$n_{REF}$ is expected to be equal to 0.5 × D*n*_$GV_{DD}$, and to track D*n*_$GV_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREF$n_{REF}$ may not exceed ±2% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF$n_{REF}$. This rail should track variations in the DC level of MVREF$n_{REF}$.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le$ D*n*_$GV_{DD}$.

Table 13 provides the DDR2 capacitance when D*n*_$GV_{DD}$(typ) = 1.8 V.

**Table 13. DDR2 SDRAM Capacitance for D*n*_$GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/output capacitance: DQ, DQS | $C_{IO}$ | 6 | 8 | pF | 1 |

Figure 4 shows the input timing diagram for the DDR controller.

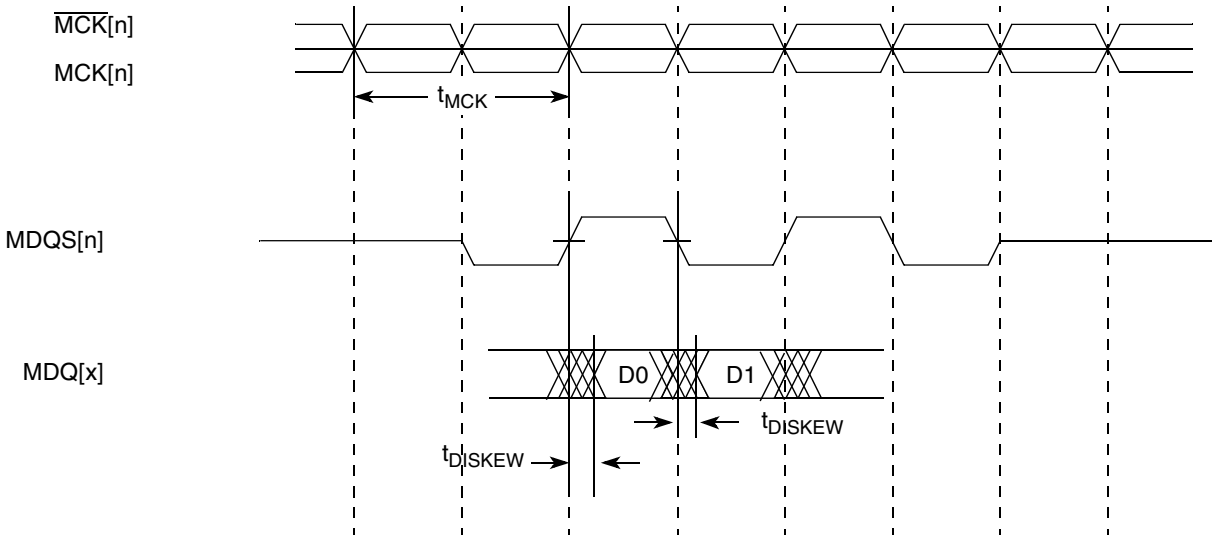



**Figure 4. DDR Input Timing Diagram**

## 6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

Table 19 provides the output AC timing specifications for the DDR1 and DDR2 SDRAM interfaces.

**Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications**

At recommended operating conditions with D*n*_GV$_{DD}$ of (1.8 or 2.5 V) ± 5%.

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK cycle time, (MCK/$\overline{\text{MCK}}$ crossing) | $t_{MCK}$ | 7.5 | 10 | ns | 2 |
| ADDR/CMD output setup with respect to MCK<br>266 MHz<br>200 MHz | $t_{DDKHAS}$ | <br>2.5<br>3.5 | <br>—<br>— | ns | 3 |
| ADDR/CMD output hold with respect to MCK<br>266 MHz<br>200 MHz | $t_{DDKHAX}$ | <br>2.5<br>3.5 | <br>—<br>— | ns | 3 |
| $\overline{\text{MCS}}$ output setup with respect to MCK<br>266 MHz<br>200 MHz | $t_{DDKHCS}$ | <br>2.5<br>3.5 | <br>—<br>— | ns | 3 |
| $\overline{\text{MCS}}$ output hold with respect to MCK<br>266 MHz<br>200 MHz | $t_{DDKHCX}$ | <br>2.5<br>3.5 | <br>—<br>— | ns | 3 |
| MCK to MDQS Skew | $t_{DDKHMH}$ | –0.6 | 0.6 | ns | 4 |

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8323E.

## 7.1 DUART DC Electrical Characteristics

Table 20 provides the DC electrical characteristics for the DUART interface of the MPC8323E.

**Table 20. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage $OV_{DD}$ | $V_{IL}$ | –0.3 | 0.8 | V |
| High-level output voltage, $I_{OH}$ = –100 µA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 µA | $V_{OL}$ | — | 0.2 | V |
| Input current (0 V ≤ $V_{IN}$ ≤ $OV_{DD}$)[1] | $I_{IN}$ | — | ±5 | µA |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 7.2 DUART AC Electrical Specifications

Table 21 provides the AC timing parameters for the DUART interface of the MPC8323E.

**Table 21. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | 256 | baud | |
| Maximum baud rate | > 1,000,000 | baud | 1 |
| Oversample rate | 16 | — | 2 |

**Notes:**
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8$^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16$^{th}$ sample.

# 8 Ethernet and MII Management

This section provides the AC and DC electrical characteristics for Ethernet and MII management.

## 8.1 Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics

The electrical characteristics specified here apply to all MII (media independent interface) and RMII (reduced media independent interface), except MDIO (management data input/output) and MDC

(management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

### 8.1.1 DC Electrical Characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in Table 22.

**Table 22. MII and RMII DC Electrical Characteristics**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 3.3 V | $OV_{DD}$ | — | | 2.97 | 3.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –4.0 mA | $OV_{DD}$ = Min | 2.40 | $OV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 4.0 mA | $OV_{DD}$ = Min | GND | 0.50 | V |
| Input high voltage | $V_{IH}$ | — | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | — | –0.3 | 0.90 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le OV_{DD}$ | | — | ±5 | μA |

## 8.2 MII and RMII AC Timing Specifications

The AC timing specifications for MII and RMII are presented in this section.

### 8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

#### 8.2.1.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

**Table 23. MII Transmit AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK clock period 10 Mbps | $t_{MTX}$ | — | 400 | — | ns |
| TX_CLK clock period 100 Mbps | $t_{MTX}$ | — | 40 | — | ns |
| TX_CLK duty cycle | $t_{MTXH}/t_{MTX}$ | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$ | 1 | 5 | 15 | ns |
| TX_CLK data clock rise time | $t_{MTXR}$ | 1.0 | — | 4.0 | ns |

### 8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

**Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (3.3 V) | $OV_{DD}$ | — | | 2.97 | 3.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | $OV_{DD}$ = Min | 2.10 | $OV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | $OV_{DD}$ = Min | GND | 0.50 | V |
| Input high voltage | $V_{IH}$ | — | | 2.00 | — | V |
| Input low voltage | $V_{IL}$ | — | | — | 0.80 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le OV_{DD}$ | | — | ±5 | μA |

### 8.3.2 MII Management AC Electrical Specifications

Table 28 provides the MII management AC timing specifications.

**Table 28. MII Management AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ is 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | — | 2.5 | — | MHz | — |
| MDC period | $t_{MDC}$ | — | 400 | — | ns | — |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| MDC to MDIO delay | $t_{MDKHDX}$ | 10 | — | 70 | ns | — |
| MDIO to MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | — |
| MDIO to MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | — |
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | — |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 13 shows the MII management AC timing diagram.

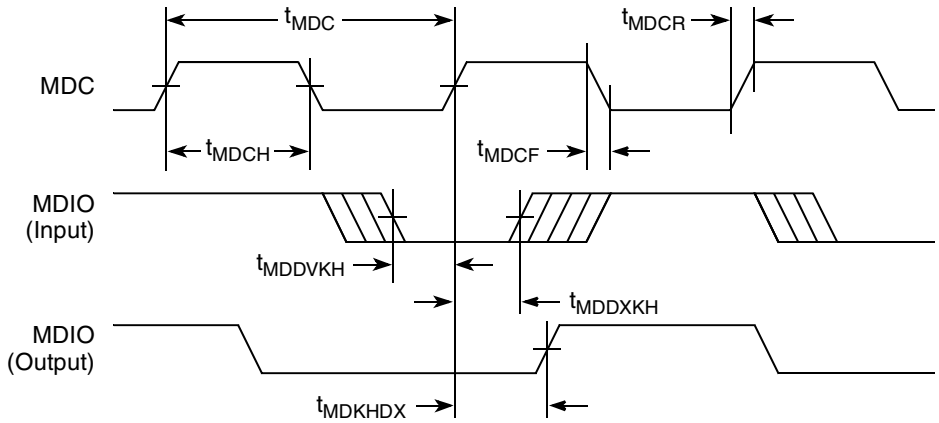



**Figure 13. MII Management Interface Timing Diagram**

# 9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8323E.

## 9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

**Table 29. Local Bus DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| High-level output voltage, $I_{OH}$ = –100 µA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 µA | $V_{OL}$ | — | 0.2 | V |
| Input current | $I_{IN}$ | — | ±5 | µA |

## 9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8323E.

**Table 30. Local Bus General Timing Parameters**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 15 | — | ns | 2 |
| Input setup to local bus clock (LCLK*n*) | $t_{LBIVKH}$ | 7 | — | ns | 3, 4 |
| Input hold from local bus clock (LCLK*n*) | $t_{LBIXKH}$ | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |

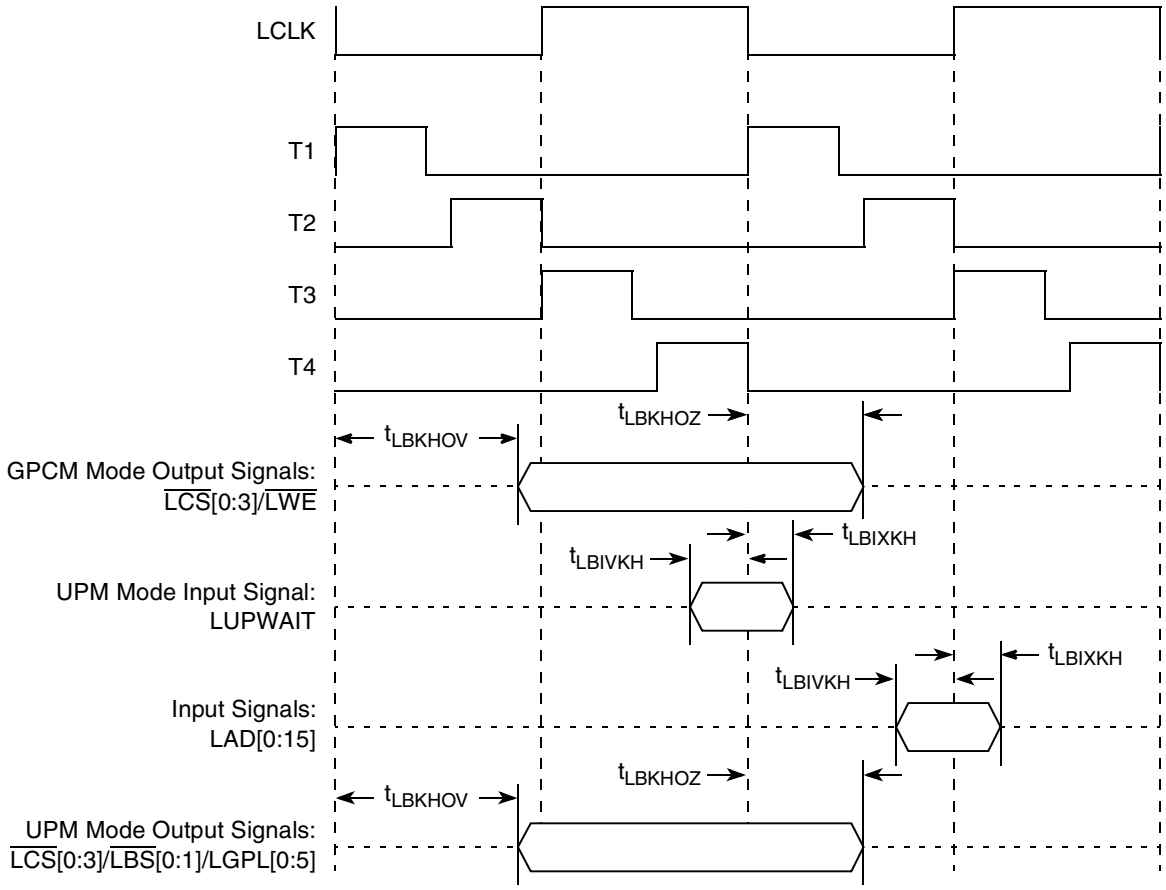



**Figure 17. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4**

# 10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8323E.

## 10.1 JTAG DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E.

**Table 31. JTAG Interface DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –6.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 6.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |
| Input high voltage | $V_{IH}$ | — | 2.5 | $OV_{DD}$ + 0.3 | V |

Figure 21 provides the boundary-scan timing diagram.

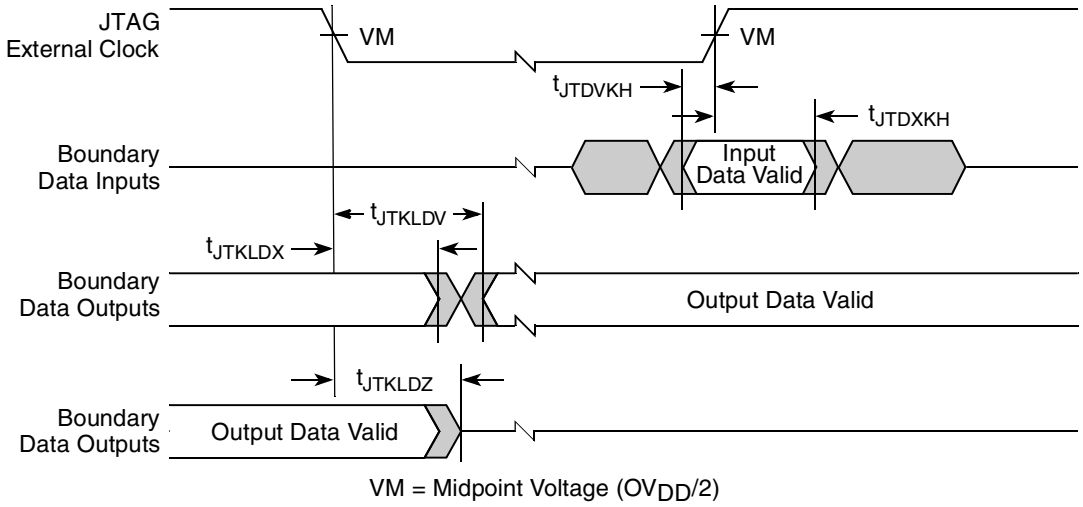



**Figure 21. Boundary-Scan Timing Diagram**

Figure 22 provides the test access port timing diagram.

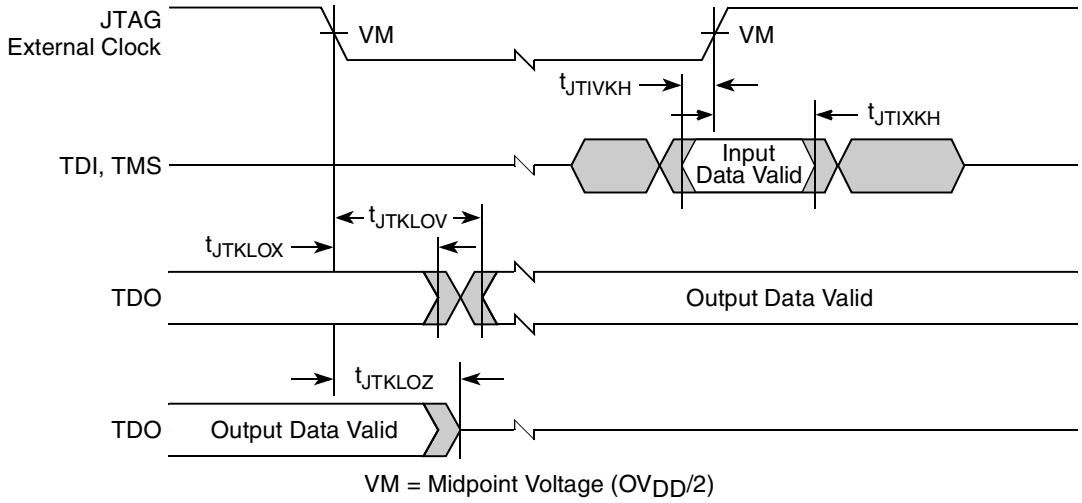



**Figure 22. Test Access Port Timing Diagram**

# 11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

## 11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

**Table 33. I²C DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 10%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage level | $V_{IH}$ | $0.7 \times OV_{DD}$ | $OV_{DD} + 0.3$ | V | — |
| Input low voltage level | $V_{IL}$ | –0.3 | $0.3 \times OV_{DD}$ | V | — |
| Low level output voltage | $V_{OL}$ | 0 | 0.4 | V | 1 |
| Output fall time from $V_{IH}$(min) to $V_{IL}$(max) with a bus capacitance from 10 to 400 pF | $t_{I2KLKV}$ | $20 + 0.1 \times C_B$ | 250 | ns | 2 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 3 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |
| Input current ($0 V \le V_{IN} \le OV_{DD}$) | $I_{IN}$ | — | ±5 | μA | 4 |

**Notes:**
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. $C_B$ = capacitance of one bus line in pF.
3. Refer to the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if $OV_{DD}$ is switched off.

## 11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I²C interface of the MPC8323E.

**Table 34. I²C AC Electrical Specifications**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 33).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz |
| Low period of the SCL clock | $t_{I2CL}$ | 1.3 | — | μs |
| High period of the SCL clock | $t_{I2CH}$ | 0.6 | — | μs |
| Setup time for a repeated START condition | $t_{I2SVKH}$ | 0.6 | — | μs |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6 | — | μs |
| Data setup time | $t_{I2DVKH}$ | 100 | — | ns |
| Data hold time: CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | —<br>0[2] | —<br>0.9[3] | μs |

# 12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8323E.

## 12.1 PCI DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the PCI interface of the MPC8323E.

**Table 35. PCI DC Electrical Characteristics[1,2]**

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | $V_{OUT} \geq V_{OH}$ (min) or | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | $V_{OUT} \leq V_{OL}$ (max) | –0.3 | 0.8 | V |
| High-level output voltage | $V_{OH}$ | $OV_{DD}$ = min, $I_{OH}$ = –100 µA | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage | $V_{OL}$ | $OV_{DD}$ = min, $I_{OL}$ = 100 µA | — | 0.2 | V |
| Input current | $I_{IN}$ | 0 V ≤ $V_{IN}$ ≤ $OV_{DD}$ | — | ±5 | µA |

**Notes:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.
2. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.3 Local Bus Specifications*.

## 12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8323E. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8323E is configured as a host or agent device. Table 36 shows the PCI AC timing specifications at 66 MHz.

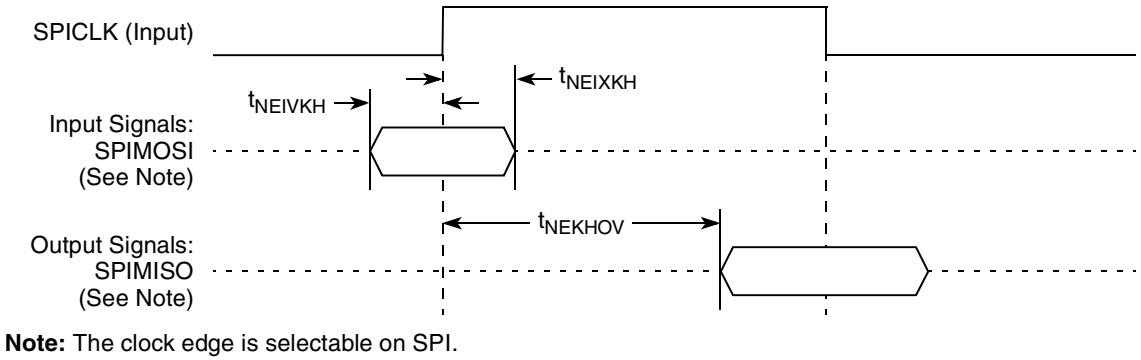
**Table 36. PCI AC Timing Specifications at 66 MHz**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 6.0 | ns | 2 |
| Output hold from clock | $t_{PCKHOX}$ | 1 | — | ns | 2 |
| Clock to output high impedence | $t_{PCKHOZ}$ | — | 14 | ns | 2, 3 |
| Input setup to clock | $t_{PCIVKH}$ | 3.0 | — | ns | 2, 4 |
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 2, 4 |

**Notes:**
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 31 and Figure 32 represent the AC timing from Table 45. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

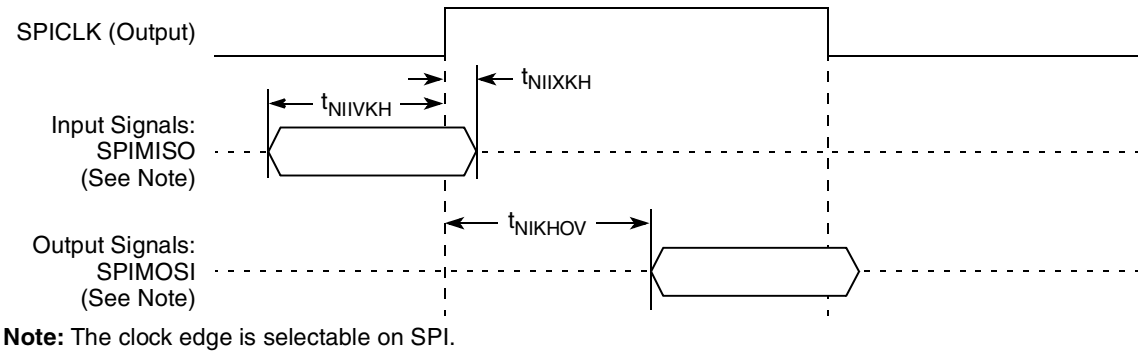
Figure 31 shows the SPI timing in slave mode (external clock).




**Note:** The clock edge is selectable on SPI.

**Figure 31. SPI AC Timing in Slave Mode (External Clock) Diagram**

Figure 32 shows the SPI timing in master mode (internal clock).




**Note:** The clock edge is selectable on SPI.

**Figure 32. SPI AC Timing in Master Mode (Internal Clock) Diagram**

# 17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8323E.

## 17.1 TDM/SI DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the MPC8323E TDM/SI.

**Table 46. TDM/SI DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –2.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.5 | V |
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |

# 21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8323E is available in a thermally enhanced Plastic Ball Grid Array (PBGA); see Section 21.1, "Package Parameters for the MPC8323E PBGA," and Section 21.2, "Mechanical Dimensions of the MPC8323E PBGA," for information on the PBGA.

## 21.1 Package Parameters for the MPC8323E PBGA

The package parameters are as provided in the following list. The package type is 27 mm × 27 mm, 516 PBGA.

| | |
|---|---|
| Package outline | 27 mm × 27 mm |
| Interconnects | 516 |
| Pitch | 1.00 mm |
| Module height (typical) | 2.25 mm |
| Solder Balls | 62 Sn/36 Pb/2 Ag (ZQ package)<br>95.5 Sn/0.5 Cu/4Ag (VR package) |
| Ball diameter (typical) | 0.6 mm |

## 21.2 Mechanical Dimensions of the MPC8323E PBGA

Figure 42 shows the mechanical dimensions and bottom surface nomenclature of the MPC8323E, 516-PBGA package.

**Table 57. Operating Frequencies for PBGA (continued)**

| Characteristic[1] | Max Operating Frequency | Unit |
|---|---|---|
| DDR1/DDR2 memory bus frequency (MCLK)[2] | 133 | MHz |
| Local bus frequency (LCLK*n*)[3] | 66 | MHz |
| PCI input frequency (CLKIN or PCI_CLK) | 66 | MHz |

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2 The DDR1/DDR2 data rate is 2× the DDR1/DDR2 memory bus frequency.
3 The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

## 22.4 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

**NOTE**

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 300–600 MHz.

**Table 58. System PLL Multiplication Factors**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 0000 | Reserved |
| 0001 | Reserved |
| 0010 | × 2 |
| 0011 | × 3 |
| 0100 | × 4 |
| 0101 | × 5 |
| 0110 | × 6 |
| 0111–1111 | Reserved |

As described in Section 22, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG\_CLKIN\_DIV}}$ configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59

shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

**Table 59. CSB Frequency Options**

| CFG_CLKIN_DIV_B at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio [2] | Input Clock Frequency (MHz)[2] | | |
|---|---|---|---|---|---|
| | | | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | |
| High | 0010 | 2 : 1 | | | 133 |
| High | 0011 | 3 : 1 | | 100 | |
| High | 0100 | 4 : 1 | 100 | 133 | |
| High | 0101 | 5 : 1 | 125 | | |
| High | 0110 | 6 : 1 | | | |
| High | 0111 | 7 : 1 | | | |
| High | 1000 | 8 : 1 | | | |
| High | 1001 | 9 : 1 | | | |
| High | 1010 | 10 : 1 | | | |
| High | 1011 | 11 : 1 | | | |
| High | 1100 | 12 : 1 | | | |
| High | 1101 | 13 : 1 | | | |
| High | 1110 | 14 : 1 | | | |
| High | 1111 | 15 : 1 | | | |
| High | 0000 | 16 : 1 | | | |
| Low | 0010 | 2 : 1 | | | 133 |
| Low | 0011 | 3 : 1 | | 100 | |
| Low | 0100 | 4 : 1 | | 133 | |
| Low | 0101 | 5 : 1 | | | |
| Low | 0110 | 6 : 1 | | | |
| Low | 0111 | 7 : 1 | | | |
| Low | 1000 | 8 : 1 | | | |
| Low | 1001 | 9 : 1 | | | |
| Low | 1010 | 10 : 1 | | | |
| Low | 1011 | 11 : 1 | | | |
| Low | 1100 | 12 : 1 | | | |
| Low | 1101 | 13 : 1 | | | |
| Low | 1110 | 14 : 1 | | | |
| Low | 1111 | 15 : 1 | | | |
| Low | 0000 | 16 : 1 | | | |

1 CFG_CLKIN_DIV_B is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV_B must be pulled up (high) in agent mode.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-567-8082
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics 800-522-2800
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation 800-248-2481
Dow-Corning Electronic Materials
P.O. Box 994
Midland, MI 48686-0997
Internet: www.dowcorning.com

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company 800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

## 23.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

### 23.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the