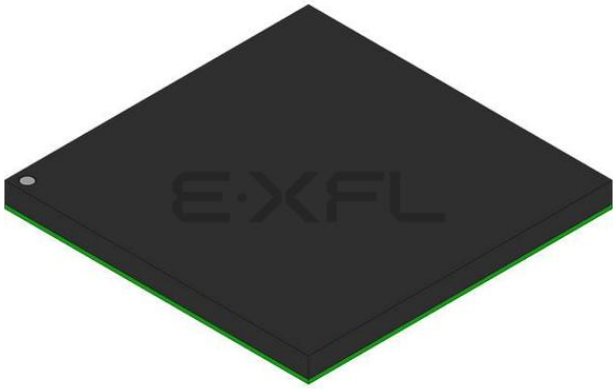

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA
Supplier Device Package	516-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8323ezqafdc

1.1.2 Serial Interfaces

The MPC8323E serial interfaces are as follows:

- Support for one UL2 interface with 31 multi-PHY addresses (MPC8323E and MPC8323 only)
- Support for up to three 10/100 Mbps Ethernet interfaces using MII or RMII
- Support for up to four T1/E1/J1/E3 or DS-3 serial interfaces (TDM)
- Support for dual UART and SPI interfaces and a single I^2C interface

1.2 QUICC Engine Block

The QUICC Engine block is a versatile communications complex that integrates several communications peripheral controllers. It provides on-chip system design for a variety of applications, particularly in communications and networking systems. The QUICC Engine block has the following features:

- One 32-bit RISC controller for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
  - 10/100 Mbps Ethernet/IEEE 802.3® standard
  - IP support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
  - ATM protocol through UTOPIA interface (note that the MPC8321 and MPC8321E do not support the UTOPIA interface)
  - HDLC /transparent up to 70-Mbps full-duplex
  - HDLC bus up to 10 Mbps
  - Asynchronous HDLC
  - UART
  - BISYNC up to 2 Mbps
  - QUICC multi-channel controller (QMC) for 64 TDM channels
- One UTOPIA interface (UPC1) supporting 31 multi-PHYs (MPC8323E- and MPC8323-specific)
- Two serial peripheral interfaces (SPI). SPI2 is dedicated to Ethernet PHY management.
- Four TDM interfaces
- Thirteen independent baud rate generators and 19 input clock pins for supplying clocks to UCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

The UCCs are similar to the PowerQUICC II peripherals: SCC (BISYNC, UART, and HDLC bus) and FCC (fast Ethernet, HDLC, transparent, and ATM).

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8323E. The MPC8323E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DDn}	–0.3 to 1.26	V	—
DDR1 and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
PCI, local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.6	V	—
Input voltage	DDR1/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2
	DDR1/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2
	Local bus, DUART, CLKIN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	5
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8323E. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions[3]

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	1
PLL supply voltage	AV_{DD}	1.0 V ± 50 mV	V	1
DDR1 and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
PCI, local bus, DUART, system control and power management, I^2C, SPI, and JTAG I/O voltage	OV_{DD}	3.3 V ± 300 mV	V	1
Junction temperature	T_A/T_J	0 to 105	°C	2

Note:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.
3. All IO pins should be interfaced with peripherals operating at same voltage level.
4. This voltage is the input to the filter discussed in Section 24.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced due to voltage drop across the filter.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8323E

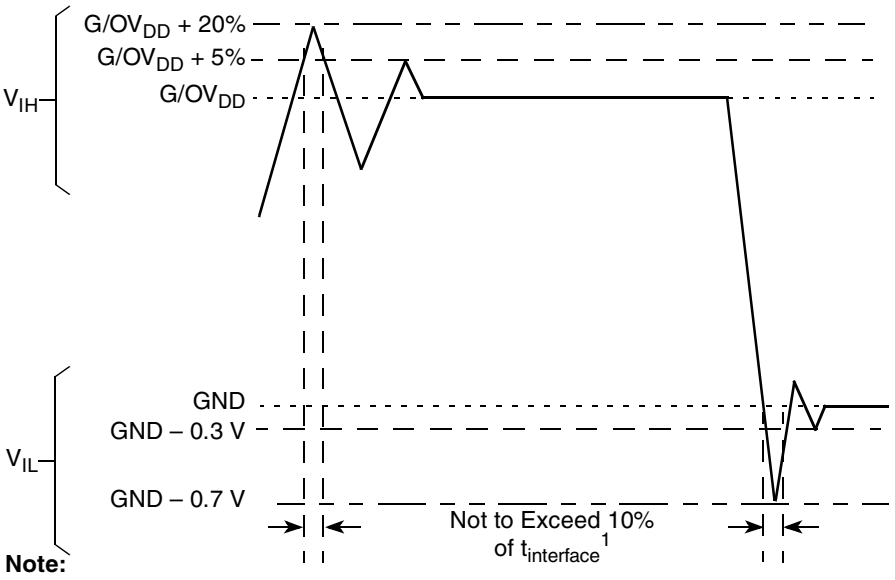


Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}

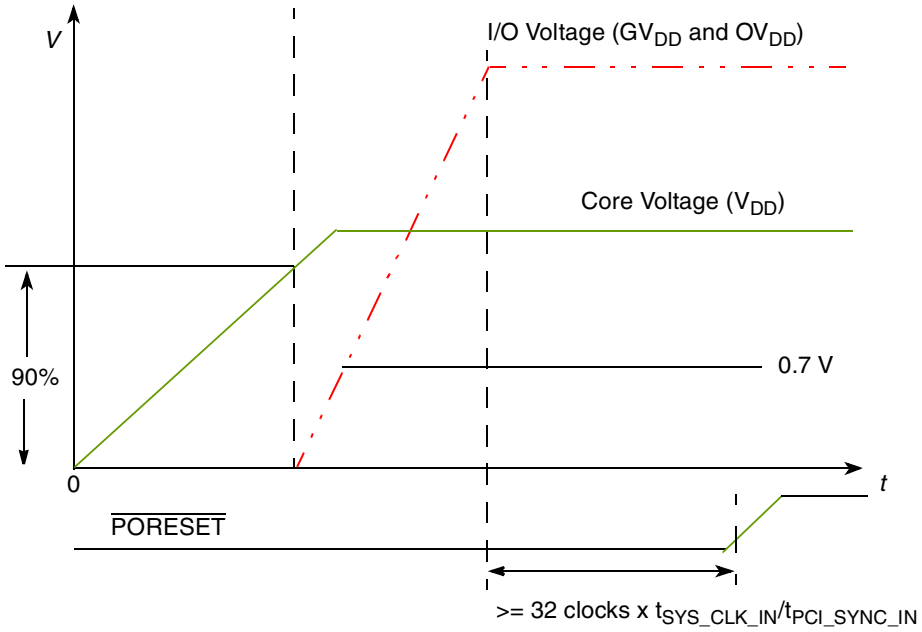


Figure 3. MPC8323E Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation for this family of MPC8323E devices is shown in Table 5.

Table 5. MPC8323E Power Dissipation

CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Core Frequency (MHz)	Typical	Maximum	Unit	Notes
133	200	266	0.74	1.48	W	1, 2, 3
133	200	333	0.78	1.62	W	1, 2, 3

Notes:
1. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a nominal voltage of V_{DD} = 1.0 V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the MPC8323MDS evaluation board using WC process silicon.
3. Maximum power is based on a voltage of V_{DD} = 1.07 V, WC process, a junction T_J = 110°C, and an artificial smoke test.

Table 6 shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V R_s = 20 Ω R_t = 50 Ω 1 pair of clocks	266 MHz, 1 × 32 bits	0.212	0.367	—	W	—

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
HRESET/SRESET assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
HRESET negation to SRESET negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8323E is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of HRESET	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of HRESET	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of HRESET	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—

Table 13. DDR2 SDRAM Capacitance for D*n*_GV$_{DD}$(typ) = 1.8 V

Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV$_{DD}$ = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25 °C, V_{OUT} = D*n*_GV$_{DD}$ ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR1 SDRAM component(s) of the MPC8323E when D*n*_GV$_{DD}$(typ) = 2.5 V.

Table 14. DDR1 SDRAM DC Electrical Characteristics for D*n*_GV$_{DD}$(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV$_{DD}$	2.375	2.625	V	1
I/O reference voltage	MVREF*n*$_{REF}$	0.49 × D*n*_GV$_{DD}$	0.51 × D*n*_GV$_{DD}$	V	2
I/O termination voltage	V_{TT}	MVREF*n*$_{REF}$ – 0.04	MVREF*n*$_{REF}$ + 0.04	V	3
Input high voltage	V_{IH}	MVREF*n*$_{REF}$ + 0.15	D*n*_GV$_{DD}$ + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF*n*$_{REF}$ – 0.15	V	—
Output leakage current	I_{OZ}	–9.9	–9.9	µA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Notes:
1. D*n*_GV$_{DD}$ is expected to be within 50 mV of the DRAM D*n*_GV$_{DD}$ at all times.
2. MVREF*n*$_{REF}$ is expected to be equal to 0.5 × D*n*_GV$_{DD}$, and to track D*n*_GV$_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n*$_{REF}$ may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF*n*$_{REF}$. This rail should track variations in the DC level of MVREF*n*$_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV$_{DD}$.

Table 15 provides the DDR1 capacitance D*n*_GV$_{DD}$(typ) = 2.5 V.

Table 15. DDR1 SDRAM Capacitance for D*n*_GV$_{DD}$(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ,DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV$_{DD}$ = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25° C, V_{OUT} = D*n*_GV$_{DD}$ ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR1 and DDR2 SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM (D*n*_GV_{DD}(typ) = 1.8 V).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with D*n*_GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MVREFn_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MVREFn_{REF} + 0.25	—	V	—

Table 17 provides the input AC timing specifications for the DDR1 SDRAM (D*n*_GV_{DD}(typ) = 2.5 V).

Table 17. DDR1 SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with D*n*_GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MVREFn_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MVREFn_{REF} + 0.31	—	V	—

Table 18 provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 18. DDR1 and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with D*n*_GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2
266 MHz		–750	750		
200 MHz		–1250	1250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with D*n*_GV$_{DD}$ of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.9 1.0	 — —	ns	5
MDQ/MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100 1200	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Table 26. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load.

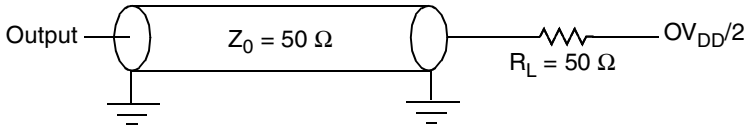


Figure 11. AC Test Load

Figure 12 shows the RMII receive AC timing diagram.

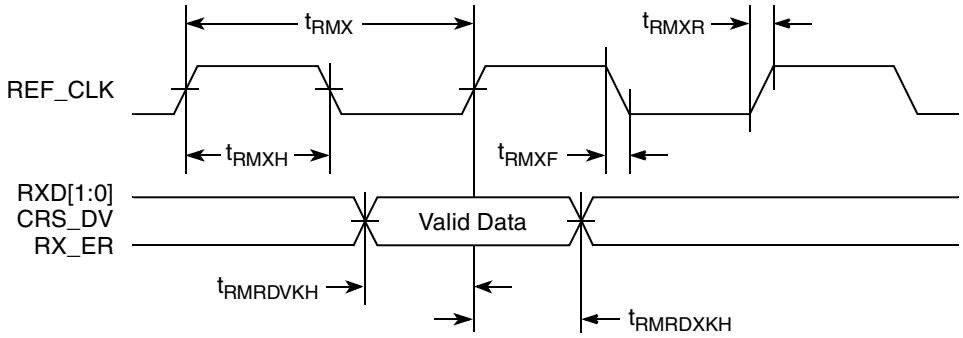


Figure 12. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, “Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics.”

Figure 13 shows the MII management AC timing diagram.

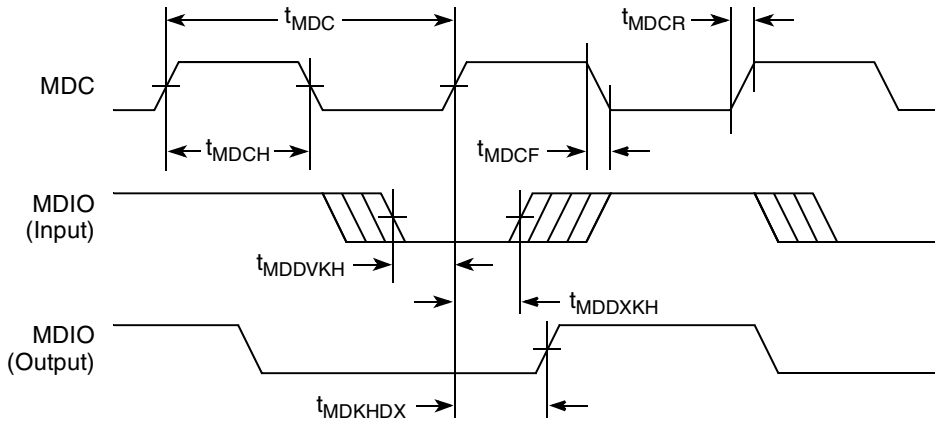


Figure 13. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8323E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±5	µA

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8323E.

Table 30. Local Bus General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK*n*)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK*n*)	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5

Table 34. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol[1]	Min	Max	Unit
Rise time of both SDA and SCL signals	t_{I2CR}	20 + 0.1 C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_b[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8323E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

Figure 23 provides the AC test load for the I²C.

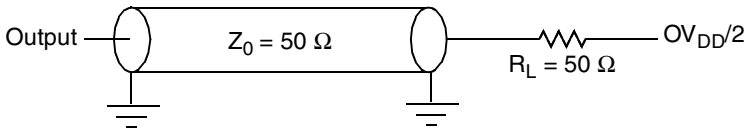


Figure 23. I²C AC Test Load

Figure 24 shows the AC timing diagram for the I²C bus.

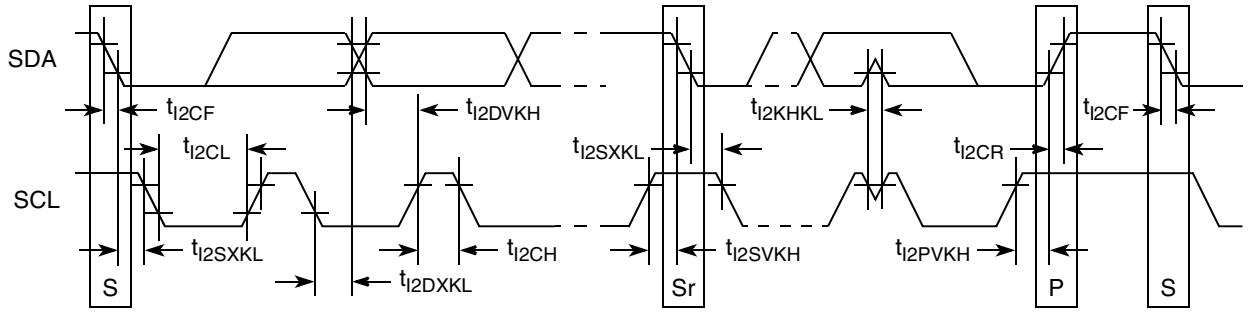


Figure 24. I²C Bus AC Timing Diagram

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Table 44. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 30 provides the AC test load for the SPI.

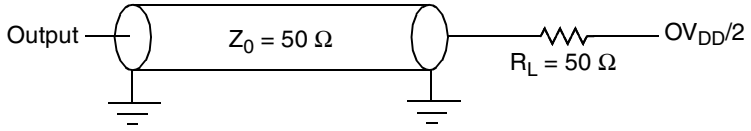
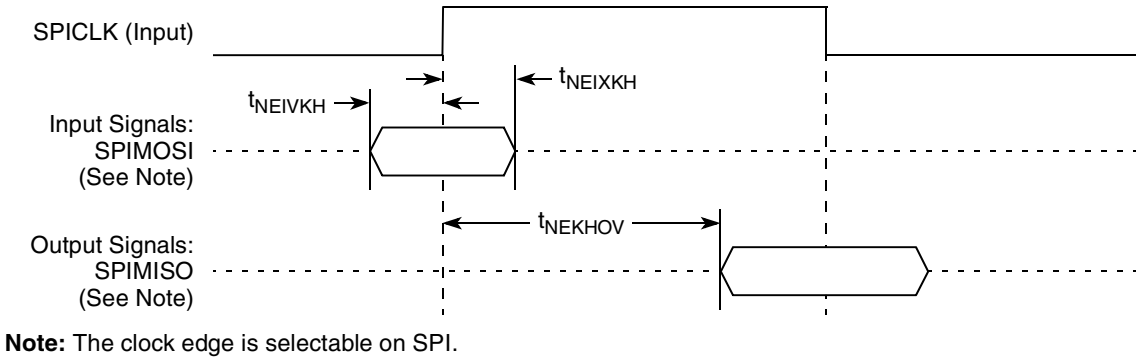


Figure 30. SPI AC Test Load

Figure 31 and Figure 32 represent the AC timing from Table 45. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

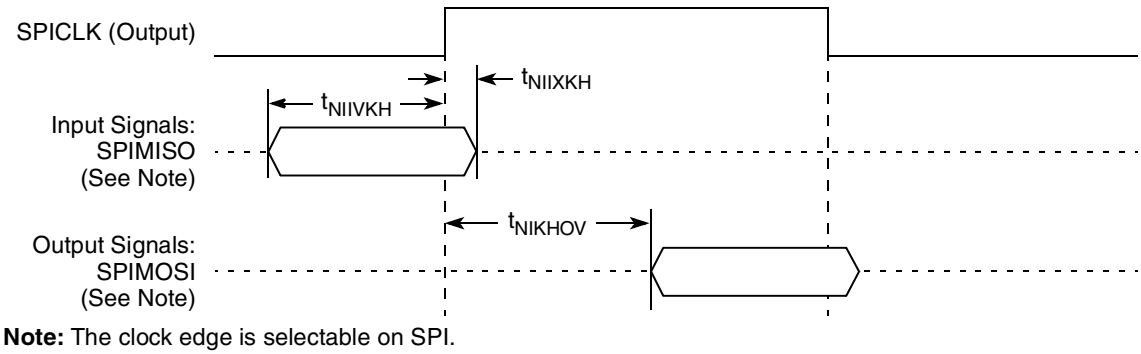
Figure 31 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 31. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 32 shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 32. SPI AC Timing in Master Mode (Internal Clock) Diagram

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8323E.

17.1 TDM/SI DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the MPC8323E TDM/SI.

Table 46. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	O	GV_{DD}	3
MEMC_MCK	AF14	O	GV_{DD}	—
$\overline{\text{MEMC\_MCK}}$	AE14	O	GV_{DD}	—
MEMC_MODT	AF11	O	GV_{DD}	—
Local Bus Controller Interface				
LAD0	N25	IO	OV_{DD}	7
LAD1	P26	IO	OV_{DD}	7
LAD2	P25	IO	OV_{DD}	7
LAD3	R26	IO	OV_{DD}	7
LAD4	R25	IO	OV_{DD}	7
LAD5	T26	IO	OV_{DD}	7
LAD6	T25	IO	OV_{DD}	7
LAD7	U25	IO	OV_{DD}	7
LAD8	M24	IO	OV_{DD}	7
LAD9	N24	IO	OV_{DD}	7
LAD10	P24	IO	OV_{DD}	7
LAD11	R24	IO	OV_{DD}	7
LAD12	T24	IO	OV_{DD}	7
LAD13	U24	IO	OV_{DD}	7
LAD14	U26	IO	OV_{DD}	7
LAD15	V26	IO	OV_{DD}	7
LA16	K25	O	OV_{DD}	7
LA17	L25	O	OV_{DD}	7
LA18	L26	O	OV_{DD}	7
LA19	L24	O	OV_{DD}	7
LA20	M26	O	OV_{DD}	7
LA21	M25	O	OV_{DD}	7
LA22	N26	O	OV_{DD}	7
LA23	AC24	O	OV_{DD}	7
LA24	AC25	O	OV_{DD}	7
LA25	AB23	O	OV_{DD}	7
$\overline{\text{LCS0}}$	AB24	O	OV_{DD}	4

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Supplies				
$AV_{DD}1$	P3	I	$AV_{DD}1$	—
$AV_{DD}2$	AA1	I	$AV_{DD}2$	—
$AV_{DD}3$	AB15	I	$AV_{DD}3$	—
$AV_{DD}4$	C24	I	$AV_{DD}4$	—
MVREF1	AB8	I	DDR reference voltage	—
MVREF2	AB17	I	DDR reference voltage	—
PCI				
$\overline{\text{PCI\_INTA}}$ /$\overline{\text{IRQ\_OUT}}$	AF2	O	OV_{DD}	2
$\overline{\text{PCI\_RESET\_OUT}}$	AE2	O	OV_{DD}	—
PCI_AD0/MSRCID0 (DDR ID)	L1	IO	OV_{DD}	—
PCI_AD1/MSRCID1 (DDR ID)	L2	IO	OV_{DD}	—
PCI_AD2/MSRCID2 (DDR ID)	M1	IO	OV_{DD}	—
PCI_AD3/MSRCID3 (DDR ID)	M2	IO	OV_{DD}	—
PCI_AD4/MSRCID4 (DDR ID)	L3	IO	OV_{DD}	—
PCI_AD5/MDVAL (DDR ID)	N1	IO	OV_{DD}	—
PCI_AD6	N2	IO	OV_{DD}	—
PCI_AD7	M3	IO	OV_{DD}	—
PCI_AD8	P1	IO	OV_{DD}	—
PCI_AD9	R1	IO	OV_{DD}	—
PCI_AD10	N3	IO	OV_{DD}	—
PCI_AD11	N4	IO	OV_{DD}	—
PCI_AD12	T1	IO	OV_{DD}	—
PCI_AD13	R2	IO	OV_{DD}	—
PCI_AD14/ECID_TMODE_IN	T2	IO	OV_{DD}	—
PCI_AD15	U1	IO	OV_{DD}	—
PCI_AD16	Y2	IO	OV_{DD}	—
PCI_AD17	Y1	IO	OV_{DD}	—
PCI_AD18	AA2	IO	OV_{DD}	—
PCI_AD19	AB1	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PB17/BRGO1/CE_EXT_REQ1	D10	IO	OV_{DD}	—
GPIO_PB18/Enet4_TXD[0]/SER4_TXD[0]/ TDMD_TXD[0]	C10	IO	OV_{DD}	—
GPIO_PB19/Enet4_TXD[1]/SER4_TXD[1]/ TDMD_TXD[1]	C9	IO	OV_{DD}	—
GPIO_PB20/Enet4_TXD[2]/SER4_TXD[2]/ TDMD_TXD[2]	D8	IO	OV_{DD}	—
GPIO_PB21/Enet4_TXD[3]/SER4_TXD[3]/ TDMD_TXD[3]	C8	IO	OV_{DD}	—
GPIO_PB22/Enet4_RXD[0]/SER4_RXD[0]/ TDMD_RXD[0]	C15	IO	OV_{DD}	—
GPIO_PB23/Enet4_RXD[1]/SER4_RXD[1]/ TDMD_RXD[1]	C14	IO	OV_{DD}	—
GPIO_PB24/Enet4_RXD[2]/SER4_RXD[2]/ TDMD_RXD[2]	D13	IO	OV_{DD}	—
GPIO_PB25/Enet4_RXD[3]/SER4_RXD[3]/ TDMD_RXD[3]	C13	IO	OV_{DD}	—
GPIO_PB26/Enet4_RX_ER/SER4_CD/TDMD_REQ	C12	IO	OV_{DD}	—
GPIO_PB27/Enet4_TX_ER/TDMD_CLKO	D11	IO	OV_{DD}	—
GPIO_PB28/Enet4_RX_DV/SER4_CTS/ TDMD_RSYNC	D12	IO	OV_{DD}	—
GPIO_PB29/Enet4_COL/RXD[4]/SER4_RXD[4]/ TDMD_STROBE	D7	IO	OV_{DD}	—
GPIO_PB30/Enet4_TX_EN/SER4_RTS/ TDMD_TSYNC	C11	IO	OV_{DD}	—
GPIO_PB31/Enet4_CRS/SDET	C7	IO	OV_{DD}	—
GPIO_PC0/UPC1_TxDATA[0]/SER5_TXD[0]	A18	IO	OV_{DD}	—
GPIO_PC1/UPC1_TxDATA[1]/SER5_TXD[1]	A19	IO	OV_{DD}	—
GPIO_PC2/UPC1_TxDATA[2]/SER5_TXD[2]	B18	IO	OV_{DD}	—
GPIO_PC3/UPC1_TxDATA[3]/SER5_TXD[3]	B19	IO	OV_{DD}	—
GPIO_PC4/UPC1_TxDATA[4]	A24	IO	OV_{DD}	—
GPIO_PC5/UPC1_TxDATA[5]	B24	IO	OV_{DD}	—
GPIO_PC6/UPC1_TxDATA[6]	A23	IO	OV_{DD}	—
GPIO_PC7/UPC1_TxDATA[7]	B26	IO	OV_{DD}	—
GPIO_PC8/UPC1_RxDATA[0]/SER5_RXD[0]	A21	IO	OV_{DD}	—
GPIO_PC9/UPC1_RxDATA[1]/SER5_RXD[1]	B20	IO	OV_{DD}	—

22.6 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. Table 61 shows the multiplication factor encodings for the QUICC Engine PLL.

Table 61. QUICC Engine PLL Multiplication Factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF)
00000–00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in Table 62.

Table 62. QUICC Engine PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

$$ce\_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$$

$$\text{QUICC Engine VCO Frequency} = ce\_clk \times \text{VCO divider} \times (1 + \text{CEPDF})$$

22.7 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8323E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 63 shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

Table 63. Suggested PLL Configurations

Conf No.	SPMF	Core PLL	CEMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0110	0	33.33	133.33	266.66	200
2	0100	0000101	1000	0	25	100	250	200
3	0010	0000100	0011	0	66.67	133.33	266.66	200
4	0100	0000101	0110	0	33.33	133.33	333.33	200
5	0101	0000101	1000	0	25	125	312.5	200
6	0010	0000101	0011	0	66.67	133.33	333.33	200

23 Thermal

This section describes the thermal specifications of the MPC8323E.

23.1 Thermal Characteristics

Table 64 provides the package thermal characteristics for the 516 27×27 mm PBGA of the MPC8323E.

Table 64. Package Thermal Characteristics for PBGA

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	21	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	23	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	13	°C/W	4
Junction-to-case	—	$R_{\theta JC}$	9	°C/W	5

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 44 shows the PLL power supply filter circuit.

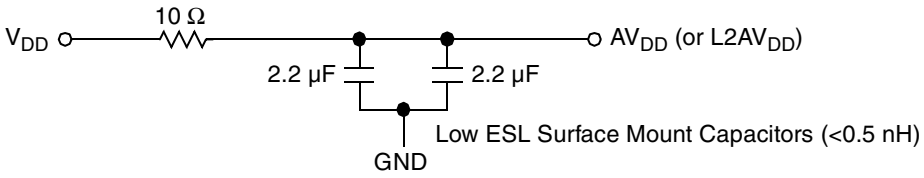


Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8323E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8323E system, and the MPC8323E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pins of the MPC8323E. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, or GV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, OV_{DD}, and GND pins of the MPC8323E.

24.5 Output Buffer DC Impedance

The MPC8323E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The

output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

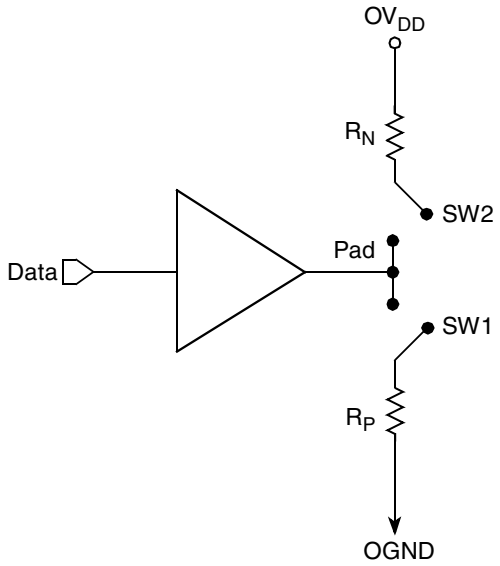


Figure 45. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 65 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 65. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

24.6 Configuration Pin Multiplexing

The MPC8323E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.