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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8323zqadc

1 Overview

The MPC8323E incorporates the e300c2 (MPC603e-based) core built on Power Architecture® technology, which includes 16 Kbytes of L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The e300c2 core does not contain a floating point unit (FPU). The MPC8323E also includes a 32-bit PCI controller, four DMA channels, a security engine, and a 32-bit DDR1/DDR2 memory controller.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8323E. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). Note that the MPC8321 and MPC8321E do not support UTOPIA. A block diagram of the MPC8323E is shown in Figure 1.

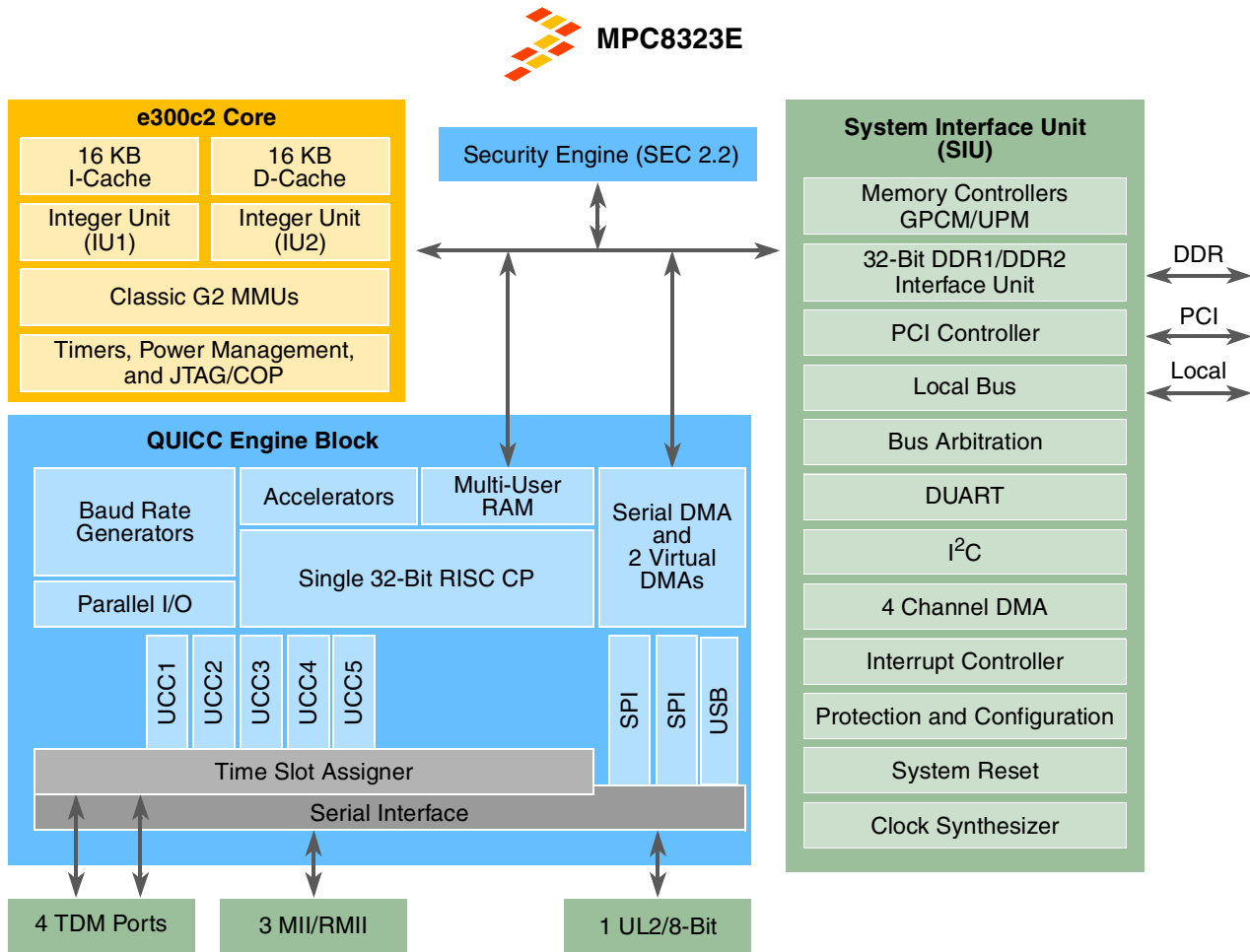


Figure 1. MPC8323E Block Diagram

Each of the five UCCs can support a variety of communication protocols: 10/100 Mbps Ethernet, serial ATM, HDLC, UART, and BISYNC—and, in the MPC8323E and MPC8323, multi-PHY ATM and ATM support for up to OC-3 speeds.

1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i™ standard, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8323E DDR1/DDR2 memory controller includes the following features:

- Single 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266-MHz data rate
- Support for two $\times 16$ devices
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O
- Support for 1 chip select only
- FCRAM, ECC, hardware/software calibration, bit deskew, QIN stage, or atomic logic are not supported.

1.5 PCI Controller

The MPC8323E PCI controller includes the following features:

- *PCI Specification Revision 2.3* compatible
- Single 32-bit data PCI interface operates up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

1.6 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 35 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

Table 6. Estimated Typical I/O Power Dissipation (continued)

Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 32 bits	—	—	0.12	W	—
PCI I/O load = 30 pF	66 MHz, 32 bits	—	—	0.057	W	—
QUICC Engine block and other I/Os	UTOPIA 8-bit 31 PHYs	—	—	0.041	W	Multiply by number of interfaces used.
	TDM serial	—	—	0.001	W	
	TDM nibble	—	—	0.004	W	
	HDLC/TRAN serial	—	—	0.003	W	
	HDLC/TRAN nibble	—	—	0.025	W	
	DUART	—	—	0.017	W	
	MIIs	—	—	0.009	W	
	RMII	—	—	0.009	W	
	Ethernet management	—	—	0.002	W	
	USB	—	—	0.001	W	
	SPI	—	—	0.001	W	
	Timer output	—	—	0.002	W	

NOTE

AV_{DDn} (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	$OV_{DD} + 0.3$	V
Input low voltage	—	V_{IL}	-0.3	0.4	V

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
$\overline{\text{HRESET}}/\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8323E is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

- $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is in PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
- t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
- POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	μs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{\text{OH}} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{\text{OL}} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$\text{OV}_{\text{DD}} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—

Table 11. Reset Signals DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA	—

Note:

1. This specification applies when operating from 3.3 V supply.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR1 and DDR2 SDRAM interface of the MPC8323E. Note that DDR1 SDRAM is $Dn_GV_{DD}(\text{typ}) = 2.5\text{ V}$ and DDR2 SDRAM is $Dn_GV_{DD}(\text{typ}) = 1.8\text{ V}$. The AC electrical specifications are the same for DDR1 and DDR2 SDRAM.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8323E when $Dn_GV_{DD}(\text{typ}) = 1.8\text{ V}$.

Table 12. DDR2 SDRAM DC Electrical Characteristics for $Dn_GV_{DD}(\text{typ}) = 1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	Dn_GV_{DD}	1.71	1.89	V	1
I/O reference voltage	$MVREFn_{REF}$	$0.49 \times Dn_GV_{DD}$	$0.51 \times Dn_GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MVREFn_{REF} - 0.04$	$MVREFn_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MVREFn_{REF} + 0.125$	$Dn_GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MVREFn_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	-9.9	9.9	μA	4
Output high current ($V_{OUT} = 1.35\text{ V}$)	I_{OH}	-13.4	—	mA	—
Output low current ($V_{OUT} = 0.280\text{ V}$)	I_{OL}	13.4	—	mA	—

Notes:

1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.
2. $MVREFn_{REF}$ is expected to be equal to $0.5 \times Dn_GV_{DD}$, and to track Dn_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on $MVREFn_{REF}$ may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to $MVREFn_{REF}$. This rail should track variations in the DC level of $MVREFn_{REF}$.
4. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq Dn_GV_{DD}$.

Table 13 provides the DDR2 capacitance when $Dn_GV_{DD}(\text{typ}) = 1.8\text{ V}$.

Table 13. DDR2 SDRAM Capacitance for $Dn_GV_{DD}(\text{typ}) = 1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1

(management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in [Section 8.3, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 DC Electrical Characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in [Table 22](#).

Table 22. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$OV_{DD} = \text{Min}$	2.40	$OV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$OV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	-0.3	0.90	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$		—	± 5	μA

8.2 MII and RMII AC Timing Specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

[Table 23](#) provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of $3.3 \text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise time	t_{MTXR}	1.0	—	4.0	ns

Table 23. MII Transmit AC Timing Specifications (continued)

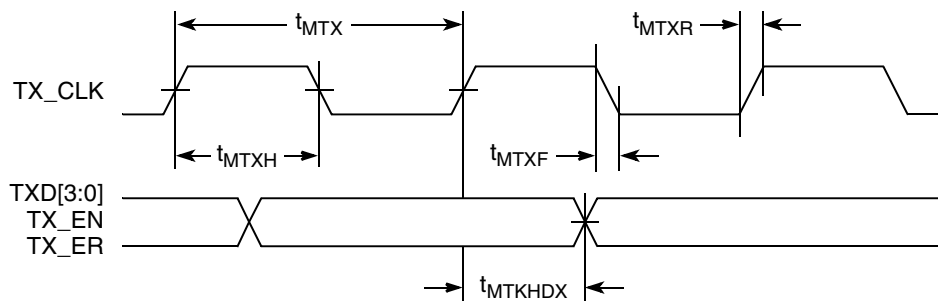
 At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
TX_CLK data clock fall time	t_{MTXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 7 shows the MII transmit AC timing diagram.


Figure 7. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

 At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time	t_{MRXR}	1.0	—	4.0	ns

Table 26. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit
REF_CLK clock fall time $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load.

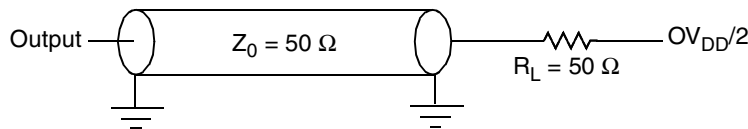


Figure 11. AC Test Load

Figure 12 shows the RMII receive AC timing diagram.

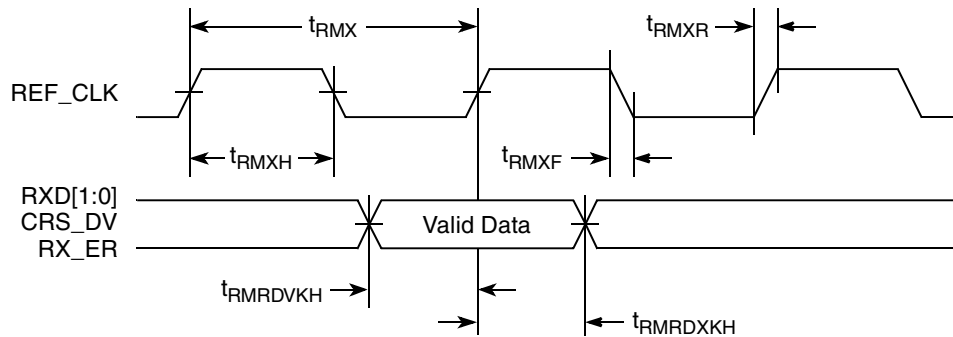


Figure 12. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in [Section 8.1, “Ethernet Controller \(10/100 Mbps\)—MII/RMII Electrical Characteristics.”](#)

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 27](#).

Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—	2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$ $OV_{DD} = \text{Min}$	2.10	$OV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$ $OV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	2.00	—	V
Input low voltage	V_{IL}	—	—	0.80	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

8.3.2 MII Management AC Electrical Specifications

[Table 28](#) provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typical	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 13 shows the MII management AC timing diagram.

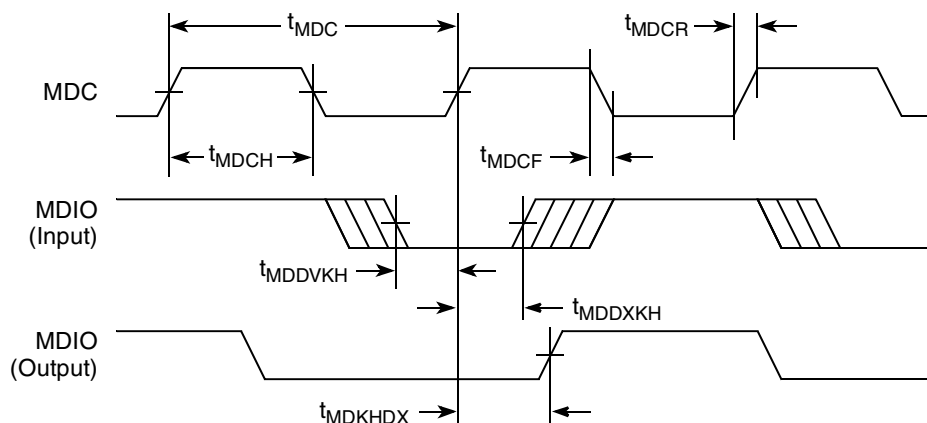


Figure 13. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8323E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V
Input current	I_{IN}	—	± 5	μA

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8323E.

Table 30. Local Bus General Timing Parameters

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK n)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK n)	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5

Table 31. JTAG Interface DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E. [Table 32](#) provides the JTAG AC timing specifications as defined in [Figure 19](#) through [Figure 22](#).

Table 32. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see [Table 2](#)).

Parameter	Symbol ²	Min	Max	Unit	Notes	
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—	
JTAG external clock cycle time	t_{JTG}	30	—	ns	—	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	11	—	ns	—	
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—	
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3	
Input setup times:	Boundary-scan data TMS, TDI	t_{JTDVKH}	4	—	ns	4
		t_{JTIVKH}	4	—		
Input hold times:	Boundary-scan data TMS, TDI	t_{JTDXKH}	10	—	ns	4
		t_{JTIXKH}	10	—		
Valid times:	Boundary-scan data TDO	t_{JTKLDV}	2	15	ns	5
		t_{JTKLOV}	2	15		
Output hold times:	Boundary-scan data TDO	t_{JTKLDX}	2	—	ns	5
		t_{JTKLOX}	2	—		

18 UTOPIA

This section describes the UTOPIA DC and AC electrical specifications of the MPC8323E.

NOTE

The MPC8321E and MPC8321 do not support UTOPIA.

18.1 UTOPIA DC Electrical Characteristics

Table 48 provides the DC electrical characteristics for the MPC8323E UTOPIA.

Table 48. UTOPIA DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 5	μA

18.2 UTOPIA AC Timing Specifications

Table 49 provides the UTOPIA input and output AC timing specifications.

Table 49. UTOPIA AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
UTOPIA outputs—Internal clock delay	t_{UIKHOV}	0	5.5	ns
UTOPIA outputs—External clock delay	t_{UEKHOV}	1	8	ns
UTOPIA outputs—Internal clock high impedance	t_{UIKHOX}	0	5.5	ns
UTOPIA outputs—External clock high impedance	t_{UEKHOX}	1	8	ns
UTOPIA inputs—Internal clock input setup time	t_{UIIVKH}	8	—	ns
UTOPIA inputs—External clock input setup time	t_{UEIVKH}	4	—	ns
UTOPIA inputs—Internal clock input hold time	t_{UIIXKH}	0	—	ns
UTOPIA inputs—External clock input hold time	t_{UEIXKH}	1	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Supplies				
AV _{DD1}	P3	I	AV _{DD1}	—
AV _{DD2}	AA1	I	AV _{DD2}	—
AV _{DD3}	AB15	I	AV _{DD3}	—
AV _{DD4}	C24	I	AV _{DD4}	—
MVREF1	AB8	I	DDR reference voltage	—
MVREF2	AB17	I	DDR reference voltage	—
PCI				
PCI_INTA /IRQ_OUT	AF2	O	OV _{DD}	2
PCI_RESET_OUT	AE2	O	OV _{DD}	—
PCI_AD0/MSRCID0 (DDR ID)	L1	IO	OV _{DD}	—
PCI_AD1/MSRCID1 (DDR ID)	L2	IO	OV _{DD}	—
PCI_AD2/MSRCID2 (DDR ID)	M1	IO	OV _{DD}	—
PCI_AD3/MSRCID3 (DDR ID)	M2	IO	OV _{DD}	—
PCI_AD4/MSRCID4 (DDR ID)	L3	IO	OV _{DD}	—
PCI_AD5/MDVAL (DDR ID)	N1	IO	OV _{DD}	—
PCI_AD6	N2	IO	OV _{DD}	—
PCI_AD7	M3	IO	OV _{DD}	—
PCI_AD8	P1	IO	OV _{DD}	—
PCI_AD9	R1	IO	OV _{DD}	—
PCI_AD10	N3	IO	OV _{DD}	—
PCI_AD11	N4	IO	OV _{DD}	—
PCI_AD12	T1	IO	OV _{DD}	—
PCI_AD13	R2	IO	OV _{DD}	—
PCI_AD14/ECID_TMODE_IN	T2	IO	OV _{DD}	—
PCI_AD15	U1	IO	OV _{DD}	—
PCI_AD16	Y2	IO	OV _{DD}	—
PCI_AD17	Y1	IO	OV _{DD}	—
PCI_AD18	AA2	IO	OV _{DD}	—
PCI_AD19	AB1	IO	OV _{DD}	—

22.1 Clocking in PCI Host Mode

When the MPC8323E is configured as a PCI host device ($RCWH[PCIHOST] = 1$), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider ($\div 2$) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexors. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

22.1.1 PCI Clock Outputs (PCI_CLK_OUT[0:2])

When the MPC8323E is configured as a PCI host, it provides three separate clock output signals, PCI_CLK_OUT[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOEn] bit. All output clocks are phase-aligned to each other.

22.2 Clocking in PCI Agent Mode

When the MPC8323E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND, and the clock output signals, PCI_CLK_OUT $_n$ and PCI_SYNC_OUT, are not used.

22.3 System Clock Domains

As shown in [Figure 43](#), the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*ce_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lb_clk*)

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = [PCI_SYNC_IN \times (1 + \sim\overline{CFG_CLKIN_DIV})] \times SPMF$$

In PCI host mode, $PCI_SYNC_IN \times (1 + \sim\overline{CFG_CLKIN_DIV})$ is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300c2 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See the “Reset Configuration” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

Clocking

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF]) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

When CLKIN is the primary input clock,

$$ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$$

When PCI_CLK is the primary input clock,

$$ce_clk = [\text{primary clock input} \times \text{CEPMF} \times (1 + \sim\text{CFG_CLKIN_DIV})] \div (1 + \text{CEPDF})$$

See the “QUICC Engine PLL Multiplication Factor” section and the “QUICC Engine PLL Division Factor” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

The DDR SDRAM memory controller operates with a frequency equal to twice the frequency of *csb_clk*. Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider ($\div 2$) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The local bus memory controller operates with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBC clock divider ratio is controlled by LCRR[CLKDIV]. See the “LBC Bus Clock and Clock Ratios” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for more information.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 56 specifies which units have a configurable clock frequency. Refer to the “System Clock Control Register (SCCR)” section in the *MPC8323E PowerQUICC II Pro Communications Processor Reference Manual* for a detailed description.

Table 56. Configurable Clock Units

Unit	Default Frequency	Options
Security core, I2C, SAP, TPR	<i>csb_clk</i>	Off, <i>csb_clk</i> /2, <i>csb_clk</i> /3
PCI and DMA complex	<i>csb_clk</i>	Off, <i>csb_clk</i>

NOTE

Setting the clock ratio of these units must be performed prior to any access to them.

Table 57 provides the operating frequencies for the 8323E PBGA under recommended operating conditions (see Table 2).

Table 57. Operating Frequencies for PBGA

Characteristic ¹	Max Operating Frequency	Unit
e300 core frequency (<i>core_clk</i>)	333	MHz
Coherent system bus frequency (<i>csb_clk</i>)	133	MHz
QUICC Engine frequency (<i>ce_clk</i>)	200	MHz

22.7 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8323E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the `csb_clk` as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. [Table 63](#) shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

Table 63. Suggested PLL Configurations

Conf No.	SPMF	Core PLL	CEMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0110	0	33.33	133.33	266.66	200
2	0100	0000101	1000	0	25	100	250	200
3	0010	0000100	0011	0	66.67	133.33	266.66	200
4	0100	0000101	0110	0	33.33	133.33	333.33	200
5	0101	0000101	1000	0	25	125	312.5	200
6	0010	0000101	0011	0	66.67	133.33	333.33	200

23 Thermal

This section describes the thermal specifications of the MPC8323E.

23.1 Thermal Characteristics

[Table 64](#) provides the package thermal characteristics for the 516 27 × 27 mm PBGA of the MPC8323E.

Table 64. Package Thermal Characteristics for PBGA

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	21	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	23	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	13	°C/W	4
Junction-to-case	—	$R_{\theta JC}$	9	°C/W	5

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta IA} = R_{\theta IC} + R_{\theta CA}$$

interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

P_D = power dissipation (W)

24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8323E.

24.1 System Clocking

The MPC8323E includes three PLLs.

- The system PLL (AV_{DD}2) generates the system clock from the externally supplied CLKIN input. The frequency ratio between the system and CLKIN is selected using the system PLL ratio configuration bits as described in [Section 22.4, “System PLL Configuration.”](#)
- The e300 core PLL (AV_{DD}3) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in [Section 22.5, “Core PLL Configuration.”](#)
- The QUICC Engine PLL (AV_{DD}1) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each AV_{DD}ⁿ pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in [Figure 44](#), one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

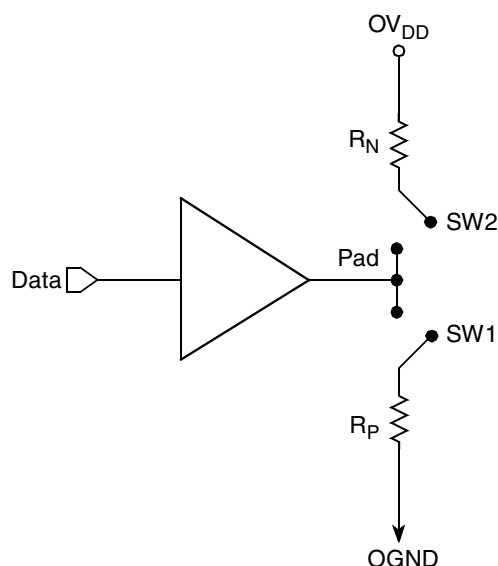


Figure 45. Driver Impedance Measurement

The value of this resistance and the strength of the driver’s current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 65 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 65. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, $T_j = 105^\circ\text{C}$.

24.6 Configuration Pin Multiplexing

The MPC8323E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

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