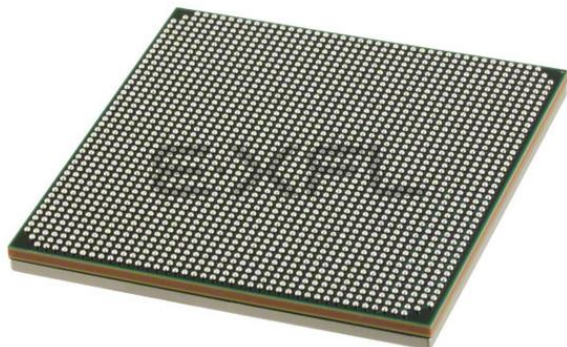




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Details

Product Status	Active
Number of LABs/CLBs	89000
Number of Logic Elements/Cells	1139200
Total RAM Bits	69304320
Number of I/O	720
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1926-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx1140t-2flg1926c

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and **Table 20** (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVTTTL_S4	1.31	1.42	1.64	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVTTTL_S8	1.31	1.42	1.64	3.50	3.64	3.73	4.26	4.50	4.72	ns
LVTTTL_S12	1.31	1.42	1.64	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVTTTL_S16	1.31	1.42	1.64	3.03	3.17	3.26	3.79	4.03	4.25	ns
LVTTTL_S24	1.31	1.42	1.64	3.25	3.39	3.48	4.01	4.25	4.47	ns
LVTTTL_F4	1.31	1.42	1.64	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVTTTL_F8	1.31	1.42	1.64	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVTTTL_F12	1.31	1.42	1.64	2.69	2.82	2.92	3.45	3.68	3.91	ns
LVTTTL_F16	1.31	1.42	1.64	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVTTTL_F24	1.31	1.42	1.64	2.41	2.64	2.89	3.17	3.50	3.88	ns
LVDS_25 ⁽¹⁾	0.64	0.68	0.80	1.36	1.47	1.55	2.12	2.33	2.54	ns
MINI_LVDS_25	0.68	0.70	0.79	1.36	1.47	1.55	2.12	2.33	2.54	ns
BLVDS_25 ⁽¹⁾	0.65	0.69	0.80	1.83	2.02	2.20	2.59	2.88	3.19	ns
RSDS_25 (point to point) ⁽¹⁾	0.63	0.68	0.79	1.36	1.48	1.55	2.12	2.34	2.54	ns
PPDS_25 ⁽¹⁾	0.65	0.69	0.80	1.36	1.49	1.58	2.12	2.35	2.57	ns
TMDS_33 ⁽¹⁾	0.72	0.76	0.86	1.43	1.54	1.60	2.19	2.40	2.59	ns
PCI33_3 ⁽¹⁾	1.28	1.41	1.65	2.71	3.08	3.52	3.47	3.94	4.51	ns
HSUL_12	0.63	0.64	0.71	1.77	1.90	2.00	2.53	2.76	2.99	ns
DIFF_HSUL_12	0.58	0.61	0.70	1.55	1.68	1.78	2.31	2.54	2.77	ns
HSTL_I_S	0.61	0.64	0.73	1.55	1.69	1.80	2.31	2.55	2.79	ns
HSTL_II_S	0.61	0.64	0.73	1.21	1.34	1.43	1.97	2.20	2.42	ns
HSTL_I_18_S	0.64	0.67	0.76	1.28	1.39	1.45	2.04	2.25	2.44	ns
HSTL_II_18_S	0.64	0.67	0.76	1.18	1.31	1.40	1.94	2.17	2.39	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	1.42	1.54	1.61	2.18	2.40	2.60	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	1.15	1.24	1.27	1.91	2.10	2.26	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	1.27	1.38	1.43	2.03	2.24	2.42	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	1.14	1.23	1.26	1.90	2.09	2.25	ns
HSTL_I_F	0.61	0.64	0.73	1.10	1.19	1.23	1.86	2.05	2.22	ns

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
HSTL_II_F	0.61	0.64	0.73	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_I_18_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_II_18_F	0.64	0.67	0.76	1.03	1.14	1.23	1.79	2.00	2.22	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	1.09	1.18	1.22	1.85	2.04	2.21	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	1.02	1.11	1.14	1.78	1.97	2.13	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	1.08	1.17	1.21	1.84	2.03	2.20	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	1.01	1.10	1.13	1.77	1.96	2.12	ns
LVC MOS33_S4	1.31	1.40	1.60	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVC MOS33_S8	1.31	1.40	1.60	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVC MOS33_S12	1.31	1.40	1.60	3.05	3.18	3.28	3.81	4.04	4.27	ns
LVC MOS33_S16	1.31	1.40	1.60	3.06	3.43	3.88	3.82	4.29	4.87	ns
LVC MOS33_F4	1.31	1.40	1.60	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVC MOS33_F8	1.31	1.40	1.60	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVC MOS33_F12	1.31	1.40	1.60	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVC MOS33_F16	1.31	1.40	1.60	2.44	2.69	2.96	3.20	3.55	3.95	ns
LVC MOS25_S4	1.08	1.16	1.32	3.08	3.22	3.31	3.84	4.08	4.30	ns
LVC MOS25_S8	1.08	1.16	1.32	2.85	2.98	3.07	3.61	3.84	4.06	ns
LVC MOS25_S12	1.08	1.16	1.32	2.44	2.57	2.67	3.20	3.43	3.66	ns
LVC MOS25_S16	1.08	1.16	1.32	2.79	2.92	3.01	3.55	3.78	4.00	ns
LVC MOS25_F4	1.08	1.16	1.32	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVC MOS25_F8	1.08	1.16	1.32	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS25_F12	1.08	1.16	1.32	2.15	2.29	2.52	2.91	3.15	3.51	ns
LVC MOS25_F16	1.08	1.16	1.32	1.92	2.17	2.45	2.68	3.03	3.44	ns
LVC MOS18_S4	0.64	0.66	0.74	1.55	1.68	1.78	2.31	2.54	2.77	ns
LVC MOS18_S8	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS18_S12	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS18_S16	0.64	0.66	0.74	1.49	1.62	1.72	2.25	2.48	2.71	ns
LVC MOS18_S24 ⁽¹⁾	0.64	0.66	0.74	1.74	1.92	2.08	2.50	2.78	3.07	ns
LVC MOS18_F4	0.64	0.66	0.74	1.38	1.51	1.61	2.14	2.37	2.60	ns
LVC MOS18_F8	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVC MOS18_F12	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVC MOS18_F16	0.64	0.66	0.74	1.52	1.68	1.81	2.28	2.54	2.80	ns
LVC MOS18_F24 ⁽¹⁾	0.64	0.66	0.74	1.34	1.46	1.55	2.10	2.32	2.54	ns
LVC MOS15_S4	0.66	0.69	0.81	1.86	2.00	2.09	2.62	2.86	3.08	ns
LVC MOS15_S8	0.66	0.69	0.81	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVC MOS15_S12	0.66	0.69	0.81	1.83	2.03	2.23	2.59	2.89	3.22	ns
LVC MOS15_S16	0.66	0.69	0.81	1.76	1.95	2.13	2.52	2.81	3.12	ns

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVC MOS15_F4	0.66	0.69	0.81	1.63	1.76	1.86	2.39	2.62	2.85	ns
LVC MOS15_F8	0.66	0.69	0.81	1.79	1.99	2.18	2.55	2.85	3.17	ns
LVC MOS15_F12	0.66	0.69	0.81	1.40	1.54	1.65	2.16	2.40	2.64	ns
LVC MOS15_F16	0.66	0.69	0.81	1.37	1.51	1.61	2.13	2.37	2.60	ns
LVC MOS12_S4	0.88	0.91	1.00	2.53	2.67	2.76	3.29	3.53	3.75	ns
LVC MOS12_S8	0.88	0.91	1.00	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVC MOS12_S12 ⁽¹⁾	0.88	0.91	1.00	1.75	1.89	1.98	2.51	2.75	2.97	ns
LVC MOS12_F4	0.88	0.91	1.00	1.94	2.07	2.17	2.70	2.93	3.16	ns
LVC MOS12_F8	0.88	0.91	1.00	1.50	1.64	1.73	2.26	2.50	2.72	ns
LVC MOS12_F12 ⁽¹⁾	0.88	0.91	1.00	1.54	1.71	1.87	2.30	2.57	2.86	ns
SSTL135_S	0.61	0.64	0.73	1.27	1.40	1.50	2.03	2.26	2.49	ns
SSTL15_S	0.61	0.64	0.73	1.24	1.37	1.47	2.00	2.23	2.46	ns
SSTL18_I_S	0.64	0.67	0.76	1.59	1.74	1.85	2.35	2.60	2.84	ns
SSTL18_II_S	0.64	0.67	0.76	1.27	1.40	1.50	2.03	2.26	2.49	ns
DIFF_SSTL135_S	0.59	0.61	0.73	1.27	1.40	1.50	2.03	2.26	2.49	ns
DIFF_SSTL15_S	0.63	0.67	0.77	1.24	1.37	1.47	2.00	2.23	2.46	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	1.50	1.63	1.72	2.26	2.49	2.71	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	1.13	1.22	1.25	1.89	2.08	2.24	ns
SSTL135_F	0.61	0.64	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
SSTL15_F	0.61	0.64	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
SSTL18_I_F	0.64	0.67	0.76	1.12	1.22	1.26	1.88	2.08	2.25	ns
SSTL18_II_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
DIFF_SSTL135_F	0.59	0.61	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
DIFF_SSTL15_F	0.63	0.67	0.77	1.04	1.17	1.26	1.80	2.03	2.25	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	1.10	1.19	1.23	1.86	2.05	2.22	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	1.02	1.10	1.14	1.78	1.96	2.13	ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 23: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{ODCK} /T _{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.45/−0.13	0.50/−0.13	0.58/−0.13	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T _{OSRCK} /T _{OCKSR}	SR pin setup/hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.49/−0.16	0.56/−0.16	0.68/−0.16	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Combinatorial					
T _{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	ns
Sequential Delays					
T _{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	ns
T _{RQ_OLOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	ns
T _{GSRQ_OLOGICE2}	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
T _{RQ_OLOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	ns
T _{GSRQ_OLOGICE3}	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
T _{RPW_OLOGICE2}	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	ns, Min
T _{RPW_OLOGICE3}	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	ns, Min

Table 27: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IO_FIFO Clock to Out Delays					
T _{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags	0.59	0.62	0.81	ns
Setup/Hold					
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.43/−0.01	0.47/−0.01	0.53/−0.01	ns
T _{IFFCCK_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.39/−0.01	0.43/−0.01	0.50/−0.01	ns
T _{OFFCCK_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	ns
Minimum Pulse Width					
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
Maximum Frequency					
F _{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	MHz

CLB Switching Characteristics

Table 28: CLB Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Combinatorial Delays					
T _{ILO}	An – Dn LUT address to A	0.05	0.05	0.06	ns, Max
T _{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.15	0.16	0.19	ns, Max
T _{ILO_3}	An – Dn LUT address to BMUX_A	0.24	0.25	0.30	ns, Max
T _{ITO}	An – Dn inputs to A – D Q outputs	0.58	0.61	0.74	ns, Max
T _{AXA}	AX inputs to AMUX output	0.38	0.40	0.49	ns, Max
T _{AXB}	AX inputs to BMUX output	0.40	0.42	0.52	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.41	0.50	ns, Max
T _{AXD}	AX inputs to DMUX output	0.43	0.44	0.52	ns, Max
T _{BXB}	BX inputs to BMUX output	0.31	0.33	0.40	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.39	0.47	ns, Max
T _{CXC}	CX inputs to CMUX output	0.27	0.28	0.34	ns, Max
T _{CXD}	CX inputs to DMUX output	0.33	0.34	0.41	ns, Max
T _{DXD}	DX inputs to DMUX output	0.32	0.33	0.40	ns, Max
Sequential Delays					
T _{CKO}	Clock to AQ – DQ outputs	0.26	0.27	0.32	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.32	0.32	0.39	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T _{AS} /T _{AH}	A _N – D _N input to CLK on A – D flip-flops	0.01/0.12	0.02/0.13	0.03/0.18	ns, Min
T _{DICK} /T _{CKDI}	A _X – D _X input to CLK on A – D flip-flops	0.04/0.14	0.04/0.14	0.05/0.20	ns, Min
	A _X – D _X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.36/0.10	0.37/0.11	0.46/0.16	ns, Min
T _{CECK_CLB} /T _{CKCE_CLB}	CE input to CLK on A – D flip-flops	0.19/0.05	0.20/0.05	0.25/0.05	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops	0.30/0.05	0.31/0.07	0.37/0.09	ns, Min
Set/Reset					
T _{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.38	0.38	0.46	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.34	0.35	0.43	ns, Max
F _{TOG}	Toggle frequency (for export control)	1818	1818	1818	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T _{SHCKO} ⁽¹⁾	Clock to A – B outputs	0.68	0.70	0.85	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	ns, Min
T _{CECK_LRAM} /T _{CKCE_LRAM}	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	ns, Min
Clock CLK					
T _{MPW}	Minimum pulse width	0.68	0.77	0.91	ns, Min
T _{MCP}	Minimum clock period	1.35	1.54	1.82	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T _{REG}	Clock to A – D outputs	0.96	0.98	1.20	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{WS_SHFREG} /T _{WH_SHFREG}	WE input	0.26/0.09	0.27/0.09	0.33/0.09	ns, Min
T _{CECK_SHFREG} /T _{CKCE_SHFREG}	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	ns, Min
T _{DS_SHFREG} /T _{DH_SHFREG}	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	ns, Min
Clock CLK					
T _{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	ns, Min

DSP48E1 Switching Characteristics

Table 32: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock					
T _{DSPDCK_A_AREG} / T _{DSPCKD_A_AREG}	A input to A register CLK	0.24/0.12	0.27/0.14	0.31/0.16	ns
T _{DSPDCK_B_BREG} /T _{DSPCKD_B_BREG}	B input to B register CLK	0.28/0.13	0.32/0.14	0.39/0.15	ns
T _{DSPDCK_C_CREG} /T _{DSPCKD_C_CREG}	C input to C register CLK	0.15/0.15	0.17/0.17	0.20/0.20	ns
T _{DSPDCK_D_DREG} /T _{DSPCKD_D_DREG}	D input to D register CLK	0.21/0.19	0.27/0.22	0.35/0.26	ns
T _{DSPDCK_ACIN_AREG} /T _{DSPCKD_ACIN_AREG}	ACIN input to A register CLK	0.21/0.12	0.24/0.14	0.27/0.16	ns
T _{DSPDCK_BCIN_BREG} /T _{DSPCKD_BCIN_BREG}	BCIN input to B register CLK	0.22/0.13	0.25/0.14	0.30/0.15	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock					
T _{DSPDCK_{A,B}_MREG_MULT} /T _{DSPCKD_B_MREG_MULT}	{A, B,} input to M register CLK using multiplier	2.04/–0.01	2.34/–0.01	2.79/–0.01	ns
T _{DSPDCK_{A,B}_ADREG} / T _{DSPCKD_D_ADREG}	{A, D} input to AD register CLK	1.09/–0.02	1.25/–0.02	1.49/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock					
T _{DSPDCK_{A,B}_PREG_MULT} /T _{DSPCKD_{A,B}_PREG_MULT}	{A, B,} input to P register CLK using multiplier	3.41/–0.24	3.90/–0.24	4.64/–0.24	ns
T _{DSPDCK_D_PREG_MULT} /T _{DSPCKD_D_PREG_MULT}	D input to P register CLK using multiplier	3.33/–0.62	3.81/–0.62	4.53/–0.62	ns
T _{DSPDCK_{A,B}_PREG} /T _{DSPCKD_{A,B}_PREG}	A or B input to P register CLK not using multiplier	1.47/–0.24	1.68/–0.24	2.00/–0.24	ns
T _{DSPDCK_C_PREG} /T _{DSPCKD_C_PREG}	C input to P register CLK not using multiplier	1.30/–0.22	1.49/–0.22	1.78/–0.22	ns
T _{DSPDCK_PCIN_PREG} /T _{DSPCKD_PCIN_PREG}	PCIN input to P register CLK	1.12/–0.13	1.28/–0.13	1.52/–0.13	ns
Setup and Hold Times of the CE Pins					
T _{DSPDCK_{CEA;CEB}_{AREG;BREG}} /T _{DSPCKD_{CEA;CEB}_{AREG;BREG}}	{CEA; CEB} input to {A; B} register CLK	0.30/0.05	0.36/0.06	0.44/0.09	ns
T _{DSPDCK_CEC_CREG} /T _{DSPCKD_CEC_CREG}	CEC input to C register CLK	0.24/0.08	0.29/0.09	0.36/0.11	ns
T _{DSPDCK_CED_DREG} /T _{DSPCKD_CED_DREG}	CED input to D register CLK	0.31/–0.02	0.36/–0.02	0.44/–0.02	ns
T _{DSPDCK_CEM_MREG} /T _{DSPCKD_CEM_MREG}	CEM input to M register CLK	0.26/0.15	0.29/0.17	0.33/0.20	ns
T _{DSPDCK_CEP_PREG} / T _{DSPCKD_CEP_PREG}	CEP input to P register CLK	0.31/0.01	0.36/0.01	0.45/0.01	ns
Setup and Hold Times of the RST Pins					
T _{DSPDCK_{RSTA;RSTB}_{AREG;BREG}} /T _{DSPCKD_{RSTA;RSTB}_{AREG;BREG}}	{RSTA, RSTB} input to {A, B} register CLK	0.34/0.10	0.39/0.11	0.47/0.13	ns
T _{DSPDCK_RSTC_CREG} /T _{DSPCKD_RSTC_CREG}	RSTC input to C register CLK	0.06/0.22	0.07/0.24	0.08/0.26	ns
T _{DSPDCK_RSTD_DREG} /T _{DSPCKD_RSTD_DREG}	RSTD input to D register CLK	0.37/0.06	0.42/0.06	0.50/0.07	ns
T _{DSPDCK_RSTM_MREG} /T _{DSPCKD_RSTM_MREG}	RSTM input to M register CLK	0.18/0.18	0.20/0.21	0.23/0.24	ns
T _{DSPDCK_RSTP_PREG} /T _{DSPCKD_RSTP_PREG}	RSTP input to P register CLK	0.24/0.01	0.26/0.01	0.30/0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
T _{DSPDO_A_CARRYOUT_MULT}	A input to CARRYOUT output using multiplier	3.21	3.69	4.39	ns
T _{DSPDO_D_P_MULT}	D input to P output using multiplier	3.15	3.61	4.30	ns

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Clock to Outs from Input Register Clock to Cascading Output Pins					
T _{DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}}	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	ns
T _{DSPCKO_CARRYCASCOUT_{AREG, BREG}_MULT}	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	ns
T _{DSPCKO_CARRYCASCOUT_ BREG}	CLK (BREG) to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	ns
T _{DSPCKO_CARRYCASCOUT_ DREG_MULT}	CLK (DREG) to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	ns
T _{DSPCKO_CARRYCASCOUT_ CREG}	CLK (CREG) to CARRYCASCOUT output	1.64	1.88	2.23	ns
Maximum Frequency					
F _{MAX}	With all registers used	741.84	650.20	547.95	MHz
F _{MAX_PATDET}	With pattern detector	627.35	549.75	463.61	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG	412.20	360.75	303.77	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG	468.82	408.66	342.70	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect	468.82	408.66	342.58	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	MHz

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 40: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T _{ICKOF}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7V585T	5.63	6.20	6.97	ns
		XC7V2000T	N/A	5.66	6.35	ns
		XC7VX330T	5.41	5.97	6.71	ns
		XC7VX415T	5.46	5.96	6.70	ns
		XC7VX485T	5.29	5.84	6.57	ns
		XC7VX550T	5.45	6.02	6.76	ns
		XC7VX690T	5.46	6.02	6.76	ns
		XC7VX980T	N/A	6.12	6.87	ns
		XC7VX1140T	N/A	5.59	6.28	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 41: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T _{ICKOFFAR}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7V585T	6.81	7.53	8.44	ns
		XC7V2000T	N/A	6.00	6.73	ns
		XC7VX330T	6.31	6.97	7.83	ns
		XC7VX415T	6.36	6.90	7.69	ns
		XC7VX485T	6.20	6.86	7.69	ns
		XC7VX550T	6.66	7.37	8.27	ns
		XC7VX690T	6.69	7.37	8.27	ns
		XC7VX980T	N/A	7.47	8.37	ns
		XC7VX1140T	N/A	5.93	6.65	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 55: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

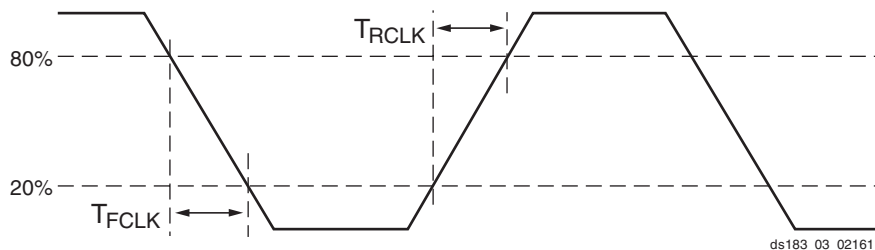


Figure 3: Reference Clock Timing Parameters

Table 56: GTX Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 57: GTX Transceiver User Clock Switching Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3/-2G ⁽³⁾	-2/-2L ⁽³⁾	-1 ⁽⁴⁾	
F _{TXOUT}	TXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F _{RXOUT}	RXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F _{RXIN}	RXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F _{TXIN2}	TXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz
F _{RXIN2}	RXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L, and -2G, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s. For speed grade -1C with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.500	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	40	–	ps
T _{FTX}	TX fall time	80%–20%	–	40	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500	ps
V _{TXOVBVDP}	Electrical idle amplitude		–	–	15	mV
T _{TXOVBTRANSITION}	Electrical idle transition time		–	–	140	ns
TJ _{12.5}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
DJ _{12.5}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{11.18}	Total jitter ⁽²⁾⁽⁴⁾	11.18 Gb/s	–	–	0.28	UI
DJ _{11.18}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{10.3125}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
DJ _{10.3125}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{9.953}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
DJ _{9.953}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{9.8}	Total jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	–	–	0.28	UI
DJ _{9.8}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{8.0}	Total jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	–	–	0.30	UI
DJ _{8.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.15	UI
TJ _{6.6_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	6.6 Gb/s	–	–	0.28	UI
DJ _{6.6_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI

Table 58: GTX Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
TJ _{6.6_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
DJ _{6.6_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
DJ _{5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
DJ _{4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.75}	Total jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	–	–	0.30	UI
DJ _{3.75}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
DJ _{3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
TJ _{3.20L}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁶⁾	–	–	0.32	UI
DJ _{3.20L}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
TJ _{2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁷⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.08	UI
TJ _{1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁸⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
TJ ₅₀₀	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s	–	–	0.10	UI
DJ ₅₀₀	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of $1e^{-12}$.
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the 7 Series FPGAs GTX/GTH Transceiver User Guide ([UG476](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: Gigabit Ethernet Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: XAUI Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: PCI Express Protocol Characteristics (GTX Transceivers)⁽¹⁾

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 ⁽³⁾	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 65: CPRI Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see [Table 64](#).

GTH Transceiver Specifications

GTH Transceiver DC Input and Output Levels

Table 66 summarizes the DC specifications of the GTH transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further details.

Table 66: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Absolute input voltage	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
DV _{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to 1010	–	–	800	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled	Equation based	V _{MGTAVTT} – DV _{PPOUT} /4			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based	V _{MGTAVTT} – DV _{PPOUT} /2			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)), and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

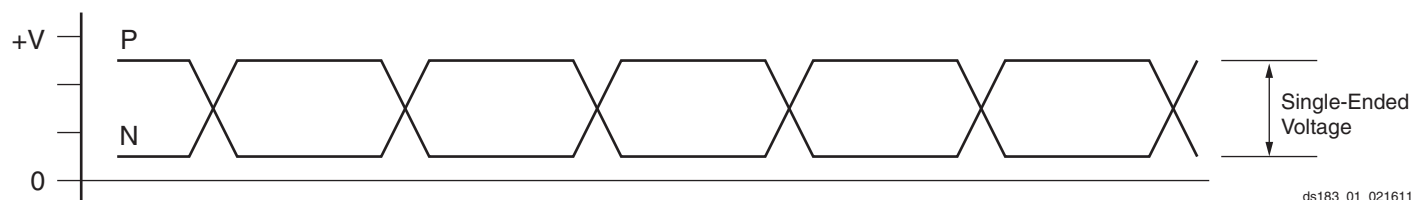


Figure 4: Single-Ended Peak-to-Peak Voltage

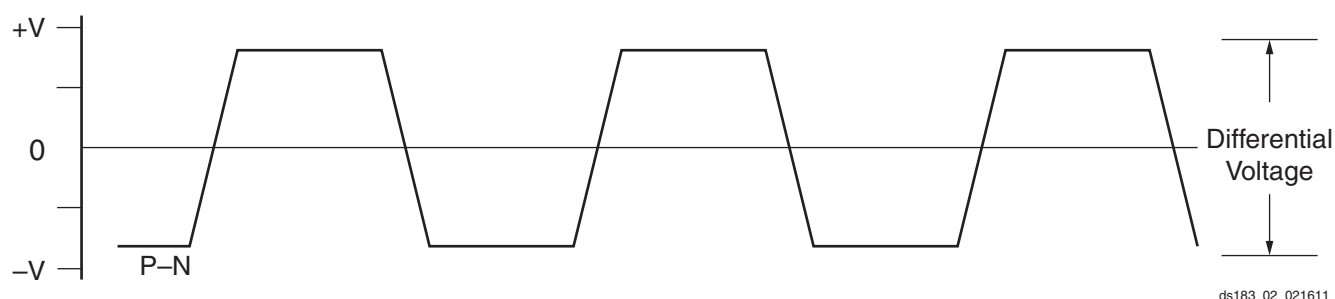


Figure 5: Differential Peak-to-Peak Voltage

Table 67 summarizes the DC specifications of the clock input of the GTH transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further details.

Table 67: GTH Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	350	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTH Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further information.

Table 68: GTH Transceiver Performance

Symbol	Description	Output Divider	Speed Grade			Units
			-3E/-2GE	-2(C&I)/-2LE	-1(C&I) ⁽¹⁾	
F _{GTHMAX}	Maximum GTH transceiver data rate		13.1	11.3	8.5	Gb/s
F _{GTHMIN}	Minimum GTH transceiver data rate		0.500	0.500	0.500	Gb/s
F _{GTHCRANGE}	CPLL line rate range	1	3.2–10.3125		3.2–8.0	Gb/s
		2	1.6–5.16		1.6–4.0	Gb/s
		4	0.8–2.58		0.8–2.0	Gb/s
		8	0.5–1.29		0.5–1.0	Gb/s
		16	N/A			Gb/s
F _{GTHQRANGE1}	QPLL line rate range 1	1	8.0–11.85	8.0–11.3	8.0–8.5	Gb/s
		2	4.0–5.925	4.0–5.65	4.0–4.25	Gb/s
		4	2.0–2.9625	2.0–2.825	2.0–2.125	Gb/s
		8	1.0–1.48125	1.0–1.4125	1.0–1.0625	Gb/s
		16	N/A			Gb/s
F _{GTHQRANGE2}	QPLL line rate range 2	1	11.85–13.1	N/A		Gb/s
		2	5.925–6.55	N/A		Gb/s
		4	2.96–3.275	N/A		Gb/s
		8	1.48–1.63	N/A		Gb/s
		16	0.74–0.81	N/A		Gb/s
F _{GCPLLRANGE}	GTH transceiver CPLL frequency range		1.6–5.16		1.6–4.0	GHz
F _{GQPLLRange1}	GTH transceiver QPLL frequency range 1		8.0–11.85	8.0–11.3	8.0–8.5	GHz
F _{GQPLLRange2}	GTH transceiver QPLL frequency range 2		11.85–13.1	N/A		GHz

Notes:

- The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), requires a 4-byte internal data width for operation above 3.8 Gb/s.

Table 69: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3/-2G	-2L	-2	-1	
F _{GTHDRPCLK}	GTHDRPCLK maximum frequency	175	175	175	156	MHz

XADC Specifications

Table 82: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, T _j = −40°C to 100°C, Typical values at T _j =+40°C						
ADC Accuracy ⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±6	LSBs
Gain Error		Gain calibration disabled	–	–	±0.5	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio ⁽²⁾	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion ⁽²⁾	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	–	70	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs ⁽³⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T _j = −40°C to 100°C.	–	–	±4	°C
		T _j = −55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −40°C to +100°C	–	–	±1	%
		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −55°C to +125°C	–	–	±2	%
Conversion Rate ⁽⁴⁾						
Conversion Time - Continuous	t _{CONV}	Number of ADCCLK cycles	26	–	32	cycle
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	cycle
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%

Table 83: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Master/Slave Serial Mode Programming Switching						
T _{DCCK} /T _{CCKD}	DIN setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{CCO}	DOUT clock to out		8.0	8.0	8.0	ns, Max
SelectMAP Mode Programming Switching						
T _{SMDCCK} /T _{SMCCKD}	D[31:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{SMWCCK} /T _{SMCCKW}	RDWR_B setup/hold		10.0/0.0	10.0/0.0	10.0/0.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)		7.0	7.0	7.0	ns, Max
T _{SMCO}	D[31:00] clock to out in readback		8.0	8.0	8.0	ns, Max
F _{RBCK}	Readback frequency	SLR-based	70	70	70	MHz, Max
		All other devices	100	100	100	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup/hold	SLR-based	9.0/2.0	9.0/2.0	9.0/2.0	ns, Min
		All other devices	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	SLR-based	17	17	17	ns, Max
		All other devices	7.0	7.0	7.0	ns, Max
F _{TCK}	TCK frequency	SLR-based	20	20	20	MHz, Max
		All other devices	66	66	66	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out		8.5	8.5	8.5	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPICCD}	D[03:00] setup/hold		3.0/0.0	3.0/0.0	3.0/0.0	ns, Min
T _{SPICCM}	MOSI clock to out		8.0	8.0	8.0	ns, Max
T _{SPICFC}	FCS_B clock to out		8.0	8.0	8.0	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* ([UG470](#)).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 84 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* ([UG470](#)).

Table 84: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

Date	Version	Description
03/27/2013	1.13	In Table 7 , added values for the XC7VX330T and XC7VX415T devices. Revised Table 15 and Table 16 to include production release of the XC7VX330T and XC7VX415T. In Table 18 , updated the table title, LPDDR2 values, and removed Note 3. Removed Note 2: <i>For QPLL line rate, the maximum line rate with the divider N set to 66 is 10.3125 Gb/s</i> from Table 68 .
04/17/2013	1.14	Updated the AC Switching Characteristics section with production release changes to Table 15 and Table 16 for XC7VX550T for all speed specifications. In Table 1 , revised V_{IN} (I/O input voltage) to match values in Table 4 and Table 5 , and combined Note 4 with old Note 5 and then added new Note 5 . Revised V_{IN} description and added Note 8 in Table 2 . Updated first 3 rows in Table 4 and Table 5 . Updated values and added new values to Table 7 . Also revised PCI33_3 voltage minimum in Table 10 to match values in Table 1 , Table 4 , and Table 5 . Added Note 1 to Table 12 and Table 13 . Throughout the data sheet (Table 29 , Table 30 , and Table 45) removed the obvious note "A Zero "0" Hold Time listing indicates no hold time or a negative hold time." Updated and clarified USRCLK data in Table 57 and Table 72 .

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