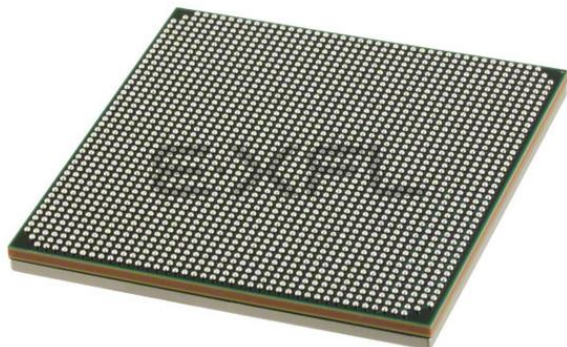




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	89000
Number of Logic Elements/Cells	1139200
Total RAM Bits	69304320
Number of I/O	480
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1928-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx1140t-2flg1928c

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 3.3V$	68	–	330	μA
	Pad pull-down (when selected) @ $V_{IN} = 1.8V$	45	–	180	μA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT} ⁽³⁾	Battery supply current	–	–	150	nA
R_{IN_TERM} ⁽⁴⁾	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

- Typical values are specified at nominal voltage, 25°C.
- This measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C.
- Termination resistance to a $V_{CCO}/2$ level.

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.55$	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

Notes:

- A total of 200 mA per bank should not be exceeded.

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Table 10: Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$			$V_{OCM}^{(3)}$			$V_{OD}^{(4)}$		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	—	—	—	1.250	—	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	$V_{CCO}-0.405$	$V_{CCO}-0.300$	$V_{CCO}-0.190$	0.400	0.600	0.800

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage ($Q - \bar{Q}$).
- V_{OCM} is the output common mode voltage.
- V_{OD} is the output differential voltage ($Q - \bar{Q}$).
- V_{OD} for BLVDS will vary significantly depending on topology and loading.
- LVDS_25 is specified in Table 12.
- LVDS is specified in Table 13.

Table 11: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$		$V_{OL}^{(3)}$	$V_{OH}^{(4)}$	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO}-0.400$	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO}-0.400$	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO}-0.400$	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO}-0.400$	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	—	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	—	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL12	0.300	0.600	0.850	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.600$	$(V_{CCO}/2) + 0.600$	13.4	–13.4

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage ($Q - \bar{Q}$).
- V_{OL} is the single-ended low-output voltage.
- V_{OH} is the single-ended high-output voltage.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-7 T and XT devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 12](#). In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 17: Networking Applications Interface Performances

Description	I/O Bank Type	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS receiver (SPI-4.2) ⁽¹⁾	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and **Table 20** (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVTTTL_S4	1.31	1.42	1.64	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVTTTL_S8	1.31	1.42	1.64	3.50	3.64	3.73	4.26	4.50	4.72	ns
LVTTTL_S12	1.31	1.42	1.64	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVTTTL_S16	1.31	1.42	1.64	3.03	3.17	3.26	3.79	4.03	4.25	ns
LVTTTL_S24	1.31	1.42	1.64	3.25	3.39	3.48	4.01	4.25	4.47	ns
LVTTTL_F4	1.31	1.42	1.64	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVTTTL_F8	1.31	1.42	1.64	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVTTTL_F12	1.31	1.42	1.64	2.69	2.82	2.92	3.45	3.68	3.91	ns
LVTTTL_F16	1.31	1.42	1.64	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVTTTL_F24	1.31	1.42	1.64	2.41	2.64	2.89	3.17	3.50	3.88	ns
LVDS_25 ⁽¹⁾	0.64	0.68	0.80	1.36	1.47	1.55	2.12	2.33	2.54	ns
MINI_LVDS_25	0.68	0.70	0.79	1.36	1.47	1.55	2.12	2.33	2.54	ns
BLVDS_25 ⁽¹⁾	0.65	0.69	0.80	1.83	2.02	2.20	2.59	2.88	3.19	ns
RSDS_25 (point to point) ⁽¹⁾	0.63	0.68	0.79	1.36	1.48	1.55	2.12	2.34	2.54	ns
PPDS_25 ⁽¹⁾	0.65	0.69	0.80	1.36	1.49	1.58	2.12	2.35	2.57	ns
TMDS_33 ⁽¹⁾	0.72	0.76	0.86	1.43	1.54	1.60	2.19	2.40	2.59	ns
PCI33_3 ⁽¹⁾	1.28	1.41	1.65	2.71	3.08	3.52	3.47	3.94	4.51	ns
HSUL_12	0.63	0.64	0.71	1.77	1.90	2.00	2.53	2.76	2.99	ns
DIFF_HSUL_12	0.58	0.61	0.70	1.55	1.68	1.78	2.31	2.54	2.77	ns
HSTL_I_S	0.61	0.64	0.73	1.55	1.69	1.80	2.31	2.55	2.79	ns
HSTL_II_S	0.61	0.64	0.73	1.21	1.34	1.43	1.97	2.20	2.42	ns
HSTL_I_18_S	0.64	0.67	0.76	1.28	1.39	1.45	2.04	2.25	2.44	ns
HSTL_II_18_S	0.64	0.67	0.76	1.18	1.31	1.40	1.94	2.17	2.39	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	1.42	1.54	1.61	2.18	2.40	2.60	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	1.15	1.24	1.27	1.91	2.10	2.26	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	1.27	1.38	1.43	2.03	2.24	2.42	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	1.14	1.23	1.26	1.90	2.09	2.25	ns
HSTL_I_F	0.61	0.64	0.73	1.10	1.19	1.23	1.86	2.05	2.22	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVDS	0.75	0.79	0.92	1.05	1.17	1.24	1.68	1.92	2.06	ns
HSUL_12	0.69	0.72	0.82	1.65	1.84	2.05	2.29	2.59	2.87	ns
DIFF_HSUL_12	0.69	0.72	0.82	1.65	1.84	2.05	2.29	2.59	2.87	ns
HSTL_I_S	0.68	0.72	0.82	1.15	1.28	1.38	1.79	2.03	2.20	ns
HSTL_II_S	0.68	0.72	0.82	1.05	1.17	1.26	1.69	1.93	2.08	ns
HSTL_I_18_S	0.70	0.72	0.82	1.12	1.24	1.34	1.75	2.00	2.16	ns
HSTL_II_18_S	0.70	0.72	0.82	1.06	1.18	1.26	1.70	1.94	2.08	ns
HSTL_I_12_S	0.68	0.72	0.82	1.14	1.27	1.37	1.78	2.02	2.20	ns
HSTL_I_DCI_S	0.68	0.72	0.82	1.11	1.23	1.33	1.74	1.99	2.15	ns
HSTL_II_DCI_S	0.68	0.72	0.82	1.05	1.17	1.26	1.69	1.93	2.08	ns
HSTL_II_T_DCI_S	0.70	0.72	0.82	1.15	1.28	1.38	1.78	2.03	2.20	ns
HSTL_I_DCI_18_S	0.70	0.72	0.82	1.11	1.23	1.33	1.74	1.99	2.15	ns
HSTL_II_DCI_18_S	0.70	0.72	0.82	1.05	1.16	1.24	1.69	1.92	2.06	ns
HSTL_II_T_DCI_18_S	0.70	0.72	0.82	1.11	1.23	1.33	1.74	1.99	2.15	ns
DIFF_HSTL_I_S	0.75	0.79	0.92	1.15	1.28	1.38	1.79	2.03	2.20	ns
DIFF_HSTL_II_S	0.75	0.79	0.92	1.05	1.17	1.26	1.69	1.93	2.08	ns
DIFF_HSTL_I_DCI_S	0.75	0.79	0.92	1.15	1.28	1.38	1.78	2.03	2.20	ns
DIFF_HSTL_II_DCI_S	0.75	0.79	0.92	1.05	1.17	1.26	1.69	1.93	2.08	ns
DIFF_HSTL_I_18_S	0.75	0.79	0.92	1.12	1.24	1.34	1.75	2.00	2.16	ns
DIFF_HSTL_II_18_S	0.75	0.79	0.92	1.06	1.18	1.26	1.70	1.94	2.08	ns
DIFF_HSTL_I_DCI_18_S	0.75	0.79	0.92	1.11	1.23	1.33	1.74	1.99	2.15	ns
DIFF_HSTL_II_DCI_18_S	0.75	0.79	0.92	1.05	1.16	1.24	1.69	1.92	2.06	ns
DIFF_HSTL_II_T_DCI_18_S	0.75	0.79	0.92	1.11	1.23	1.33	1.74	1.99	2.15	ns
HSTL_I_F	0.68	0.72	0.82	1.02	1.14	1.22	1.66	1.90	2.04	ns
HSTL_II_F	0.68	0.72	0.82	0.97	1.08	1.15	1.61	1.84	1.97	ns
HSTL_I_18_F	0.70	0.72	0.82	1.04	1.16	1.24	1.68	1.91	2.06	ns
HSTL_II_18_F	0.70	0.72	0.82	0.98	1.09	1.16	1.62	1.85	1.98	ns
HSTL_I_12_F	0.68	0.72	0.82	1.02	1.13	1.21	1.65	1.88	2.03	ns
HSTL_I_DCI_F	0.68	0.72	0.82	1.04	1.16	1.24	1.67	1.91	2.06	ns
HSTL_II_DCI_F	0.68	0.72	0.82	0.97	1.08	1.15	1.61	1.84	1.97	ns
HSTL_II_T_DCI_F	0.70	0.72	0.82	1.02	1.14	1.22	1.66	1.90	2.04	ns
HSTL_I_DCI_18_F	0.70	0.72	0.82	1.04	1.16	1.24	1.67	1.91	2.06	ns
HSTL_II_DCI_18_F	0.70	0.72	0.82	0.98	1.09	1.16	1.61	1.85	1.98	ns
HSTL_II_T_DCI_18_F	0.70	0.72	0.82	1.04	1.16	1.24	1.67	1.91	2.06	ns
DIFF_HSTL_I_F	0.75	0.79	0.92	1.02	1.14	1.22	1.66	1.90	2.04	ns
DIFF_HSTL_II_F	0.75	0.79	0.92	0.97	1.08	1.15	1.61	1.84	1.97	ns
DIFF_HSTL_I_DCI_F	0.75	0.79	0.92	1.02	1.14	1.22	1.66	1.90	2.04	ns
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.97	1.08	1.15	1.61	1.84	1.97	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVDCI_15	0.59	0.62	0.73	1.98	2.23	2.58	2.62	2.99	3.40	ns
LVDCI_DV2_18	0.47	0.50	0.60	1.99	2.15	2.34	2.62	2.90	3.17	ns
LVDCI_DV2_15	0.59	0.62	0.73	1.98	2.23	2.58	2.62	2.99	3.40	ns
HSLVDCI_18	0.68	0.72	0.82	1.99	2.15	2.35	2.62	2.91	3.17	ns
HSLVDCI_15	0.68	0.72	0.82	1.98	2.23	2.58	2.62	2.99	3.40	ns
SSTL18_I_S	0.68	0.72	0.82	1.02	1.15	1.24	1.66	1.90	2.07	ns
SSTL18_II_S	0.68	0.72	0.82	1.17	1.29	1.37	1.81	2.05	2.19	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.92	1.06	1.17	1.56	1.82	1.99	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.88	0.98	1.08	1.51	1.74	1.90	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.92	1.06	1.17	1.56	1.82	1.99	ns
SSTL15_S	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
SSTL135_S	0.69	0.72	0.82	0.97	1.10	1.19	1.60	1.85	2.01	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
SSTL12_S	0.69	0.72	0.82	0.96	1.09	1.18	1.60	1.84	2.00	ns
SSTL12_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	1.02	1.15	1.24	1.66	1.90	2.07	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	1.17	1.29	1.37	1.81	2.05	2.19	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.92	1.06	1.17	1.56	1.82	1.99	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.88	0.98	1.08	1.51	1.74	1.90	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.92	1.06	1.17	1.56	1.82	1.99	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
DIFF_SSTL135_S	0.69	0.72	0.82	0.97	1.10	1.19	1.60	1.85	2.01	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.96	1.09	1.18	1.60	1.84	2.00	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
SSTL18_I_F	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
SSTL18_II_F	0.68	0.72	0.82	0.97	1.09	1.16	1.61	1.84	1.99	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns

Input/Output Logic Switching Characteristics

Table 22: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{ICE1CK} /T _{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	ns
T _{ISRCK} /T _{ICKSR}	SR pin setup/hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	ns
T _{IDOCKE2} /T _{IOCKDE2}	D pin setup/hold with respect to CLK without delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	ns
T _{IDOCKDE2} /T _{IOCKDDE2}	DDL _Y pin setup/hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	ns
T _{IDOCKE3} /T _{IOCKDE3}	D pin setup/hold with respect to CLK without delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	ns
T _{IDOCKDE3} /T _{IOCKDDE3}	DDL _Y pin setup/hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	ns
Combinatorial					
T _{IDIE2}	D pin to O pin propagation delay, no delay (HP I/O banks only)	0.09	0.10	0.12	ns
T _{IDIDE2}	DDL _Y pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	ns
T _{IDIE3}	D pin to O pin propagation delay, no delay (HR I/O banks only)	0.09	0.10	0.12	ns
T _{IDIDE3}	DDL _Y pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	ns
Sequential Delays					
T _{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without delay (HP I/O banks only)	0.36	0.39	0.45	ns
T _{IDLODE2}	DDL _Y pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	ns
T _{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without delay (HR I/O banks only)	0.36	0.39	0.45	ns
T _{IDLODE3}	DDL _Y pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	ns
T _{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	ns
T _{RQ_ILOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	ns
T _{GSRQ_ILOGICE2}	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
T _{RQ_ILOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	ns
T _{GSRQ_ILOGICE3}	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
T _{RPW_ILOGICE2}	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	ns, Min
T _{RPW_ILOGICE3}	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 24: ISERDES Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold for Control Lines					
$T_{ISCK_BITSLIP}/T_{ISCK_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	ns
$T_{ISCK_CE} / T_{ISCK_CE}^{(2)}$	CE pin setup/hold with respect to CLK (for CE1)	0.39/−0.02	0.44/−0.02	0.63/−0.02	ns
$T_{ISCK_CE2} / T_{ISCK_CE2}^{(2)}$	CE pin setup/hold with respect to CLKDIV (for CE2)	−0.12/0.29	−0.12/0.31	−0.12/0.35	ns
Setup/Hold for Data Lines					
T_{ISDCK_D}/T_{ISCKD_D}	D pin setup/hold with respect to CLK	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_DDL}/T_{ISCKD_DDL}$	DDL pin setup/hold with respect to CLK (using IDELAY) ⁽¹⁾	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_D_DDR} / T_{ISCKD_D_DDR}$	D pin setup/hold with respect to CLK at DDR mode	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_DDL_DDR}/T_{ISCKD_DDL_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾	0.11/0.11	0.12/0.12	0.15/0.15	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCK_CE2} and T_{ISCK_CE2} are reported as T_{ISCK_CE}/T_{ISCK_CE} in the timing report.

Output Serializer/Deserializer Switching Characteristics

Table 25: OSERDES Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{OSDCK_D} /T _{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input setup/hold with respect to CLK	0.49/−0.15	0.56/−0.15	0.68/−0.15	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input setup/hold with respect to CLKDIV	0.27/−0.15	0.30/−0.15	0.34/−0.15	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T _{OSCCK_S}	SR (Reset) input setup with respect to CLKDIV	0.41	0.46	0.75	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Sequential Delays					
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	ns
Combinatorial					
T _{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Table 27: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IO_FIFO Clock to Out Delays					
T _{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags	0.59	0.62	0.81	ns
Setup/Hold					
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.43/−0.01	0.47/−0.01	0.53/−0.01	ns
T _{IFFCKC_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.39/−0.01	0.43/−0.01	0.50/−0.01	ns
T _{OFFCKC_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	ns
Minimum Pulse Width					
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
Maximum Frequency					
F _{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	MHz

DSP48E1 Switching Characteristics

Table 32: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock					
T _{DSPDCK_A_AREG} / T _{DSPCKD_A_AREG}	A input to A register CLK	0.24/0.12	0.27/0.14	0.31/0.16	ns
T _{DSPDCK_B_BREG} /T _{DSPCKD_B_BREG}	B input to B register CLK	0.28/0.13	0.32/0.14	0.39/0.15	ns
T _{DSPDCK_C_CREG} /T _{DSPCKD_C_CREG}	C input to C register CLK	0.15/0.15	0.17/0.17	0.20/0.20	ns
T _{DSPDCK_D_DREG} /T _{DSPCKD_D_DREG}	D input to D register CLK	0.21/0.19	0.27/0.22	0.35/0.26	ns
T _{DSPDCK_ACIN_AREG} /T _{DSPCKD_ACIN_AREG}	ACIN input to A register CLK	0.21/0.12	0.24/0.14	0.27/0.16	ns
T _{DSPDCK_BCIN_BREG} /T _{DSPCKD_BCIN_BREG}	BCIN input to B register CLK	0.22/0.13	0.25/0.14	0.30/0.15	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock					
T _{DSPDCK_{A,B}_MREG_MULT} /T _{DSPCKD_B_MREG_MULT}	{A, B,} input to M register CLK using multiplier	2.04/–0.01	2.34/–0.01	2.79/–0.01	ns
T _{DSPDCK_{A,B}_ADREG} / T _{DSPCKD_D_ADREG}	{A, D} input to AD register CLK	1.09/–0.02	1.25/–0.02	1.49/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock					
T _{DSPDCK_{A,B}_PREG_MULT} /T _{DSPCKD_{A,B}_PREG_MULT}	{A, B,} input to P register CLK using multiplier	3.41/–0.24	3.90/–0.24	4.64/–0.24	ns
T _{DSPDCK_D_PREG_MULT} /T _{DSPCKD_D_PREG_MULT}	D input to P register CLK using multiplier	3.33/–0.62	3.81/–0.62	4.53/–0.62	ns
T _{DSPDCK_{A,B}_PREG} /T _{DSPCKD_{A,B}_PREG}	A or B input to P register CLK not using multiplier	1.47/–0.24	1.68/–0.24	2.00/–0.24	ns
T _{DSPDCK_C_PREG} /T _{DSPCKD_C_PREG}	C input to P register CLK not using multiplier	1.30/–0.22	1.49/–0.22	1.78/–0.22	ns
T _{DSPDCK_PCIN_PREG} /T _{DSPCKD_PCIN_PREG}	PCIN input to P register CLK	1.12/–0.13	1.28/–0.13	1.52/–0.13	ns
Setup and Hold Times of the CE Pins					
T _{DSPDCK_{CEA;CEB}_{AREG;BREG}} /T _{DSPCKD_{CEA;CEB}_{AREG;BREG}}	{CEA; CEB} input to {A; B} register CLK	0.30/0.05	0.36/0.06	0.44/0.09	ns
T _{DSPDCK_CEC_CREG} /T _{DSPCKD_CEC_CREG}	CEC input to C register CLK	0.24/0.08	0.29/0.09	0.36/0.11	ns
T _{DSPDCK_CED_DREG} /T _{DSPCKD_CED_DREG}	CED input to D register CLK	0.31/–0.02	0.36/–0.02	0.44/–0.02	ns
T _{DSPDCK_CEM_MREG} /T _{DSPCKD_CEM_MREG}	CEM input to M register CLK	0.26/0.15	0.29/0.17	0.33/0.20	ns
T _{DSPDCK_CEP_PREG} / T _{DSPCKD_CEP_PREG}	CEP input to P register CLK	0.31/0.01	0.36/0.01	0.45/0.01	ns
Setup and Hold Times of the RST Pins					
T _{DSPDCK_{RSTA;RSTB}_{AREG;BREG}} /T _{DSPCKD_{RSTA;RSTB}_{AREG;BREG}}	{RSTA, RSTB} input to {A, B} register CLK	0.34/0.10	0.39/0.11	0.47/0.13	ns
T _{DSPDCK_RSTC_CREG} /T _{DSPCKD_RSTC_CREG}	RSTC input to C register CLK	0.06/0.22	0.07/0.24	0.08/0.26	ns
T _{DSPDCK_RSTD_DREG} /T _{DSPCKD_RSTD_DREG}	RSTD input to D register CLK	0.37/0.06	0.42/0.06	0.50/0.07	ns
T _{DSPDCK_RSTM_MREG} /T _{DSPCKD_RSTM_MREG}	RSTM input to M register CLK	0.18/0.18	0.20/0.21	0.23/0.24	ns
T _{DSPDCK_RSTP_PREG} /T _{DSPCKD_RSTP_PREG}	RSTP input to P register CLK	0.24/0.01	0.26/0.01	0.30/0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
T _{DSPDO_A_CARRYOUT_MULT}	A input to CARRYOUT output using multiplier	3.21	3.69	4.39	ns
T _{DSPDO_D_P_MULT}	D input to P output using multiplier	3.15	3.61	4.30	ns

Table 37: Duty Cycle Distortion and Clock Tree Skew

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
T _{DCD_CLK}	Global clock tree duty cycle distortion ⁽¹⁾	All	0.20	0.20	0.20	ns
T _{CKSKEW}	Global clock tree skew ⁽²⁾	XC7V585T	0.75	0.91	0.98	ns
		XC7V2000T	N/A	0.39	0.39	ns
		XC7VX330T	0.60	0.74	0.79	ns
		XC7VX415T	0.76	0.84	0.91	ns
		XC7VX485T	0.60	0.74	0.79	ns
		XC7VX550T	0.73	0.88	0.96	ns
		XC7VX690T	0.73	0.88	0.96	ns
		XC7VX980T	N/A	0.91	0.98	ns
		XC7VX1140T	N/A	0.39	0.39	ns
T _{DCD_BUFIN}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	ns
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	ns
T _{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip-flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements in a single SLR. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 38: MMCM Specification

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
MMCM_F _{INMAX}	Maximum input clock frequency	1066.00	933.00	800.00	MHz
MMCM_F _{INMIN}	Minimum input clock frequency	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
MMCM_F _{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	550.00	500.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs ⁽²⁾	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter	Note 3			
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision ⁽⁴⁾	0.20	0.20	0.20	ns

Table 38: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
MMCM_T _{LOCKMAX}	MMCM maximum Lock Time	100	100	100	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency	1066.00	933.00	800.00	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency ⁽⁵⁾⁽⁶⁾	4.69	4.69	4.69	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation	< 20% of clock input period or 1 ns Max			
MMCM_RST _{MINPULSE}	Minimum reset pulse width	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector	10.00	10.00	10.00	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
T _{MMCMDCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and hold of phase-shift enable	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMDCK_PSINCDEC} / T _{MMCMCKD_PSINCDEC}	Setup and hold of phase-shift increment/decrement	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMCKO_PSDONE}	Phase shift clock-to-out of PSDONE	0.59	0.68	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
T _{MMCMDCK_DADDR} / T _{MMCMCKD_DADDR}	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{MMCMDCK_DI} /T _{MMCMCKD_DI}	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{MMCMDCK_DEN} /T _{MMCMCKD_DEN}	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	ns, Min
T _{MMCMDCK_DWE} /T _{MMCMCKD_DWE}	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{MMCMCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 39: PLL Specification

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
PLL_F _{INMAX}	Maximum input clock frequency	1066.00	933.00	800.00	MHz
PLL_F _{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
PLL_F _{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	MHz
PLL_F _{BANDWIDTH}	Low PLL bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs ⁽²⁾	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter	Note 3			
PLL_T _{OUTDUTY}	PLL output clock duty cycle precision ⁽⁴⁾	0.20	0.20	0.20	ns
PLL_T _{LOCKMAX}	PLL maximum lock time	100	100	100	μs
PLL_F _{OUTMAX}	PLL maximum output frequency	1066.00	933.00	800.00	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency ⁽⁵⁾	6.25	6.25	6.25	MHz
PLL_T _{EXTFDVAR}	External clock feedback variation	< 20% of clock input period or 1 ns Max			
PLL_RST _{MINPULSE}	Minimum reset pulse width	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
T _{PLLDCK_DADDR} /T _{PLLCKD_DADDR}	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{PLLDCK_DI} /T _{PLLCKD_DI}	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{PLLDCK_DEN} /T _{PLLCKD_DEN}	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	ns, Min
T _{PLLDCK_DWE} /T _{PLLCKD_DWE}	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	MHz, Max

Notes:

- The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
- The static offset is measured between any PLL outputs with identical phase.
- Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
- Includes global clock buffer.
- Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Table 47: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾⁽²⁾						
T _{PSPLLCC} / T _{PHPLLCC}	No delay clock-capable clock input and IFF ⁽³⁾ with PLL	XC7V585T	3.07/−0.21	3.40/−0.21	3.72/−0.21	ns
		XC7V2000T	N/A	2.99/−0.35	3.27/−0.35	ns
		XC7VX330T	2.94/−0.26	3.26/−0.26	3.57/−0.26	ns
		XC7VX415T	3.09/−0.10	3.42/−0.10	3.75/−0.10	ns
		XC7VX485T	2.95/−0.26	3.26/−0.26	3.58/−0.26	ns
		XC7VX550T	3.08/−0.20	3.40/−0.20	3.74/−0.20	ns
		XC7VX690T	3.08/−0.10	3.40/−0.10	3.74/−0.10	ns
		XC7VX980T	N/A	3.39/−0.21	3.72/−0.21	ns
		XC7VX1140T	N/A	3.00/−0.35	3.27/−0.35	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T _{PSCS} /T _{PHCS}	Setup/hold of I/O clock for HR I/O banks	–0.36/1.36	–0.36/1.50	–0.36/1.70	ns
	Setup/hold of I/O clock for HP I/O banks	–0.34/1.39	–0.34/1.53	–0.34/1.73	ns

Table 49: Sample Window

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T _{SAMP}	Sampling error at receiver pins ⁽¹⁾	0.51	0.56	0.61	ns
T _{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO ⁽²⁾	0.30	0.35	0.40	ns

Notes:

- This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
These measurements do not include package or clock tree skew.
- This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 51 summarizes the DC specifications of the GTX transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

Table 51: GTX Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
V _{CMOUTDC}	DC common mode output voltage.	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–200	–	$V_{MGTAVTT}$	mV
V _{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–	$2/3 V_{MGTAVTT}$	–	mV
R _{IN}	Differential input resistance		–	100	–	Ω
C _{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476), and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

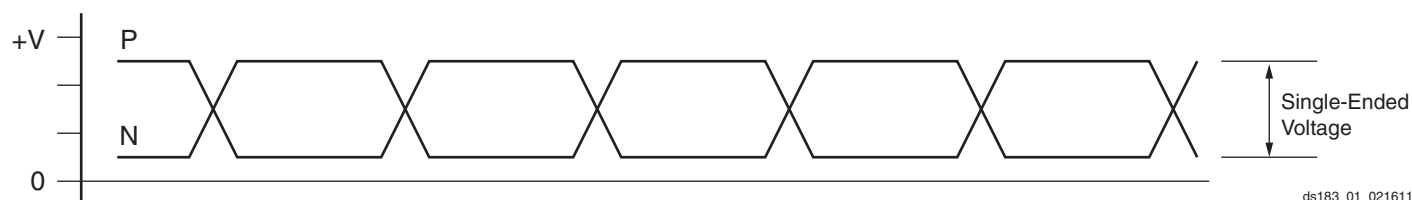


Figure 1: Single-Ended Peak-to-Peak Voltage

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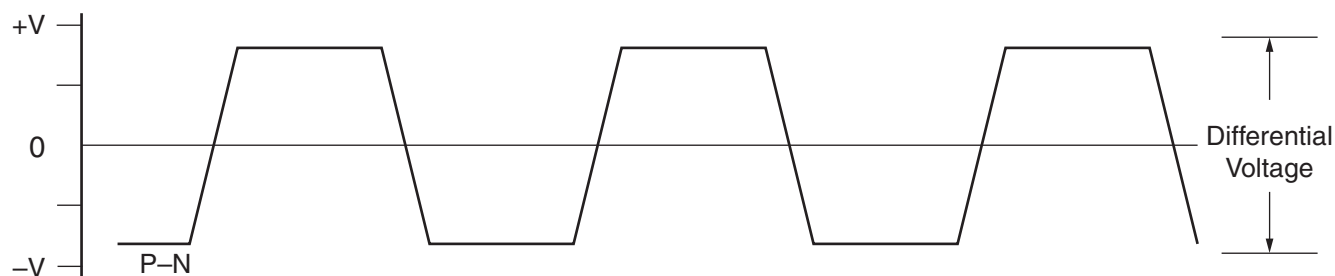


Figure 2: Differential Peak-to-Peak Voltage

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GTH Transceiver Specifications

GTH Transceiver DC Input and Output Levels

Table 66 summarizes the DC specifications of the GTH transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

Table 66: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Absolute input voltage	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
DV _{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to 1010	–	–	800	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled	Equation based	V _{MGTAVTT} – DV _{PPOUT} /4			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based	V _{MGTAVTT} – DV _{PPOUT} /2			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476), and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

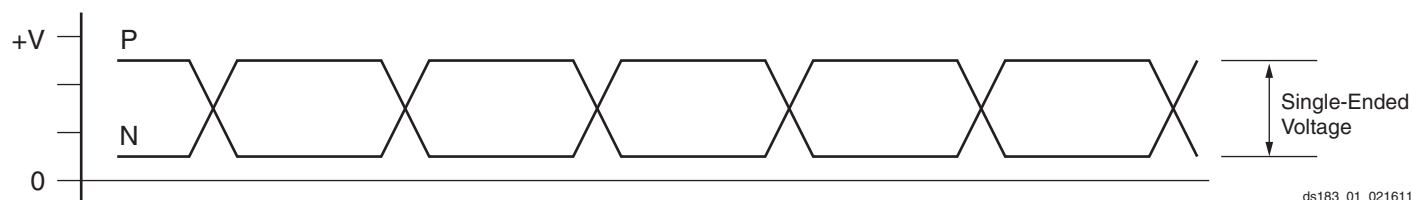


Figure 4: Single-Ended Peak-to-Peak Voltage

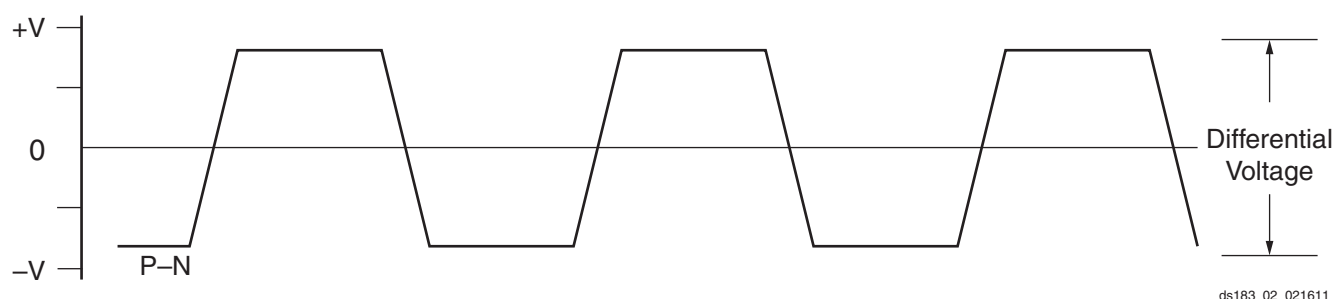


Figure 5: Differential Peak-to-Peak Voltage

Table 72: GTH Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3E/-2GE ⁽²⁾	-2(C&I)/-2LE ⁽²⁾	-1(C&I) ⁽³⁾	
F _{TXOUT}	TXUSERCLKOUT maximum frequency			412.500	412.500	312.500	MHz
F _{RXOUT}	RXUSERCLKOUT maximum frequency			412.500	412.500	312.500	MHz
F _{TXIN}	TXUSERCLKIN maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	409.375	353.125	265.625	MHz
F _{RXIN}	RXUSERCLKIN maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	409.375	353.125	265.625	MHz
F _{TXIN2}	TXUSERCLKIN2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	409.375	353.125	265.625	MHz
		64-bit	64-bit	204.688	176.563	132.813	MHz
F _{RXIN2}	RXUSERCLKIN2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	409.375	353.125	265.625	MHz
		64-bit	64-bit	204.688	176.563	132.813	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
2. For speed grades -3E, -2GE, -2C, -2I, and -2LE, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
3. For speed grade -1 (and when V_{CCINT} = 0.9V), a 16-bit data path can only be used for speeds less than 5.0 Gb/s.

Table 73: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	—	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	—	40	—	ps
T _{FTX}	TX fall time	80%–20%	—	40	—	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		—	—	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		—	—	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		—	—	140	ns
TJ _{13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	—	—	0.3	UI
DJ _{13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{12.5}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	—	—	0.28	UI
DJ _{12.5}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{11.3}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	—	—	0.28	UI
DJ _{11.3}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	—	—	0.28	UI
DJ _{10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	—	—	0.33	UI
DJ _{10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		—	—	0.17	UI
TJ _{9.953}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	—	—	0.28	UI
DJ _{9.953}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{9.8}	Total jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	—	—	0.28	UI
DJ _{9.8}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{8.0_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	—	—	0.28	UI
DJ _{8.0_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI

GTH Transceiver Protocol Jitter Characteristics

For [Table 75](#) through [Table 80](#), the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 75: Gigabit Ethernet Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 76: XAUI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 77: PCI Express Protocol Characteristics (GTH Transceivers)⁽¹⁾

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 ⁽³⁾	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.