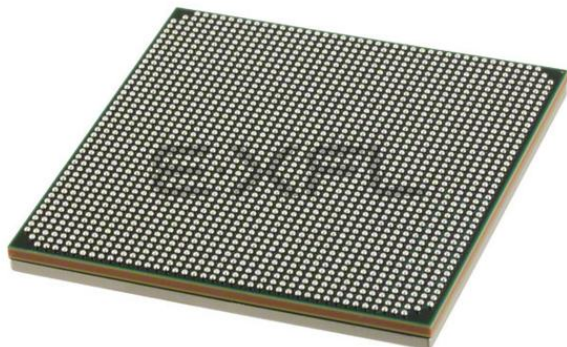




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	89000
Number of Logic Elements/Cells	1139200
Total RAM Bits	69304320
Number of I/O	1100
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1930-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx1140t-2flg1930c

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 3.3V$	68	–	330	μA
	Pad pull-down (when selected) @ $V_{IN} = 1.8V$	45	–	180	μA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT} ⁽³⁾	Battery supply current	–	–	150	nA
R_{IN_TERM} ⁽⁴⁾	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

- Typical values are specified at nominal voltage, 25°C.
- This measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C.
- Termination resistance to a $V_{CCO}/2$ level.

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.55$	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

Notes:

- A total of 200 mA per bank should not be exceeded.

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Table 7 shows the minimum current, in addition to I_{CCQ} , that is required by Virtex-7 T and XT devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the XPower tools to estimate current drain on these supplies.

Table 7: Power-On Current for Virtex-7 T and XT Devices

Device	$I_{CCINTMIN}$ Typ ⁽¹⁾	$I_{CCAUXMIN}$ Typ ⁽¹⁾	I_{CCOMIN} Typ ⁽¹⁾	I_{CCAUX_IO} Typ ⁽¹⁾	I_{CCBRAM} Typ ⁽¹⁾	Units
XC7V585T	$I_{CCINTQ} + 2700$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 60$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 108$	mA
XC7V2000T	$I_{CCINTQ} + 4000$	$I_{CCAUXQ} + 80$	$I_{CCOQ} + 60$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 176$	mA
XC7VX330T	$I_{CCINTQ} + 1000$	$I_{CCAUXQ} + 65$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 95$	mA
XC7VX415T	$I_{CCINTQ} + 1200$	$I_{CCAUXQ} + 75$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 115$	mA
XC7VX485T	$I_{CCINTQ} + 1200$	$I_{CCAUXQ} + 80$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 140$	mA
XC7VX550T	$I_{CCINTQ} + 3300$	$I_{CCAUXQ} + 143$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 57$ mA per bank	$I_{CCBRAMQ} + 200$	mA
XC7VX690T	$I_{CCINTQ} + 3300$	$I_{CCAUXQ} + 143$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 57$ mA per bank	$I_{CCBRAMQ} + 200$	mA
XC7VX980T	$I_{CCINTQ} + 6500$	$I_{CCAUXQ} + 202$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 60$ mA per bank	$I_{CCBRAMQ} + 204$	mA
XC7VX1140T	$I_{CCINTQ} + 8000$	$I_{CCAUXQ} + 235$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 63$ mA per bank	$I_{CCBRAMQ} + 256$	mA

Notes:

- Typical values are specified at nominal voltage, 25°C.
- Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

Table 8: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of V_{CCAUX_IO}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100^{\circ}C^{(1)}$	–	500	ms
		$T_J = 85^{\circ}C^{(1)}$	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$		0.2	50	ms

Notes:

- Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

LVDS DC Specifications (LVDS_25)

The LVDS standard is available in the HR I/O banks.

Table 12: LVDS_25 DC Specifications⁽¹⁾

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks.

Table 13: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		1.710	1.800	1.890	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ± 350 mV	0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

Table 18: Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator⁽¹⁾⁽²⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO}	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
4:1 Memory Controllers						
DDR3	HP	2.0V	1866	1866	1600	Mb/s
	HP	1.8V	1600	1333	1066	Mb/s
	HR	N/A	1066	1066	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	Mb/s
	HP	1.8V	1333	1066	800	Mb/s
	HR	N/A	800	800	667	Mb/s
DDR2	HP	2.0V	800	800	800	Mb/s
	HP	1.8V	800	800	800	Mb/s
	HR	N/A	800	800	800	Mb/s
RLDRAM III	HP	2.0V	800	667	667	MHz
	HP	1.8V	550	500	450	MHz
	HR	N/A	N/A			
2:1 Memory Controllers						
DDR3	HP	2.0V	1066	1066	800	Mb/s
	HP	1.8V	1066	1066	800	Mb/s
	HR	N/A	1066	1066	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	Mb/s
	HP	1.8V	1066	1066	800	Mb/s
	HR	N/A	800	800	667	Mb/s
DDR2	HP	2.0V	800	800	800	Mb/s
	HP	1.8V				
	HR	N/A				
QDR II+ ⁽³⁾	HP	2.0V	550	500	450	MHz
	HP	1.8V				
	HR	N/A	500	450	400	MHz
RLDRAM II	HP	2.0V	533	500	450	MHz
	HP	1.8V				
	HR	N/A				
LPDDR2	HP	2.0V	667	667	667	Mb/s
	HP	1.8V	667	667	667	Mb/s
	HR	N/A	667	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* ([UG586](#)).
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
SSTL15_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL135_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
SSTL12_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.94	1.06	1.15	1.58	1.82	1.97	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.97	1.09	1.16	1.61	1.84	1.99	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL135_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 21 specifies the values of T_{IOTPHZ} and T_{IOIBUFDISABLE}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). T_{IOIBUFDISABLE} is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 21: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T _{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	ns
T _{IOIBUFDISABLE_HR}	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	ns
T _{IOIBUFDISABLE_HP}	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	ns

Input/Output Delay Switching Characteristics

Table 26: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IDELAYCTRL					
T _{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.22	3.22	3.22	μs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	MHz
	Attribute REFCLK frequency = 300.0 ⁽¹⁾	300	300	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum reset pulse width	52.00	52.00	52.00	ns
IDELAY/ODELAY					
T _{IDELAYRESOLUTION}	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F _{REF})			ps
T _{IDELAYPAT_JIT} and T _{ODELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽³⁾	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽⁴⁾	±9	±9	±9	ps per tap
T _{IDELAY_CLK_MAX} / T _{ODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY/ODELAY	800	800	710	MHz
T _{IDCCK_CE} / T _{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	ns
T _{ODCCK_CE} / T _{ODCKC_CE}	CE pin setup/hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	ns
T _{IDCCK_INC} / T _{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	ns
T _{ODCCK_INC} / T _{ODCKC_INC}	INC pin setup/hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	ns
T _{IDCCK_RST} / T _{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	ns
T _{ODCCK_RST} / T _{ODCKC_RST}	RST pin setup/hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	ns
T _{IDDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	ps
T _{ODDO_ODATAIN}	Propagation delay through ODELAY	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

Table 27: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IO_FIFO Clock to Out Delays					
T _{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags	0.59	0.62	0.81	ns
Setup/Hold					
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.43/−0.01	0.47/−0.01	0.53/−0.01	ns
T _{IFFCKC_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.39/−0.01	0.43/−0.01	0.50/−0.01	ns
T _{OFFCKC_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	ns
Minimum Pulse Width					
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
Maximum Frequency					
F _{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T _{SHCKO} ⁽¹⁾	Clock to A – B outputs	0.68	0.70	0.85	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	ns, Min
T _{CECK_LRAM} /T _{CKCE_LRAM}	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	ns, Min
Clock CLK					
T _{MPW}	Minimum pulse width	0.68	0.77	0.91	ns, Min
T _{MCP}	Minimum clock period	1.35	1.54	1.82	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T _{REG}	Clock to A – D outputs	0.96	0.98	1.20	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{WS_SHFREG} /T _{WH_SHFREG}	WE input	0.26/0.09	0.27/0.09	0.33/0.09	ns, Min
T _{CECK_SHFREG} /T _{CKCE_SHFREG}	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	ns, Min
T _{DS_SHFREG} /T _{DH_SHFREG}	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	ns, Min
Clock CLK					
T _{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	ns, Min

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$T_{\text{DSPDO_A_P}}$	A input to P output not using multiplier	1.30	1.48	1.76	ns
$T_{\text{DSPDO_C_P}}$	C input to P output	1.13	1.30	1.55	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
$T_{\text{DSPDO_}\{A; B\}_ \{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	ns
$T_{\text{DSPDO_}\{A, B\}_ \text{CARRYCASCOUT_MULT}}$	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	ns
$T_{\text{DSPDO_D_CARRYCASCOUT_MULT}}$	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	ns
$T_{\text{DSPDO_}\{A, B\}_ \text{CARRYCASCOUT}}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	ns
$T_{\text{DSPDO_C_CARRYCASCOUT}}$	C input to CARRYCASCOUT output	1.34	1.53	1.83	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
$T_{\text{DSPDO_ACIN_P_MULT}}$	ACIN input to P output using multiplier	3.09	3.55	4.24	ns
$T_{\text{DSPDO_ACIN_P}}$	ACIN input to P output not using multiplier	1.16	1.33	1.59	ns
$T_{\text{DSPDO_ACIN_ACOUT}}$	ACIN input to ACOUT output	0.32	0.37	0.45	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT_MULT}}$	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT}}$	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	ns
$T_{\text{DSPDO_PCIN_P}}$	PCIN input to P output	0.94	1.08	1.29	ns
$T_{\text{DSPDO_PCIN_CARRYCASCOUT}}$	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	ns
Clock to Outs from Output Register Clock to Output Pins					
$T_{\text{DSPCKO_P_PREG}}$	CLK PREG to P output	0.33	0.35	0.39	ns
$T_{\text{DSPCKO_CARRYCASCOUT_PREG}}$	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
$T_{\text{DSPCKO_P_MREG}}$	CLK MREG to P output	1.42	1.64	1.96	ns
$T_{\text{DSPCKO_CARRYCASCOUT_MREG}}$	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	ns
$T_{\text{DSPCKO_P_ADREG_MULT}}$	CLK ADREG to P output using multiplier	2.30	2.63	3.13	ns
$T_{\text{DSPCKO_CARRYCASCOUT_ADREG_MULT}}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	ns
Clock to Outs from Input Register Clock to Output Pins					
$T_{\text{DSPCKO_P_AREG_MULT}}$	CLK AREG to P output using multiplier	3.34	3.83	4.55	ns
$T_{\text{DSPCKO_P_BREG}}$	CLK BREG to P output not using multiplier	1.39	1.59	1.88	ns
$T_{\text{DSPCKO_P_CREG}}$	CLK CREG to P output not using multiplier	1.43	1.64	1.95	ns
$T_{\text{DSPCKO_P_DREG_MULT}}$	CLK DREG to P output using multiplier	3.32	3.80	4.51	ns

Clock Buffers and Networks

Table 33: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$T_{BCCCK_CE}/T_{BCCCK_CE}^{(1)}$	CE pins setup/hold	0.12/0.30	0.14/0.38	0.26/0.38	ns
$T_{BCCCK_S}/T_{BCCCK_S}^{(1)}$	S pins setup/hold	0.12/0.30	0.14/0.38	0.26/0.38	ns
$T_{BCKO_O}^{(2)}$	BUFGCTRL delay from I/O to O	0.08	0.10	0.12	ns
Maximum Frequency					
F_{MAX_BUFG}	Global clock tree (BUFG)	741.00	710.00	625.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCCK_S} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BCKO_O} (BUFG delay from I/O to O) values are the same as T_{BCKO_O} values.

Table 34: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BIOCKO_O}	Clock to out delay from I to O	1.04	1.14	1.32	ns
Maximum Frequency					
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800.00	800.00	710.00	MHz

Table 35: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BRCKO_O}	Clock to out delay from I to O	0.60	0.65	0.77	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.30	0.32	0.38	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.71	0.75	0.96	ns
Maximum Frequency					
$F_{MAX_BUFR}^{(1)}$	Regional clock tree (BUFR)	600.00	540.00	450.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 36: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	ns
$T_{BHCKCK_CE}/T_{BHCKCK_CE}$	CE pin setup and hold	0.20/0.16	0.23/0.20	0.38/0.21	ns
Maximum Frequency					
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	741.00	710.00	625.00	MHz

Table 37: Duty Cycle Distortion and Clock Tree Skew

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
T _{DCD_CLK}	Global clock tree duty cycle distortion ⁽¹⁾	All	0.20	0.20	0.20	ns
T _{CKSKEW}	Global clock tree skew ⁽²⁾	XC7V585T	0.75	0.91	0.98	ns
		XC7V2000T	N/A	0.39	0.39	ns
		XC7VX330T	0.60	0.74	0.79	ns
		XC7VX415T	0.76	0.84	0.91	ns
		XC7VX485T	0.60	0.74	0.79	ns
		XC7VX550T	0.73	0.88	0.96	ns
		XC7VX690T	0.73	0.88	0.96	ns
		XC7VX980T	N/A	0.91	0.98	ns
		XC7VX1140T	N/A	0.39	0.39	ns
T _{DCD_BUFIN}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	ns
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	ns
T _{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip-flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements in a single SLR. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 38: MMCM Specification

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
MMCM_F _{INMAX}	Maximum input clock frequency	1066.00	933.00	800.00	MHz
MMCM_F _{INMIN}	Minimum input clock frequency	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
MMCM_F _{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	550.00	500.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs ⁽²⁾	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter	Note 3			
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision ⁽⁴⁾	0.20	0.20	0.20	ns

Table 47: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾⁽²⁾						
T _{PSPLLCC} / T _{PHPLLCC}	No delay clock-capable clock input and IFF ⁽³⁾ with PLL	XC7V585T	3.07/−0.21	3.40/−0.21	3.72/−0.21	ns
		XC7V2000T	N/A	2.99/−0.35	3.27/−0.35	ns
		XC7VX330T	2.94/−0.26	3.26/−0.26	3.57/−0.26	ns
		XC7VX415T	3.09/−0.10	3.42/−0.10	3.75/−0.10	ns
		XC7VX485T	2.95/−0.26	3.26/−0.26	3.58/−0.26	ns
		XC7VX550T	3.08/−0.20	3.40/−0.20	3.74/−0.20	ns
		XC7VX690T	3.08/−0.10	3.40/−0.10	3.74/−0.10	ns
		XC7VX980T	N/A	3.39/−0.21	3.72/−0.21	ns
		XC7VX1140T	N/A	3.00/−0.35	3.27/−0.35	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. IFF = Input Flip-Flop or Latch
4. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T _{PSCS} /T _{PHCS}	Setup/hold of I/O clock for HR I/O banks	–0.36/1.36	–0.36/1.50	–0.36/1.70	ns
	Setup/hold of I/O clock for HP I/O banks	–0.34/1.39	–0.34/1.53	–0.34/1.73	ns

Table 49: Sample Window

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T _{SAMP}	Sampling error at receiver pins ⁽¹⁾	0.51	0.56	0.61	ns
T _{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO ⁽²⁾	0.30	0.35	0.40	ns

Notes:

1. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-7 T and XT FPGA clock transmitter and receiver data-valid windows.

Table 50: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC7V585T	FFG1157	232	ps
			FFG1761	255	ps
		XC7V2000T	FHG1761	308	ps
			FLG1925	266	ps
		XC7VX330T	FFG1157	170	ps
			FFG1761	270	ps
		XC7VX415T	FFG1157	203	ps
			FFG1158	237	ps
			FFG1927	183	ps
		XC7VX485T	FFG1157	191	ps
			FFG1158	209	ps
			FFG1761	274	ps
			FFG1927	209	ps
			FFG1930	304	ps
		XC7VX550T	FFG1158	217	ps
			FFG1927	254	ps
		XC7VX690T	FFG1157	239	ps
			FFG1158	217	ps
			FFG1761	284	ps
			FFG1926	238	ps
			FFG1927	254	ps
			FFG1930	287	ps
		XC7VX980T	FFG1926	242	ps
			FFG1928	199	ps
			FFG1930	243	ps
		XC7VX1140T	FLG1926	271	ps
			FLG1928	216	ps
			FLG1930	279	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
- Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the 7 Series FPGAs GTX/GTH Transceiver User Guide ([UG476](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: Gigabit Ethernet Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: XAUI Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: PCI Express Protocol Characteristics (GTX Transceivers)⁽¹⁾

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 ⁽³⁾	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 74: GTH Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTHRX}	Serial data rate	RX oversampler not enabled	0.500	–	F _{GTHMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm
RX _{RL}	Run length (CID)		–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s	0.3	–	–	UI
JT_SJ _{12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.3	–	–	UI
JT_SJ _{11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s	0.3	–	–	UI
JT_SJ _{10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.8}	Sinusoidal jitter (QPLL) ⁽³⁾	9.8 Gb/s	0.3	–	–	UI
JT_SJ _{8.0_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	8.0 Gb/s	0.44	–	–	UI
JT_SJ _{8.0_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	8.0 Gb/s	0.42	–	–	UI
JT_SJ _{6.6_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	6.6 Gb/s	0.48	–	–	UI
JT_SJ _{6.6_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal jitter (CPLL) ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{3.2L}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁵⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁷⁾	0.5	–	–	UI
JT_SJ ₅₀₀	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
JT_TJSE _{6.6}		6.6 Gb/s	0.70	–	–	UI
JT_SJSE _{3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.1	–	–	UI
JT_SJSE _{6.6}		6.6 Gb/s	0.1	–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

Table 80: CPRI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 79.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 81: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	500.00	500.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz

XADC Specifications

Table 82: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, T _j = −40°C to 100°C, Typical values at T _j =+40°C						
ADC Accuracy ⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±6	LSBs
Gain Error		Gain calibration disabled	–	–	±0.5	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio ⁽²⁾	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion ⁽²⁾	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	–	70	–	dB
ADC Accuracy at Extended Temperatures (−55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs ⁽³⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T _j = −40°C to 100°C.	–	–	±4	°C
		T _j = −55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −40°C to +100°C	–	–	±1	%
		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −55°C to +125°C	–	–	±2	%
Conversion Rate ⁽⁴⁾						
Conversion Time - Continuous	t _{CONV}	Number of ADCCLK cycles	26	–	32	cycle
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	cycle
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%

Table 83: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Master/Slave Serial Mode Programming Switching						
T _{DCC} /T _{CCKD}	DIN setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{CCO}	DOUT clock to out		8.0	8.0	8.0	ns, Max
SelectMAP Mode Programming Switching						
T _{SMDCC} /T _{SMCCKD}	D[31:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{SMWCCK} /T _{SMCCKW}	RDWR_B setup/hold		10.0/0.0	10.0/0.0	10.0/0.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)		7.0	7.0	7.0	ns, Max
T _{SMCO}	D[31:00] clock to out in readback		8.0	8.0	8.0	ns, Max
F _{RBCK}	Readback frequency	SLR-based	70	70	70	MHz, Max
		All other devices	100	100	100	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup/hold	SLR-based	9.0/2.0	9.0/2.0	9.0/2.0	ns, Min
		All other devices	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	SLR-based	17	17	17	ns, Max
		All other devices	7.0	7.0	7.0	ns, Max
F _{TCK}	TCK frequency	SLR-based	20	20	20	MHz, Max
		All other devices	66	66	66	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out		8.5	8.5	8.5	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPICCD}	D[03:00] setup/hold		3.0/0.0	3.0/0.0	3.0/0.0	ns, Min
T _{SPICCM}	MOSI clock to out		8.0	8.0	8.0	ns, Max
T _{SPICCF}	FCS_B clock to out		8.0	8.0	8.0	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* ([UG470](#)).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 84 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* ([UG470](#)).

Table 84: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document.

Date	Version	Description
03/01/2011	1.0	Initial Xilinx release.
10/05/2011	1.1	Removed the XC7V285T, XC7V450T, and XC7V855T devices from the entire data sheet. Added the XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T, and XC7VX1140T devices to the entire data sheet. Replaced -1L with -2L throughout this data sheet. Added the extended temperature range discussion to page 1. Updated Min/Max values and removed Note 5 from Table 2. Clarified Power-On/Off Power Supply Sequencing power sequencing discussion including adding $T_{VCCO2VCCAUX}$ to Table 8. Added I_{CCAUX_IO} and I_{CCBRAM} to Table 6 and Table 7. Updated V_{ICM} in Table 12 and Table 13. Added Note 1 to Table 12. Updated Table 84 including adding Note 1. Added Table 13. Revised the reference clock maximum frequency (F_{GCLK}) in Table 55. Added Table 57. Added GTH Transceiver Specifications section. Removed erroneous instances of HSTL_III from Table 20. Removed the <i>I/O Standard Adjustment Measurement Methodology</i> section. Use IBIS for more accurate information and measurements. Updated $T_{IDELAYPAT_JIT}$ in Table 26. Added T_{AS}/T_{AH} to Table 28. Added $T_{RDCK_DI_WF_NC}/T_{RDCK_DI_WF_NC}$ and $T_{RDCK_DI_RF}/T_{RDCK_DI_RF}$ to Table 31. Completely updated the specifications in Table 83. Updated $MMCM_F_{INDUTY}$ and added $F_{INJITTER}$, $T_{OUTJITTER}$, and $T_{EXTFVAR}$ and Note 3 to Table 38. Updated the AC Switching Characteristics section. Updated the Table 50 package list. Updated the Notice of Disclaimer.
11/07/2011	1.2	Added -2G speed grade, where appropriate, throughout document. Revised the V_{OCM} specification in Table 12. Updated the AC Switching Characteristics based upon the ISE 13.3 v1.02 speed specification throughout document including Table 19 and Table 20. Added MMCM to the symbol names of a few specifications in Table 38 and PLL to the symbol names in Table 39. In Table 40 through Table 47, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 49.
02/13/2012	1.3	Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Added typical numbers to Table 3. Updated the notes in Table 6. Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to Table 8. Rearranged Table 9, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 10 and Table 11. Revised the specifications in Table 12 and Table 13. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the IO_FIFO Switching Characteristics table. Revised I_{CCADC} and updated Note 1 in Table 82. Revised DDR LVDS transmitter data width in Table 17. Updated the AC Switching Characteristics based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from Table 28 as they are no longer applicable. Updated specifications in Table 83. Updated Note 1 in Table 37. In the GTX Transceiver Specifications section: Revised V_{IN}, and added I_{DCIN} and I_{DCOUT} to Table 51. Updated and added notes to Table 53. In Table 55, revised F_{GCLK}, removed T_{PHASE}, and added T_{DLOCK}. Revised specifications and added Note 2 to Table 57. Added Table 58 and Table 59 along with GTX Transceiver Protocol Jitter Characteristics in Table 60 through Table 65.
05/23/2012	1.4	Reorganized entire data sheet including adding Table 44 and Table 48. Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Added values to Table 6 and Table 7. Updated Power-On/Off Power Supply Sequencing section with regards to GTX/GTH transceivers. Updated many parameters in Table 9, including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 11. Updated V_{OL} in Table 12. Updated Table 17 and removed notes 2 and 3. Updated Table 18. Updated the AC Switching Characteristics section based upon the ISE 14.1 v1.04 for the -3, -2, -2L (1.0V), -1, and v1.05 for the -2L (0.9V) speed specifications throughout the document. In Table 31, updated Reset Delays section including Note 10 and Note 11. Added data for T_{LOCK} and T_{DLOCK} in Table 55. Updated many of the XADC specifications in Table 82 and added Note 2. Updated and moved <i>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</i> section from Table 83 to Table 38 and Table 39.