



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	25500
Number of Logic Elements/Cells	326400
Total RAM Bits	27648000
Number of I/O	700
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1761-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx330t-1ffg1761i

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.5 and Vivado® Design Suite 2013.1 as outlined in [Table 14](#).

Table 14: Virtex-7 T and XT FPGA Speed Specification Version By Device/Speed Grade

Version In:		Typical V _{CCINT}	Device
ISE 14.5	Vivado 2013.1	(Table 2)	
1.09	1.09	1.0V	XC7V585T, XC7VX485T
N/A	1.08	1.0V	XC7V2000T
1.08	1.08	1.0V	XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T
N/A	1.08	1.0V	XC7VX1140T

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-7 T and XT FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 15](#) correlates the current status of each Virtex-7 T and XT device on a per speed grade basis.

Table 15: Virtex-7 T and XT Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7V585T			-3, -2, -2L, -1
XC7V2000T	-2L, -2G		-2, -1
XC7VX330T			-3, -2, -2L, -1
XC7VX415T			-3, -2, -2L, -1
XC7VX485T			-3, -2, -2L, -1
XC7VX550T			-3, -2, -2L, -1
XC7VX690T			-3, -2, -2L, -1
XC7VX980T	-2, -2L, -1		
XC7VX1140T	-2, -2L, -2G, -1		

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 16](#) lists the production released Virtex-7 T and XT device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 16: Virtex-7 T and XT Device Production Software and Speed Specification Release

Device	Speed Grade Designations				
	-3	-2G	-2	-2L	-1
XC7V585T	Vivado 2012.4 v1.08 or ISE 14.2 v1.06	N/A	Vivado 2012.4 v1.08 or ISE 14.2 v1.06		
XC7V2000T	N/A		Vivado 2012.4 v1.07		Vivado 2012.4 v1.07
XC7VX330T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX415T		N/A			
XC7VX485T	Vivado 2012.4 v1.08 or ISE 14.2 v1.06	N/A	Vivado 2012.4 v1.08 or ISE 14.2 v1.06		
XC7VX550T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX690T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX980T	N/A	N/A			
XC7VX1140T	N/A				

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
HSTL_II_F	0.61	0.64	0.73	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_I_18_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_II_18_F	0.64	0.67	0.76	1.03	1.14	1.23	1.79	2.00	2.22	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	1.09	1.18	1.22	1.85	2.04	2.21	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	1.02	1.11	1.14	1.78	1.97	2.13	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	1.08	1.17	1.21	1.84	2.03	2.20	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	1.01	1.10	1.13	1.77	1.96	2.12	ns
LVC MOS33_S4	1.31	1.40	1.60	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVC MOS33_S8	1.31	1.40	1.60	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVC MOS33_S12	1.31	1.40	1.60	3.05	3.18	3.28	3.81	4.04	4.27	ns
LVC MOS33_S16	1.31	1.40	1.60	3.06	3.43	3.88	3.82	4.29	4.87	ns
LVC MOS33_F4	1.31	1.40	1.60	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVC MOS33_F8	1.31	1.40	1.60	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVC MOS33_F12	1.31	1.40	1.60	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVC MOS33_F16	1.31	1.40	1.60	2.44	2.69	2.96	3.20	3.55	3.95	ns
LVC MOS25_S4	1.08	1.16	1.32	3.08	3.22	3.31	3.84	4.08	4.30	ns
LVC MOS25_S8	1.08	1.16	1.32	2.85	2.98	3.07	3.61	3.84	4.06	ns
LVC MOS25_S12	1.08	1.16	1.32	2.44	2.57	2.67	3.20	3.43	3.66	ns
LVC MOS25_S16	1.08	1.16	1.32	2.79	2.92	3.01	3.55	3.78	4.00	ns
LVC MOS25_F4	1.08	1.16	1.32	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVC MOS25_F8	1.08	1.16	1.32	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS25_F12	1.08	1.16	1.32	2.15	2.29	2.52	2.91	3.15	3.51	ns
LVC MOS25_F16	1.08	1.16	1.32	1.92	2.17	2.45	2.68	3.03	3.44	ns
LVC MOS18_S4	0.64	0.66	0.74	1.55	1.68	1.78	2.31	2.54	2.77	ns
LVC MOS18_S8	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS18_S12	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS18_S16	0.64	0.66	0.74	1.49	1.62	1.72	2.25	2.48	2.71	ns
LVC MOS18_S24 ⁽¹⁾	0.64	0.66	0.74	1.74	1.92	2.08	2.50	2.78	3.07	ns
LVC MOS18_F4	0.64	0.66	0.74	1.38	1.51	1.61	2.14	2.37	2.60	ns
LVC MOS18_F8	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVC MOS18_F12	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVC MOS18_F16	0.64	0.66	0.74	1.52	1.68	1.81	2.28	2.54	2.80	ns
LVC MOS18_F24 ⁽¹⁾	0.64	0.66	0.74	1.34	1.46	1.55	2.10	2.32	2.54	ns
LVC MOS15_S4	0.66	0.69	0.81	1.86	2.00	2.09	2.62	2.86	3.08	ns
LVC MOS15_S8	0.66	0.69	0.81	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVC MOS15_S12	0.66	0.69	0.81	1.83	2.03	2.23	2.59	2.89	3.22	ns
LVC MOS15_S16	0.66	0.69	0.81	1.76	1.95	2.13	2.52	2.81	3.12	ns

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVC MOS15_F4	0.66	0.69	0.81	1.63	1.76	1.86	2.39	2.62	2.85	ns
LVC MOS15_F8	0.66	0.69	0.81	1.79	1.99	2.18	2.55	2.85	3.17	ns
LVC MOS15_F12	0.66	0.69	0.81	1.40	1.54	1.65	2.16	2.40	2.64	ns
LVC MOS15_F16	0.66	0.69	0.81	1.37	1.51	1.61	2.13	2.37	2.60	ns
LVC MOS12_S4	0.88	0.91	1.00	2.53	2.67	2.76	3.29	3.53	3.75	ns
LVC MOS12_S8	0.88	0.91	1.00	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVC MOS12_S12 ⁽¹⁾	0.88	0.91	1.00	1.75	1.89	1.98	2.51	2.75	2.97	ns
LVC MOS12_F4	0.88	0.91	1.00	1.94	2.07	2.17	2.70	2.93	3.16	ns
LVC MOS12_F8	0.88	0.91	1.00	1.50	1.64	1.73	2.26	2.50	2.72	ns
LVC MOS12_F12 ⁽¹⁾	0.88	0.91	1.00	1.54	1.71	1.87	2.30	2.57	2.86	ns
SSTL135_S	0.61	0.64	0.73	1.27	1.40	1.50	2.03	2.26	2.49	ns
SSTL15_S	0.61	0.64	0.73	1.24	1.37	1.47	2.00	2.23	2.46	ns
SSTL18_I_S	0.64	0.67	0.76	1.59	1.74	1.85	2.35	2.60	2.84	ns
SSTL18_II_S	0.64	0.67	0.76	1.27	1.40	1.50	2.03	2.26	2.49	ns
DIFF_SSTL135_S	0.59	0.61	0.73	1.27	1.40	1.50	2.03	2.26	2.49	ns
DIFF_SSTL15_S	0.63	0.67	0.77	1.24	1.37	1.47	2.00	2.23	2.46	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	1.50	1.63	1.72	2.26	2.49	2.71	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	1.13	1.22	1.25	1.89	2.08	2.24	ns
SSTL135_F	0.61	0.64	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
SSTL15_F	0.61	0.64	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
SSTL18_I_F	0.64	0.67	0.76	1.12	1.22	1.26	1.88	2.08	2.25	ns
SSTL18_II_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
DIFF_SSTL135_F	0.59	0.61	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
DIFF_SSTL15_F	0.63	0.67	0.77	1.04	1.17	1.26	1.80	2.03	2.25	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	1.10	1.19	1.23	1.86	2.05	2.22	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	1.02	1.10	1.14	1.78	1.96	2.13	ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
DIFF_HSTL_I_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.68	1.91	2.06	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.98	1.09	1.16	1.62	1.85	1.98	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.67	1.91	2.06	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.98	1.09	1.16	1.61	1.85	1.98	ns
DIFF_HSTL_II_T_DCI_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.67	1.91	2.06	ns
LVC MOS18_S2	0.47	0.50	0.60	3.95	4.28	4.85	4.59	5.04	5.67	ns
LVC MOS18_S4	0.47	0.50	0.60	2.67	2.98	3.43	3.31	3.73	4.26	ns
LVC MOS18_S6	0.47	0.50	0.60	2.14	2.38	2.72	2.77	3.14	3.54	ns
LVC MOS18_S8	0.47	0.50	0.60	1.98	2.21	2.52	2.61	2.97	3.35	ns
LVC MOS18_S12	0.47	0.50	0.60	1.70	1.91	2.17	2.34	2.67	2.99	ns
LVC MOS18_S16	0.47	0.50	0.60	1.57	1.75	1.97	2.20	2.51	2.79	ns
LVC MOS18_F2	0.47	0.50	0.60	3.50	3.87	4.48	4.14	4.63	5.30	ns
LVC MOS18_F4	0.47	0.50	0.60	2.23	2.50	2.87	2.87	3.25	3.69	ns
LVC MOS18_F6	0.47	0.50	0.60	1.80	2.00	2.26	2.43	2.76	3.08	ns
LVC MOS18_F8	0.47	0.50	0.60	1.46	1.72	2.04	2.10	2.47	2.86	ns
LVC MOS18_F12	0.47	0.50	0.60	1.26	1.40	1.53	1.89	2.16	2.35	ns
LVC MOS18_F16	0.47	0.50	0.60	1.19	1.33	1.44	1.83	2.08	2.26	ns
LVC MOS15_S2	0.59	0.62	0.73	3.55	3.89	4.45	4.19	4.65	5.27	ns
LVC MOS15_S4	0.59	0.62	0.73	2.45	2.70	3.06	3.08	3.45	3.89	ns
LVC MOS15_S6	0.59	0.62	0.73	2.24	2.51	2.88	2.88	3.26	3.71	ns
LVC MOS15_S8	0.59	0.62	0.73	1.91	2.16	2.49	2.55	2.91	3.31	ns
LVC MOS15_S12	0.59	0.62	0.73	1.77	1.98	2.23	2.41	2.73	3.05	ns
LVC MOS15_S16	0.59	0.62	0.73	1.62	1.81	2.02	2.26	2.56	2.84	ns
LVC MOS15_F2	0.59	0.62	0.73	3.38	3.69	4.18	4.02	4.44	5.00	ns
LVC MOS15_F4	0.59	0.62	0.73	2.04	2.21	2.44	2.68	2.97	3.26	ns
LVC MOS15_F6	0.59	0.62	0.73	1.47	1.74	2.09	2.10	2.50	2.91	ns
LVC MOS15_F8	0.59	0.62	0.73	1.31	1.46	1.61	1.95	2.22	2.43	ns
LVC MOS15_F12	0.59	0.62	0.73	1.21	1.34	1.45	1.84	2.10	2.27	ns
LVC MOS15_F16	0.59	0.62	0.73	1.18	1.31	1.41	1.82	2.07	2.23	ns
LVC MOS12_S2	0.64	0.67	0.78	3.38	3.80	4.48	4.02	4.55	5.30	ns
LVC MOS12_S4	0.64	0.67	0.78	2.62	2.94	3.43	3.26	3.70	4.25	ns
LVC MOS12_S6	0.64	0.67	0.78	2.05	2.33	2.72	2.69	3.08	3.54	ns
LVC MOS12_S8	0.64	0.67	0.78	1.94	2.18	2.51	2.58	2.94	3.33	ns
LVC MOS12_F2	0.64	0.67	0.78	2.84	3.15	3.62	3.48	3.90	4.44	ns
LVC MOS12_F4	0.64	0.67	0.78	1.97	2.18	2.44	2.61	2.93	3.26	ns
LVC MOS12_F6	0.64	0.67	0.78	1.33	1.51	1.70	1.96	2.26	2.52	ns
LVC MOS12_F8	0.64	0.67	0.78	1.27	1.42	1.55	1.91	2.18	2.37	ns
LVDCI_18	0.47	0.50	0.60	1.99	2.15	2.35	2.62	2.91	3.17	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVDCI_15	0.59	0.62	0.73	1.98	2.23	2.58	2.62	2.99	3.40	ns
LVDCI_DV2_18	0.47	0.50	0.60	1.99	2.15	2.34	2.62	2.90	3.17	ns
LVDCI_DV2_15	0.59	0.62	0.73	1.98	2.23	2.58	2.62	2.99	3.40	ns
HSLVDCI_18	0.68	0.72	0.82	1.99	2.15	2.35	2.62	2.91	3.17	ns
HSLVDCI_15	0.68	0.72	0.82	1.98	2.23	2.58	2.62	2.99	3.40	ns
SSTL18_I_S	0.68	0.72	0.82	1.02	1.15	1.24	1.66	1.90	2.07	ns
SSTL18_II_S	0.68	0.72	0.82	1.17	1.29	1.37	1.81	2.05	2.19	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.92	1.06	1.17	1.56	1.82	1.99	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.88	0.98	1.08	1.51	1.74	1.90	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.92	1.06	1.17	1.56	1.82	1.99	ns
SSTL15_S	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
SSTL135_S	0.69	0.72	0.82	0.97	1.10	1.19	1.60	1.85	2.01	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
SSTL12_S	0.69	0.72	0.82	0.96	1.09	1.18	1.60	1.84	2.00	ns
SSTL12_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	1.02	1.15	1.24	1.66	1.90	2.07	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	1.17	1.29	1.37	1.81	2.05	2.19	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.92	1.06	1.17	1.56	1.82	1.99	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.88	0.98	1.08	1.51	1.74	1.90	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.92	1.06	1.17	1.56	1.82	1.99	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
DIFF_SSTL135_S	0.69	0.72	0.82	0.97	1.10	1.19	1.60	1.85	2.01	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.96	1.09	1.18	1.60	1.84	2.00	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
SSTL18_I_F	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
SSTL18_II_F	0.68	0.72	0.82	0.97	1.09	1.16	1.61	1.84	1.99	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns

Input Serializer/Deserializer Switching Characteristics

Table 24: ISERDES Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold for Control Lines					
$T_{ISCK_BITSLIP}/T_{ISCK_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	ns
$T_{ISCK_CE} / T_{ISCK_CE}^{(2)}$	CE pin setup/hold with respect to CLK (for CE1)	0.39/−0.02	0.44/−0.02	0.63/−0.02	ns
$T_{ISCK_CE2} / T_{ISCK_CE2}^{(2)}$	CE pin setup/hold with respect to CLKDIV (for CE2)	−0.12/0.29	−0.12/0.31	−0.12/0.35	ns
Setup/Hold for Data Lines					
T_{ISDCK_D}/T_{ISCKD_D}	D pin setup/hold with respect to CLK	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_DDLY}/T_{ISCKD_DDLY}$	DDLY pin setup/hold with respect to CLK (using IDELAY) ⁽¹⁾	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_D_DDR} / T_{ISCKD_D_DDR}$	D pin setup/hold with respect to CLK at DDR mode	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_DDLY_DDR}/T_{ISCKD_DDLY_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾	0.11/0.11	0.12/0.12	0.15/0.15	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCK_CE2} and T_{ISCK_CE2} are reported as T_{ISCK_CE}/T_{ISCK_CE} in the timing report.

Input/Output Delay Switching Characteristics

Table 26: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IDELAYCTRL					
T _{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.22	3.22	3.22	μs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	MHz
	Attribute REFCLK frequency = 300.0 ⁽¹⁾	300	300	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum reset pulse width	52.00	52.00	52.00	ns
IDELAY/ODELAY					
T _{IDELAYRESOLUTION}	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F _{REF})			ps
T _{IDELAYPAT_JIT} and T _{ODELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽³⁾	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽⁴⁾	±9	±9	±9	ps per tap
T _{IDELAY_CLK_MAX} / T _{ODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY/ODELAY	800	800	710	MHz
T _{IDCCK_CE} / T _{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	ns
T _{ODCCK_CE} / T _{ODCKC_CE}	CE pin setup/hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	ns
T _{IDCCK_INC} / T _{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	ns
T _{ODCCK_INC} / T _{ODCKC_INC}	INC pin setup/hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	ns
T _{IDCCK_RST} / T _{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	ns
T _{ODCCK_RST} / T _{ODCKC_RST}	RST pin setup/hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	ns
T _{IDDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	ps
T _{ODDO_ODATAIN}	Propagation delay through ODELAY	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

Block RAM and FIFO Switching Characteristics

Table 31: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Block RAM and FIFO Clock-to-Out Delays					
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.57	1.80	2.08	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.54	0.63	0.75	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.35	2.58	3.26	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.62	0.69	0.80	ns, Max
T _{RCKO_DO_CASCOUT} and T _{RCKO_DO_CASCOUT_REG}	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.21	2.45	2.80	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	0.98	1.08	1.24	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.65	0.74	0.89	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.79	0.87	0.98	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (without output register)	2.17	2.38	3.01	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	ns, Max
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{RCKC_ADDRA} /T _{RCKC_ADDRA}	ADDR inputs ⁽⁸⁾	0.38/0.27	0.42/0.28	0.48/0.31	ns, Min
T _{RDCK_DI_WF_NC} / T _{RCKD_DI_WF_NC}	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾	0.49/0.51	0.55/0.53	0.63/0.57	ns, Min
T _{RDCK_DI_RF} /T _{RCKD_DI_RF}	Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾	0.17/0.25	0.19/0.29	0.21/0.35	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.42/0.37	0.47/0.39	0.53/0.43	ns, Min
T _{RDCK_DI_ECCW} /T _{RCKD_DI_ECCW}	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.79/0.37	0.87/0.39	0.99/0.43	ns, Min
T _{RDCK_DI_ECC_FIFO} / T _{RCKD_DI_ECC_FIFO}	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.89/0.47	0.98/0.50	1.12/0.54	ns, Min
T _{RCKC_INJECTBITERR} / T _{RCKC_INJECTBITERR}	Inject single/double bit error in ECC mode	0.49/0.30	0.55/0.31	0.63/0.34	ns, Min
T _{RCKC_EN} /T _{RCKC_EN}	Block RAM Enable (EN) input	0.30/0.17	0.33/0.18	0.38/0.20	ns, Min
T _{RCKC_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.21/0.13	0.25/0.13	0.31/0.14	ns, Min
T _{RCKC_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input	0.25/0.06	0.27/0.06	0.29/0.06	ns, Min
T _{RCKC_RSTRAM} /T _{RCKC_RSTRAM}	Synchronous RSTRAM input	0.27/0.35	0.29/0.37	0.31/0.39	ns, Min
T _{RCKC_WEA} /T _{RCKC_WEA}	Write Enable (WE) input (Block RAM only)	0.38/0.15	0.41/0.16	0.46/0.17	ns, Min
T _{RCKC_WREN} /T _{RCKC_WREN}	WREN FIFO inputs	0.39/0.25	0.39/0.30	0.40/0.37	ns, Min
T _{RCKC_RDEN} /T _{RCKC_RDEN}	RDEN FIFO inputs	0.36/0.26	0.36/0.30	0.37/0.37	ns, Min
Reset Delays					
T _{RCO_FLAGS}	Reset RST to FIFO flags/pointers ⁽¹⁰⁾	0.76	0.83	0.93	ns, Max
T _{RREC_RST} /T _{RREM_RST}	FIFO reset recovery and removal timing ⁽¹¹⁾	1.59/–0.68	1.76/–0.68	2.01/–0.68	ns, Max

Table 37: Duty Cycle Distortion and Clock Tree Skew

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
T _{DCD_CLK}	Global clock tree duty cycle distortion ⁽¹⁾	All	0.20	0.20	0.20	ns
T _{CKSKEW}	Global clock tree skew ⁽²⁾	XC7V585T	0.75	0.91	0.98	ns
		XC7V2000T	N/A	0.39	0.39	ns
		XC7VX330T	0.60	0.74	0.79	ns
		XC7VX415T	0.76	0.84	0.91	ns
		XC7VX485T	0.60	0.74	0.79	ns
		XC7VX550T	0.73	0.88	0.96	ns
		XC7VX690T	0.73	0.88	0.96	ns
		XC7VX980T	N/A	0.91	0.98	ns
		XC7VX1140T	N/A	0.39	0.39	ns
T _{DCD_BUFIN}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	ns
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	ns
T _{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip-flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements in a single SLR. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 38: MMCM Specification

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
MMCM_F _{INMAX}	Maximum input clock frequency	1066.00	933.00	800.00	MHz
MMCM_F _{INMIN}	Minimum input clock frequency	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
MMCM_F _{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	550.00	500.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs ⁽²⁾	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter	Note 3			
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision ⁽⁴⁾	0.20	0.20	0.20	ns

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 45: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks (only)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾						
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) Global clock Input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7V585T	3.12/−0.37	3.19/−0.37	3.42/−0.37	ns
		XC7V2000T	N/A	N/A	N/A	ns
		XC7VX330T	2.90/−0.31	2.96/−0.31	3.16/−0.31	ns
		XC7VX415T	N/A	N/A	N/A	ns
		XC7VX485T	N/A	N/A	N/A	ns
		XC7VX550T	N/A	N/A	N/A	ns
		XC7VX690T	N/A	N/A	N/A	ns
		XC7VX980T	N/A	N/A	N/A	ns
		XC7VX1140T	N/A	N/A	N/A	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch

Table 46: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾⁽²⁾						
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽³⁾ with MMCM	XC7V585T	2.71/−0.10	3.00/−0.10	3.33/−0.10	ns
		XC7V2000T	N/A	2.60/−0.24	2.87/−0.24	ns
		XC7VX330T	2.58/−0.15	2.87/−0.15	3.18/−0.15	ns
		XC7VX415T	2.73/0.01	3.03/0.01	3.36/0.01	ns
		XC7VX485T	2.58/−0.15	2.87/−0.15	3.18/−0.15	ns
		XC7VX550T	2.72/−0.09	3.01/−0.09	3.34/−0.09	ns
		XC7VX690T	2.72/0.01	3.01/0.01	3.34/0.01	ns
		XC7VX980T	N/A	3.01/−0.10	3.36/−0.10	ns
		XC7VX1140T	N/A	2.61/−0.24	2.88/−0.24	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-7 T and XT FPGA clock transmitter and receiver data-valid windows.

Table 50: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC7V585T	FFG1157	232	ps
			FFG1761	255	ps
		XC7V2000T	FHG1761	308	ps
			FLG1925	266	ps
		XC7VX330T	FFG1157	170	ps
			FFG1761	270	ps
		XC7VX415T	FFG1157	203	ps
			FFG1158	237	ps
			FFG1927	183	ps
		XC7VX485T	FFG1157	191	ps
			FFG1158	209	ps
			FFG1761	274	ps
			FFG1927	209	ps
			FFG1930	304	ps
		XC7VX550T	FFG1158	217	ps
			FFG1927	254	ps
		XC7VX690T	FFG1157	239	ps
			FFG1158	217	ps
			FFG1761	284	ps
			FFG1926	238	ps
			FFG1927	254	ps
			FFG1930	287	ps
		XC7VX980T	FFG1926	242	ps
			FFG1928	199	ps
			FFG1930	243	ps
		XC7VX1140T	FLG1926	271	ps
			FLG1928	216	ps
			FLG1930	279	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
- Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 55: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

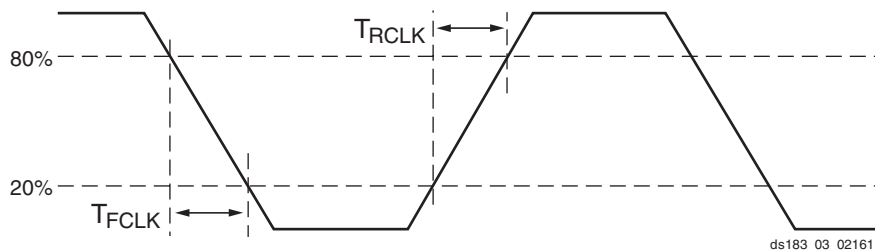


Figure 3: Reference Clock Timing Parameters

Table 56: GTX Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 57: GTX Transceiver User Clock Switching Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3/-2G ⁽³⁾	-2/-2L ⁽³⁾	-1 ⁽⁴⁾	
F _{TXOUT}	TXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F _{RXOUT}	RXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F _{RXIN}	RXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F _{TXIN2}	TXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz
F _{RXIN2}	RXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L, and -2G, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s. For speed grade -1C with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.500	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	40	–	ps
T _{FTX}	TX fall time	80%–20%	–	40	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500	ps
V _{TXOVBVDP}	Electrical idle amplitude		–	–	15	mV
T _{TXOVBTRANSITION}	Electrical idle transition time		–	–	140	ns
TJ _{12.5}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
DJ _{12.5}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{11.18}	Total jitter ⁽²⁾⁽⁴⁾	11.18 Gb/s	–	–	0.28	UI
DJ _{11.18}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{10.3125}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
DJ _{10.3125}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{9.953}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
DJ _{9.953}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{9.8}	Total jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	–	–	0.28	UI
DJ _{9.8}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{8.0}	Total jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	–	–	0.30	UI
DJ _{8.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.15	UI
TJ _{6.6_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	6.6 Gb/s	–	–	0.28	UI
DJ _{6.6_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI

Table 63: CEI-6G and CEI-11G Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter ⁽²⁾	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽²⁾	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 64: SFP+ Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40 ⁽¹⁾	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40 ⁽¹⁾	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 72: GTH Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3E/-2GE ⁽²⁾	-2(C&I)/-2LE ⁽²⁾	-1(C&I) ⁽³⁾	
F _{TXOUT}	TXUSERCLKOUT maximum frequency			412.500	412.500	312.500	MHz
F _{RXOUT}	RXUSERCLKOUT maximum frequency			412.500	412.500	312.500	MHz
F _{TXIN}	TXUSERCLKIN maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	409.375	353.125	265.625	MHz
F _{RXIN}	RXUSERCLKIN maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	409.375	353.125	265.625	MHz
F _{TXIN2}	TXUSERCLKIN2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	409.375	353.125	265.625	MHz
		64-bit	64-bit	204.688	176.563	132.813	MHz
F _{RXIN2}	RXUSERCLKIN2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	409.375	353.125	265.625	MHz
		64-bit	64-bit	204.688	176.563	132.813	MHz

Notes:

- Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
- For speed grades -3E, -2GE, -2C, -2I, and -2LE, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
- For speed grade -1 (and when V_{CCINT} = 0.9V), a 16-bit data path can only be used for speeds less than 5.0 Gb/s.

Table 73: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	—	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	—	40	—	ps
T _{FTX}	TX fall time	80%–20%	—	40	—	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		—	—	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		—	—	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		—	—	140	ns
TJ _{13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	—	—	0.3	UI
DJ _{13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{12.5}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	—	—	0.28	UI
DJ _{12.5}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{11.3}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	—	—	0.28	UI
DJ _{11.3}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	—	—	0.28	UI
DJ _{10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	—	—	0.33	UI
DJ _{10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		—	—	0.17	UI
TJ _{9.953}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	—	—	0.28	UI
DJ _{9.953}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{9.8}	Total jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	—	—	0.28	UI
DJ _{9.8}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{8.0_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	—	—	0.28	UI
DJ _{8.0_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI

GTH Transceiver Protocol Jitter Characteristics

For Table 75 through Table 80, the 7 Series FPGAs GTX/GTH Transceiver User Guide ([UG476](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 75: Gigabit Ethernet Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 76: XAUI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 77: PCI Express Protocol Characteristics (GTH Transceivers)⁽¹⁾

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 ⁽³⁾	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

XADC Specifications

Table 82: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, T _j = −40°C to 100°C, Typical values at T _j =+40°C						
ADC Accuracy ⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±6	LSBs
Gain Error		Gain calibration disabled	–	–	±0.5	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio ⁽²⁾	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion ⁽²⁾	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	–	70	–	dB
ADC Accuracy at Extended Temperatures (−55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs ⁽³⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T _j = −40°C to 100°C.	–	–	±4	°C
		T _j = −55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −40°C to +100°C	–	–	±1	%
		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −55°C to +125°C	–	–	±2	%
Conversion Rate ⁽⁴⁾						
Conversion Time - Continuous	t _{CONV}	Number of ADCCLK cycles	26	–	32	cycle
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	cycle
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%

Table 83: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Master/Slave Serial Mode Programming Switching						
T _{DCC} /T _{CCKD}	DIN setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{CCO}	DOUT clock to out		8.0	8.0	8.0	ns, Max
SelectMAP Mode Programming Switching						
T _{SMDCC} /T _{SMCCKD}	D[31:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T _{SMWCCK} /T _{SMCCKW}	RDWR_B setup/hold		10.0/0.0	10.0/0.0	10.0/0.0	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)		7.0	7.0	7.0	ns, Max
T _{SMCO}	D[31:00] clock to out in readback		8.0	8.0	8.0	ns, Max
F _{RBCK}	Readback frequency	SLR-based	70	70	70	MHz, Max
		All other devices	100	100	100	MHz, Max
Boundary-Scan Port Timing Specifications						
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup/hold	SLR-based	9.0/2.0	9.0/2.0	9.0/2.0	ns, Min
		All other devices	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output	SLR-based	17	17	17	ns, Max
		All other devices	7.0	7.0	7.0	ns, Max
F _{TCK}	TCK frequency	SLR-based	20	20	20	MHz, Max
		All other devices	66	66	66	MHz, Max
BPI Master Flash Mode Programming Switching						
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out		8.5	8.5	8.5	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
SPI Master Flash Mode Programming Switching						
T _{SPIDCC} /T _{SPICCD}	D[03:00] setup/hold		3.0/0.0	3.0/0.0	3.0/0.0	ns, Min
T _{SPICCM}	MOSI clock to out		8.0	8.0	8.0	ns, Max
T _{SPICCF}	FCS_B clock to out		8.0	8.0	8.0	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* ([UG470](#)).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 84 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* ([UG470](#)).

Table 84: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	—	—	115	mA
t_j	Temperature range	15	—	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.