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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	32200
Number of Logic Elements/Cells	412160
Total RAM Bits	32440320
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1157-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx415t-2ff1157i

Table 6: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX/GTH transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Table 10: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 12.
7. LVDS is specified in Table 13.

Table 11: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the ISE® Design Suite 14.5 and Vivado® Design Suite 2013.1 as outlined in Table 14.

Table 14: **Virtex-7 T and XT FPGA Speed Specification Version By Device/Speed Grade**

Version In:		Typical V_{CCINT}	Device
ISE 14.5	Vivado 2013.1	(Table 2)	
1.09	1.09	1.0V	XC7V585T, XC7VX485T
N/A	1.08	1.0V	XC7V2000T
1.08	1.08	1.0V	XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T
N/A	1.08	1.0V	XC7VX1140T

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-7 T and XT FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Virtex-7 T and XT device on a per speed grade basis.

Table 15: **Virtex-7 T and XT Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7V585T			-3, -2, -2L, -1
XC7V2000T	-2L, -2G		-2, -1
XC7VX330T			-3, -2, -2L, -1
XC7VX415T			-3, -2, -2L, -1
XC7VX485T			-3, -2, -2L, -1
XC7VX550T			-3, -2, -2L, -1
XC7VX690T			-3, -2, -2L, -1
XC7VX980T	-2, -2L, -1		
XC7VX1140T	-2, -2L, -2G, -1		

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 16 lists the production released Virtex-7 T and XT device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 16: **Virtex-7 T and XT Device Production Software and Speed Specification Release**

Device	Speed Grade Designations				
	-3	-2G	-2	-2L	-1
XC7V585T	Vivado 2012.4 v1.08 or ISE 14.2 v1.06	N/A	Vivado 2012.4 v1.08 or ISE 14.2 v1.06		
XC7V2000T	N/A		Vivado 2012.4 v1.07		Vivado 2012.4 v1.07
XC7VX330T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX415T		N/A			
XC7VX485T	Vivado 2012.4 v1.08 or ISE 14.2 v1.06	N/A	Vivado 2012.4 v1.08 or ISE 14.2 v1.06		
XC7VX550T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX690T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX980T	N/A	N/A			
XC7VX1140T	N/A				

Notes:

1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
DIFF_HSTL_I_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.68	1.91	2.06	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.98	1.09	1.16	1.62	1.85	1.98	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.67	1.91	2.06	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.98	1.09	1.16	1.61	1.85	1.98	ns
DIFF_HSTL_II _T_DCI_18_F	0.75	0.79	0.92	1.04	1.16	1.24	1.67	1.91	2.06	ns
LVCMOS18_S2	0.47	0.50	0.60	3.95	4.28	4.85	4.59	5.04	5.67	ns
LVCMOS18_S4	0.47	0.50	0.60	2.67	2.98	3.43	3.31	3.73	4.26	ns
LVCMOS18_S6	0.47	0.50	0.60	2.14	2.38	2.72	2.77	3.14	3.54	ns
LVCMOS18_S8	0.47	0.50	0.60	1.98	2.21	2.52	2.61	2.97	3.35	ns
LVCMOS18_S12	0.47	0.50	0.60	1.70	1.91	2.17	2.34	2.67	2.99	ns
LVCMOS18_S16	0.47	0.50	0.60	1.57	1.75	1.97	2.20	2.51	2.79	ns
LVCMOS18_F2	0.47	0.50	0.60	3.50	3.87	4.48	4.14	4.63	5.30	ns
LVCMOS18_F4	0.47	0.50	0.60	2.23	2.50	2.87	2.87	3.25	3.69	ns
LVCMOS18_F6	0.47	0.50	0.60	1.80	2.00	2.26	2.43	2.76	3.08	ns
LVCMOS18_F8	0.47	0.50	0.60	1.46	1.72	2.04	2.10	2.47	2.86	ns
LVCMOS18_F12	0.47	0.50	0.60	1.26	1.40	1.53	1.89	2.16	2.35	ns
LVCMOS18_F16	0.47	0.50	0.60	1.19	1.33	1.44	1.83	2.08	2.26	ns
LVCMOS15_S2	0.59	0.62	0.73	3.55	3.89	4.45	4.19	4.65	5.27	ns
LVCMOS15_S4	0.59	0.62	0.73	2.45	2.70	3.06	3.08	3.45	3.89	ns
LVCMOS15_S6	0.59	0.62	0.73	2.24	2.51	2.88	2.88	3.26	3.71	ns
LVCMOS15_S8	0.59	0.62	0.73	1.91	2.16	2.49	2.55	2.91	3.31	ns
LVCMOS15_S12	0.59	0.62	0.73	1.77	1.98	2.23	2.41	2.73	3.05	ns
LVCMOS15_S16	0.59	0.62	0.73	1.62	1.81	2.02	2.26	2.56	2.84	ns
LVCMOS15_F2	0.59	0.62	0.73	3.38	3.69	4.18	4.02	4.44	5.00	ns
LVCMOS15_F4	0.59	0.62	0.73	2.04	2.21	2.44	2.68	2.97	3.26	ns
LVCMOS15_F6	0.59	0.62	0.73	1.47	1.74	2.09	2.10	2.50	2.91	ns
LVCMOS15_F8	0.59	0.62	0.73	1.31	1.46	1.61	1.95	2.22	2.43	ns
LVCMOS15_F12	0.59	0.62	0.73	1.21	1.34	1.45	1.84	2.10	2.27	ns
LVCMOS15_F16	0.59	0.62	0.73	1.18	1.31	1.41	1.82	2.07	2.23	ns
LVCMOS12_S2	0.64	0.67	0.78	3.38	3.80	4.48	4.02	4.55	5.30	ns
LVCMOS12_S4	0.64	0.67	0.78	2.62	2.94	3.43	3.26	3.70	4.25	ns
LVCMOS12_S6	0.64	0.67	0.78	2.05	2.33	2.72	2.69	3.08	3.54	ns
LVCMOS12_S8	0.64	0.67	0.78	1.94	2.18	2.51	2.58	2.94	3.33	ns
LVCMOS12_F2	0.64	0.67	0.78	2.84	3.15	3.62	3.48	3.90	4.44	ns
LVCMOS12_F4	0.64	0.67	0.78	1.97	2.18	2.44	2.61	2.93	3.26	ns
LVCMOS12_F6	0.64	0.67	0.78	1.33	1.51	1.70	1.96	2.26	2.52	ns
LVCMOS12_F8	0.64	0.67	0.78	1.27	1.42	1.55	1.91	2.18	2.37	ns
LVDCI_18	0.47	0.50	0.60	1.99	2.15	2.35	2.62	2.91	3.17	ns

Output Serializer/Deserializer Switching Characteristics

Table 25: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T_{OSDCK_D}/T_{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input setup/hold with respect to CLK	0.49/–0.15	0.56/–0.15	0.68/–0.15	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input setup/hold with respect to CLKDIV	0.27/–0.15	0.30/–0.15	0.34/–0.15	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T_{OSCCK_S}	SR (Reset) input setup with respect to CLKDIV	0.41	0.46	0.75	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Sequential Delays					
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	ns
Combinatorial					
T_{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T_{SHCKO}[1]	Clock to A – B outputs	0.68	0.70	0.85	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	ns, Min
$T_{CECK\_LRAM}/T_{CKCE\_LRAM}$	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	ns, Min
Clock CLK					
T_{MPW}	Minimum pulse width	0.68	0.77	0.91	ns, Min
T_{MCP}	Minimum clock period	1.35	1.54	1.82	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T_{REG}	Clock to A – D outputs	0.96	0.98	1.20	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK					
$T_{WS\_SHFREG}/T_{WH\_SHFREG}$	WE input	0.26/0.09	0.27/0.09	0.33/0.09	ns, Min
$T_{CECK\_SHFREG}/T_{CKCE\_SHFREG}$	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	ns, Min
$T_{DS\_SHFREG}/T_{DH\_SHFREG}$	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	ns, Min
Clock CLK					
T_{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	ns, Min

Table 31: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Maximum Frequency					
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	601.32	543.77	458.09	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601.32	543.77	458.09	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528.26	477.33	400.80	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551.27	493.83	408.00	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551.27	493.83	408.00	MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478.24	427.35	350.88	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	601.32	543.77	458.09	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	484.26	430.85	351.12	MHz

Notes:

1. The timing report shows all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 32: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup and Hold Times of Data/Control Pins to the Input Register Clock					
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.24/0.12	0.27/0.14	0.31/0.16	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.28/0.13	0.32/0.14	0.39/0.15	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.15/0.15	0.17/0.17	0.20/0.20	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.21/0.19	0.27/0.22	0.35/0.26	ns
$T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.21/0.12	0.24/0.14	0.27/0.16	ns
$T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.22/0.13	0.25/0.14	0.30/0.15	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock					
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$	{A, B,} input to M register CLK using multiplier	2.04/–0.01	2.34/–0.01	2.79/–0.01	ns
$T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$	{A, D} input to AD register CLK	1.09/–0.02	1.25/–0.02	1.49/–0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock					
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG\_MULT}$	{A, B,} input to P register CLK using multiplier	3.41/–0.24	3.90/–0.24	4.64/–0.24	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.33/–0.62	3.81/–0.62	4.53/–0.62	ns
$T_{DSPDCK\_\{A, B\}\ \_PREG}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG}$	A or B input to P register CLK not using multiplier	1.47/–0.24	1.68/–0.24	2.00/–0.24	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.30/–0.22	1.49/–0.22	1.78/–0.22	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.12/–0.13	1.28/–0.13	1.52/–0.13	ns
Setup and Hold Times of the CE Pins					
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.30/0.05	0.36/0.06	0.44/0.09	ns
$T_{DSPDCK\_CEC\_CREG}$/$T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.24/0.08	0.29/0.09	0.36/0.11	ns
$T_{DSPDCK\_CED\_DREG}$/$T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.31/–0.02	0.36/–0.02	0.44/–0.02	ns
$T_{DSPDCK\_CEM\_MREG}$/$T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.26/0.15	0.29/0.17	0.33/0.20	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.31/0.01	0.36/0.01	0.45/0.01	ns
Setup and Hold Times of the RST Pins					
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.34/0.10	0.39/0.11	0.47/0.13	ns
$T_{DSPDCK\_RSTC\_CREG}$/$T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.06/0.22	0.07/0.24	0.08/0.26	ns
$T_{DSPDCK\_RSTD\_DREG}$/$T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.37/0.06	0.42/0.06	0.50/0.07	ns
$T_{DSPDCK\_RSTM\_MREG}$/$T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.18/0.18	0.20/0.21	0.23/0.24	ns
$T_{DSPDCK\_RSTP\_PREG}$/$T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.24/0.01	0.26/0.01	0.30/0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.21	3.69	4.39	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.15	3.61	4.30	ns

Table 32: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Clock to Outs from Input Register Clock to Cascading Output Pins					
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK (BREG) to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK (DREG) to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK (CREG) to CARRYCASCOUT output	1.64	1.88	2.23	ns
Maximum Frequency					
F_{MAX}	With all registers used	741.84	650.20	547.95	MHz
F_{MAX_PATDET}	With pattern detector	627.35	549.75	463.61	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	412.20	360.75	303.77	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	468.82	408.66	342.70	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	468.82	408.66	342.58	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	MHz

Table 47: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)(2)						
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(3) with PLL	XC7V585T	3.07/–0.21	3.40/–0.21	3.72/–0.21	ns
		XC7V2000T	N/A	2.99/–0.35	3.27/–0.35	ns
		XC7VX330T	2.94/–0.26	3.26/–0.26	3.57/–0.26	ns
		XC7VX415T	3.09/–0.10	3.42/–0.10	3.75/–0.10	ns
		XC7VX485T	2.95/–0.26	3.26/–0.26	3.58/–0.26	ns
		XC7VX550T	3.08/–0.20	3.40/–0.20	3.74/–0.20	ns
		XC7VX690T	3.08/–0.10	3.40/–0.10	3.74/–0.10	ns
		XC7VX980T	N/A	3.39/–0.21	3.72/–0.21	ns
		XC7VX1140T	N/A	3.00/–0.35	3.27/–0.35	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. IFF = Input Flip-Flop or Latch
4. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T_{PSCS}/T_{PHCS}	Setup/hold of I/O clock for HR I/O banks	–0.36/1.36	–0.36/1.50	–0.36/1.70	ns
	Setup/hold of I/O clock for HP I/O banks	–0.34/1.39	–0.34/1.53	–0.34/1.73	ns

Table 49: **Sample Window**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{SAMP}	Sampling error at receiver pins(1)	0.51	0.56	0.61	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO(2)	0.30	0.35	0.40	ns

Notes:

1. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-7 T and XT FPGA clock transmitter and receiver data-valid windows.

Table 50: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC7V585T	FFG1157	232	ps
			FFG1761	255	ps
		XC7V2000T	FHG1761	308	ps
			FLG1925	266	ps
		XC7VX330T	FFG1157	170	ps
			FFG1761	270	ps
		XC7VX415T	FFG1157	203	ps
			FFG1158	237	ps
			FFG1927	183	ps
		XC7VX485T	FFG1157	191	ps
			FFG1158	209	ps
			FFG1761	274	ps
			FFG1927	209	ps
			FFG1930	304	ps
		XC7VX550T	FFG1158	217	ps
			FFG1927	254	ps
		XC7VX690T	FFG1157	239	ps
			FFG1158	217	ps
			FFG1761	284	ps
			FFG1926	238	ps
			FFG1927	254	ps
			FFG1930	287	ps
		XC7VX980T	FFG1926	242	ps
			FFG1928	199	ps
			FFG1930	243	ps
		XC7VX1140T	FLG1926	271	ps
			FLG1928	216	ps
			FLG1930	279	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 59: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.500	–	F_{GTXMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)		–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.3	–	–	UI
$JT\_SJ_{11.18}$	Sinusoidal jitter (QPLL)(3)	11.18 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.95}$	Sinusoidal jitter (QPLL)(3)	9.95 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.8}$	Sinusoidal jitter (QPLL)(3)	9.8 Gb/s	0.3	–	–	UI
$JT\_SJ_{8.0}$	Sinusoidal jitter (QPLL)(3)	8.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{6.6\_QPLL}$	Sinusoidal jitter (QPLL)(3)	6.6 Gb/s	0.48	–	–	UI
$JT\_SJ_{6.6\_CPLL}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal jitter (CPLL)(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{3.2L}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(5)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(6)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(7)	0.5	–	–	UI
JT_SJ_{500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$JT\_TJSE_{6.6}$		6.6 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.1	–	–	UI
$JT\_SJSE_{6.6}$		6.6 Gb/s	0.1	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.

Table 70: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

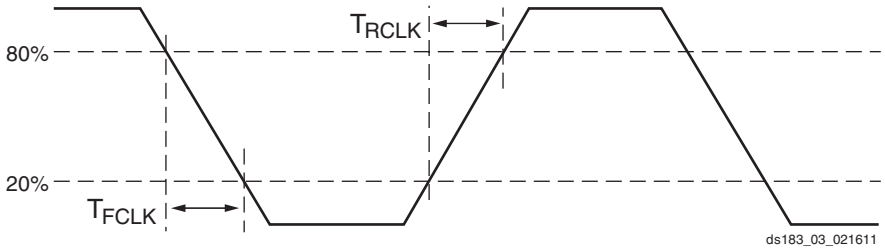

Figure 6: **Reference Clock Timing Parameters**

Table 71: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 73: **GTH Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$TJ_{8.0\_CPLL}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$DJ_{8.0\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$TJ_{6.6\_QPLL}$	Total jitter(2)(4)	6.6 Gb/s	–	–	0.28	UI
$DJ_{6.6\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{6.6\_CPLL}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$DJ_{6.6\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$TJ_{5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$TJ_{4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$TJ_{3.75}$	Total jitter(3)(4)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$TJ_{3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.2	UI
$DJ_{3.20}$	Deterministic jitter(3)(4)		–	–	0.1	UI
$TJ_{3.20L}$	Total jitter(3)(4)	3.20 Gb/s(6)	–	–	0.32	UI
$DJ_{3.20L}$	Deterministic jitter(3)(4)		–	–	0.16	UI
$TJ_{2.5}$	Total jitter(3)(4)	2.5 Gb/s(7)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic jitter(3)(4)		–	–	0.08	UI
$TJ_{1.25}$	Total jitter(3)(4)	1.25 Gb/s(8)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic jitter(3)(4)		–	–	0.06	UI
TJ_{500}	Total jitter(3)(4)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTH Quads).
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of $1e^{-12}$.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 80: **CPRI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 79.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 81: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
$F_{USERCLK}$	User clock maximum frequency	500.00	500.00	250.00	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz

Table 82: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference(5)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for new BitGen option XADCEnhancedLinearity = ON.
3. For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
4. For a detailed description, see the Timing chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 83: **Configuration Switching Characteristics**

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Power-up Timing Characteristics						
T_{PL}(1)	Program latency		5	5	5	ms, Max
T_{POR}(1)	Power-on reset (50ms ramp rate time)		10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1ms ramp rate time)		10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width		250	250	250	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay		150	150	150	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle		40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle		40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency		100	100	100	MHz, Max
	Master CCLK frequency for AES encrypted x16		50	50	50	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration		3	3	3	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK.		±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time		2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time		2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave CCLK frequency		100	100	100	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time		2.5	2.5	2.5	ns, Min
T_{EMCCKH}	External master CCLK High time		2.5	2.5	2.5	ns, Min
F_{EMCCK}	External master CCLK frequency		100	100	100	MHz, Max
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2)		100.00	100.00	100.00	MHz, Max

Table 83: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T_{CCO}	DOUT clock to out		8.0	8.0	8.0	ns, Max
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	D[31:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B setup/hold		10.0/0.0	10.0/0.0	10.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)		7.0	7.0	7.0	ns, Max
T_{SMCO}	D[31:00] clock to out in readback		8.0	8.0	8.0	ns, Max
F_{RBCCK}	Readback frequency	SLR-based	70	70	70	MHz, Max
		All other devices	100	100	100	MHz, Max
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold	SLR-based	9.0/2.0	9.0/2.0	9.0/2.0	ns, Min
		All other devices	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	SLR-based	17	17	17	ns, Max
		All other devices	7.0	7.0	7.0	ns, Max
F_{TCK}	TCK frequency	SLR-based	20	20	20	MHz, Max
		All other devices	66	66	66	MHz, Max
BPI Master Flash Mode Programming Switching						
T_{BPICCO} (2)	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out		8.5	8.5	8.5	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
SPI Master Flash Mode Programming Switching						
T_{SPIDCC}/T_{SPICCD}	D[03:00] setup/hold		3.0/0.0	3.0/0.0	3.0/0.0	ns, Min
T_{SPICCM}	MOSI clock to out		8.0	8.0	8.0	ns, Max
$T_{SPICCFC}$	FCS_B clock to out		8.0	8.0	8.0	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 84 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470).

Table 84: **eFUSE Programming Conditions** (1)

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document.

Date	Version	Description
03/01/2011	1.0	Initial Xilinx release.
10/05/2011	1.1	Removed the XC7V285T, XC7V450T, and XC7V855T devices from the entire data sheet. Added the XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T, and XC7VX1140T devices to the entire data sheet. Replaced -1L with -2L throughout this data sheet. Added the extended temperature range discussion to page 1. Updated Min/Max values and removed Note 5 from Table 2. Clarified Power-On/Off Power Supply Sequencing power sequencing discussion including adding $T_{VCCO2VCCAUX}$ to Table 8. Added I_{CCAUX_IO} and I_{CCBRAM} to Table 6 and Table 7. Updated V_{ICM} in Table 12 and Table 13. Added Note 1 to Table 12. Updated Table 84 including adding Note 1. Added Table 13. Revised the reference clock maximum frequency (F_{GCLK}) in Table 55. Added Table 57. Added GTH Transceiver Specifications section. Removed erroneous instances of HSTL_III from Table 20. Removed the *I/O Standard Adjustment Measurement Methodology* section. Use IBIS for more accurate information and measurements. Updated $T_{IDELAYPAT\_JIT}$ in Table 26. Added T_{AS}/T_{AH} to Table 28. Added $T_{RDCK\_DI\_WF\_NC}/T_{RCKD\_DI\_WF\_NC}$ and $T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$ to Table 31. Completely updated the specifications in Table 83. Updated MMCM_F_{INDUTY} and added $F_{INJITTER}$, $T_{OUTJITTER}$, and $T_{EXTFDVAR}$ and Note 3 to Table 38. Updated the AC Switching Characteristics section. Updated the Table 50 package list. Updated the Notice of Disclaimer.
11/07/2011	1.2	Added -2G speed grade, where appropriate, throughout document. Revised the V_{OCM} specification in Table 12. Updated the AC Switching Characteristics based upon the ISE 13.3 v1.02 speed specification throughout document including Table 19 and Table 20. Added MMCM to the symbol names of a few specifications in Table 38 and PLL to the symbol names in Table 39. In Table 40 through Table 47, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 49.
02/13/2012	1.3	Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Added typical numbers to Table 3. Updated the notes in Table 6. Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to Table 8. Rearranged Table 9, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 10 and Table 11. Revised the specifications in Table 12 and Table 13. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the IO_FIFO Switching Characteristics table. Revised I_{CCADC} and updated Note 1 in Table 82. Revised DDR LVDS transmitter data width in Table 17. Updated the AC Switching Characteristics based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from Table 28 as they are no longer applicable. Updated specifications in Table 83. Updated Note 1 in Table 37. In the GTX Transceiver Specifications section: Revised V_{IN}, and added I_{DCIN} and I_{DCOUT} to Table 51. Updated and added notes to Table 53. In Table 55, revised F_{GCLK}, removed T_{PHASE}, and added T_{DLOCK}. Revised specifications and added Note 2 to Table 57. Added Table 58 and Table 59 along with GTX Transceiver Protocol Jitter Characteristics in Table 60 through Table 65.
05/23/2012	1.4	Reorganized entire data sheet including adding Table 44 and Table 48. Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Added values to Table 6 and Table 7. Updated Power-On/Off Power Supply Sequencing section with regards to GTX/GTH transceivers. Updated many parameters in Table 9, including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 11. Updated V_{OL} in Table 12. Updated Table 17 and removed notes 2 and 3. Updated Table 18. Updated the AC Switching Characteristics section based upon the ISE 14.1 v1.04 for the -3, -2, -2L (1.0V), -1, and v1.05 for the -2L (0.9V) speed specifications throughout the document. In Table 31, updated Reset Delays section including Note 10 and Note 11. Added data for T_{LOCK} and T_{DLOCK} in Table 55. Updated many of the XADC specifications in Table 82 and added Note 2. Updated and moved *Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK* section from Table 83 to Table 38 and Table 39.