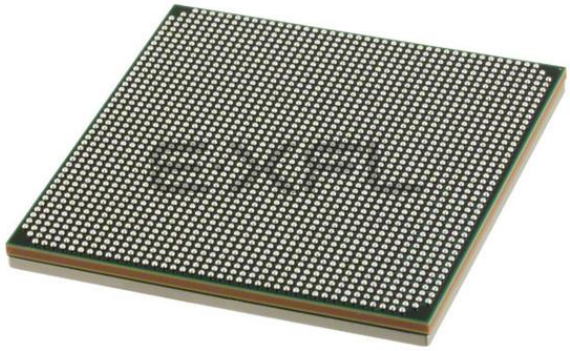
AMD Xilinx - XC7VX415T-2FFG1927C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	32200
Number of Logic Elements/Cells	412160
Total RAM Bits	32440320
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1927-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx415t-2ffg1927c

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ[1]	Max	Units
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}[3]	Battery supply current	–	–	150	nA
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V_{CCO}/2 level.

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[1]**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 6: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: **SelectIO DC Input and Output Levels(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	6.3	–6.3
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15, LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18, LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 6	Note 6
LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO} – 0.400	Note 6	Note 6
LVTTL	–0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.1	–0.1
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.0	–13.0
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.9	–8.9
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.0	–13.0
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.9	–8.9
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8	–8
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.4	–13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471).

LVDS DC Specifications (LVDS_25)

The LVDS standard is available in the HR I/O banks.

Table 12: **LVDS_25 DC Specifications(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks.

Table 13: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		1.710	1.800	1.890	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ±350 mV	0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

Table 18: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
4:1 Memory Controllers						
DDR3	HP	2.0V	1866	1866	1600	Mb/s
	HP	1.8V	1600	1333	1066	Mb/s
	HR	N/A	1066	1066	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	Mb/s
	HP	1.8V	1333	1066	800	Mb/s
	HR	N/A	800	800	667	Mb/s
DDR2	HP	2.0V	800	800	800	Mb/s
	HP	1.8V	800	800	800	Mb/s
	HR	N/A	800	800	800	Mb/s
RLDRAM III	HP	2.0V	800	667	667	MHz
	HP	1.8V	550	500	450	MHz
	HR	N/A	N/A			
2:1 Memory Controllers						
DDR3	HP	2.0V	1066	1066	800	Mb/s
	HP	1.8V	1066	1066	800	Mb/s
	HR	N/A	1066	1066	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	Mb/s
	HP	1.8V	1066	1066	800	Mb/s
	HR	N/A	800	800	667	Mb/s
DDR2	HP	2.0V	800	800	800	Mb/s
	HP	1.8V				
	HR	N/A				
QDR II+(3)	HP	2.0V	550	500	450	MHz
	HP	1.8V				
	HR	N/A	500	450	400	MHz
RLDRAM II	HP	2.0V	533	500	450	MHz
	HP	1.8V				
	HR	N/A				
LPDDR2	HP	2.0V	667	667	667	Mb/s
	HP	1.8V	667	667	667	Mb/s
	HR	N/A	667	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 19: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVCMOS15_F4	0.66	0.69	0.81	1.63	1.76	1.86	2.39	2.62	2.85	ns
LVCMOS15_F8	0.66	0.69	0.81	1.79	1.99	2.18	2.55	2.85	3.17	ns
LVCMOS15_F12	0.66	0.69	0.81	1.40	1.54	1.65	2.16	2.40	2.64	ns
LVCMOS15_F16	0.66	0.69	0.81	1.37	1.51	1.61	2.13	2.37	2.60	ns
LVCMOS12_S4	0.88	0.91	1.00	2.53	2.67	2.76	3.29	3.53	3.75	ns
LVCMOS12_S8	0.88	0.91	1.00	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVCMOS12_S12(1)	0.88	0.91	1.00	1.75	1.89	1.98	2.51	2.75	2.97	ns
LVCMOS12_F4	0.88	0.91	1.00	1.94	2.07	2.17	2.70	2.93	3.16	ns
LVCMOS12_F8	0.88	0.91	1.00	1.50	1.64	1.73	2.26	2.50	2.72	ns
LVCMOS12_F12(1)	0.88	0.91	1.00	1.54	1.71	1.87	2.30	2.57	2.86	ns
SSTL135_S	0.61	0.64	0.73	1.27	1.40	1.50	2.03	2.26	2.49	ns
SSTL15_S	0.61	0.64	0.73	1.24	1.37	1.47	2.00	2.23	2.46	ns
SSTL18_I_S	0.64	0.67	0.76	1.59	1.74	1.85	2.35	2.60	2.84	ns
SSTL18_II_S	0.64	0.67	0.76	1.27	1.40	1.50	2.03	2.26	2.49	ns
DIFF_SSTL135_S	0.59	0.61	0.73	1.27	1.40	1.50	2.03	2.26	2.49	ns
DIFF_SSTL15_S	0.63	0.67	0.77	1.24	1.37	1.47	2.00	2.23	2.46	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	1.50	1.63	1.72	2.26	2.49	2.71	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	1.13	1.22	1.25	1.89	2.08	2.24	ns
SSTL135_F	0.61	0.64	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
SSTL15_F	0.61	0.64	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
SSTL18_I_F	0.64	0.67	0.76	1.12	1.22	1.26	1.88	2.08	2.25	ns
SSTL18_II_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
DIFF_SSTL135_F	0.59	0.61	0.73	1.04	1.17	1.26	1.80	2.03	2.25	ns
DIFF_SSTL15_F	0.63	0.67	0.77	1.04	1.17	1.26	1.80	2.03	2.25	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	1.10	1.19	1.23	1.86	2.05	2.22	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	1.02	1.10	1.14	1.78	1.96	2.13	ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
SSTL15_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL135_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
SSTL12_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.94	1.06	1.15	1.58	1.82	1.97	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.97	1.09	1.16	1.61	1.84	1.99	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL135_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 21 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 21: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	ns
$T_{IOIBUFDISABLE\_HR}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	ns
$T_{IOIBUFDISABLE\_HP}$	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	ns

Table 23: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T_{ODCK}/T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.45/–0.13	0.50/–0.13	0.58/–0.13	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T_{OSRCK}/T_{OCKSR}	SR pin setup/hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.49/–0.16	0.56/–0.16	0.68/–0.16	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Combinatorial					
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	ns
Sequential Delays					
T_{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	ns
$T_{RQ\_OLOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	ns
$T_{GSRQ\_OLOGICE2}$	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
$T_{RQ\_OLOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	ns
$T_{GSRQ\_OLOGICE3}$	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
$T_{RPW\_OLOGICE2}$	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	ns, Min
$T_{RPW\_OLOGICE3}$	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	ns, Min

Table 27: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IO_FIFO Clock to Out Delays					
T_{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags	0.59	0.62	0.81	ns
Setup/Hold					
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.43/–0.01	0.47/–0.01	0.53/–0.01	ns
$T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$	WREN to WRCLK	0.39/–0.01	0.43/–0.01	0.50/–0.01	ns
$T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	ns
Minimum Pulse Width					
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
Maximum Frequency					
F_{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	MHz

CLB Switching Characteristics

Table 28: **CLB Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Combinatorial Delays					
T_{ILO}	An – Dn LUT address to A	0.05	0.05	0.06	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.15	0.16	0.19	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.24	0.25	0.30	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.58	0.61	0.74	ns, Max
T_{AXA}	AX inputs to AMUX output	0.38	0.40	0.49	ns, Max
T_{AXB}	AX inputs to BMUX output	0.40	0.42	0.52	ns, Max
T_{AXC}	AX inputs to CMUX output	0.39	0.41	0.50	ns, Max
T_{AXD}	AX inputs to DMUX output	0.43	0.44	0.52	ns, Max
T_{BXB}	BX inputs to BMUX output	0.31	0.33	0.40	ns, Max
T_{BXD}	BX inputs to DMUX output	0.38	0.39	0.47	ns, Max
T_{CXC}	CX inputs to CMUX output	0.27	0.28	0.34	ns, Max
T_{CXD}	CX inputs to DMUX output	0.33	0.34	0.41	ns, Max
T_{DXD}	DX inputs to DMUX output	0.32	0.33	0.40	ns, Max
Sequential Delays					
T_{CKO}	Clock to AQ – DQ outputs	0.26	0.27	0.32	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.32	0.32	0.39	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D flip-flops	0.01/0.12	0.02/0.13	0.03/0.18	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D flip-flops	0.04/0.14	0.04/0.14	0.05/0.20	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.36/0.10	0.37/0.11	0.46/0.16	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops	0.19/0.05	0.20/0.05	0.25/0.05	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	0.30/0.05	0.31/0.07	0.37/0.09	ns, Min
Set/Reset					
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.38	0.38	0.46	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.34	0.35	0.43	ns, Max
F_{TOG}	Toggle frequency (for export control)	1818	1818	1818	MHz

Block RAM and FIFO Switching Characteristics

Table 31: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Block RAM and FIFO Clock-to-Out Delays					
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	1.57	1.80	2.08	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.54	0.63	0.75	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.35	2.58	3.26	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.62	0.69	0.80	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	2.21	2.45	2.80	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	0.98	1.08	1.24	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.65	0.74	0.89	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.79	0.87	0.98	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register)	2.17	2.38	3.01	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	ns, Max
Setup and Hold Times Before/After Clock CLK					
$T_{RCCK\_ADDRA}/T_{RCKC\_ADDRA}$	ADDR inputs[8]	0.38/0.27	0.42/0.28	0.48/0.31	ns, Min
$T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9]	0.49/0.51	0.55/0.53	0.63/0.57	ns, Min
$T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode[9]	0.17/0.25	0.19/0.29	0.21/0.35	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.42/0.37	0.47/0.39	0.53/0.43	ns, Min
$T_{RDCK\_DI\_ECCW}/T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only[9]	0.79/0.37	0.87/0.39	0.99/0.43	ns, Min
$T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$	DIN inputs with FIFO ECC in standard mode[9]	0.89/0.47	0.98/0.50	1.12/0.54	ns, Min
$T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.49/0.30	0.55/0.31	0.63/0.34	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.30/0.17	0.33/0.18	0.38/0.20	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.21/0.13	0.25/0.13	0.31/0.14	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.25/0.06	0.27/0.06	0.29/0.06	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.27/0.35	0.29/0.37	0.31/0.39	ns, Min
$T_{RCCK\_WEA}/T_{RCKC\_WEA}$	Write Enable (WE) input (Block RAM only)	0.38/0.15	0.41/0.16	0.46/0.17	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.39/0.25	0.39/0.30	0.40/0.37	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.36/0.26	0.36/0.30	0.37/0.37	ns, Min
Reset Delays					
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers[10]	0.76	0.83	0.93	ns, Max
$T_{RREC\_RST}/T_{RREM\_RST}$	FIFO reset recovery and removal timing[11]	1.59/–0.68	1.76/–0.68	2.01/–0.68	ns, Max

Table 32: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$T_{DSPDO\_A\_P}$	A input to P output not using multiplier	1.30	1.48	1.76	ns
$T_{DSPDO\_C\_P}$	C input to P output	1.13	1.30	1.55	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.34	1.53	1.83	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.09	3.55	4.24	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.16	1.33	1.59	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.32	0.37	0.45	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	0.94	1.08	1.29	ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	ns
Clock to Outs from Output Register Clock to Output Pins					
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.35	0.39	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output	1.42	1.64	1.96	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier	2.30	2.63	3.13	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	ns
Clock to Outs from Input Register Clock to Output Pins					
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.34	3.83	4.55	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.39	1.59	1.88	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.43	1.64	1.95	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.32	3.80	4.51	ns

Clock Buffers and Networks

Table 33: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins setup/hold	0.12/0.30	0.14/0.38	0.26/0.38	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins setup/hold	0.12/0.30	0.14/0.38	0.26/0.38	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.10	0.12	ns
Maximum Frequency					
F_{MAX_BUFG}	Global clock tree (BUFG)	741.00	710.00	625.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 34: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BIOCKO_O}	Clock to out delay from I to O	1.04	1.14	1.32	ns
Maximum Frequency					
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800.00	800.00	710.00	MHz

Table 35: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BRCKO_O}	Clock to out delay from I to O	0.60	0.65	0.77	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.30	0.32	0.38	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.71	0.75	0.96	ns
Maximum Frequency					
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	600.00	540.00	450.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 36: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin setup and hold	0.20/0.16	0.23/0.20	0.38/0.21	ns
Maximum Frequency					
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	741.00	710.00	625.00	MHz

Table 37: **Duty Cycle Distortion and Clock Tree Skew**

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
T_{DCD_CLK}	Global clock tree duty cycle distortion(1)	All	0.20	0.20	0.20	ns
T_{CKSKEW}	Global clock tree skew(2)	XC7V585T	0.75	0.91	0.98	ns
		XC7V2000T	N/A	0.39	0.39	ns
		XC7VX330T	0.60	0.74	0.79	ns
		XC7VX415T	0.76	0.84	0.91	ns
		XC7VX485T	0.60	0.74	0.79	ns
		XC7VX550T	0.73	0.88	0.96	ns
		XC7VX690T	0.73	0.88	0.96	ns
		XC7VX980T	N/A	0.91	0.98	ns
		XC7VX1140T	N/A	0.39	0.39	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip-flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements in a single SLR. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 38: **MMCM Specification**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$MMCM\_F_{INMAX}$	Maximum input clock frequency	1066.00	933.00	800.00	MHz
$MMCM\_F_{INMIN}$	Minimum input clock frequency	10	10	10	MHz
$MMCM\_F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
$MMCM\_F_{INDUTY}$	Allowable input duty cycle: 10—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
$MMCM\_F_{MIN\_PSCLK}$	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	MHz
$MMCM\_F_{MAX\_PSCLK}$	Maximum dynamic phase shift clock frequency	550.00	500.00	450.00	MHz
$MMCM\_F_{VCOMIN}$	Minimum MMCM VCO frequency	600.00	600.00	600.00	MHz
$MMCM\_F_{VCOMAX}$	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	MHz
$MMCM\_F_{BANDWIDTH}$	Low MMCM bandwidth at typical(1)	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical(1)	4.00	4.00	4.00	MHz
$MMCM\_T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs(2)	0.12	0.12	0.12	ns
$MMCM\_T_{OUTJITTER}$	MMCM output jitter	Note 3			
$MMCM\_T_{OUTDUTY}$	MMCM output clock duty cycle precision(4)	0.20	0.20	0.20	ns

Table 63: **CEI-6G and CEI-11G Protocol Characteristics (GTX Transceivers)**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter(2)	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(2)	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 64: **SFP+ Protocol Characteristics (GTX Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40(1)	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40(1)	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 70: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

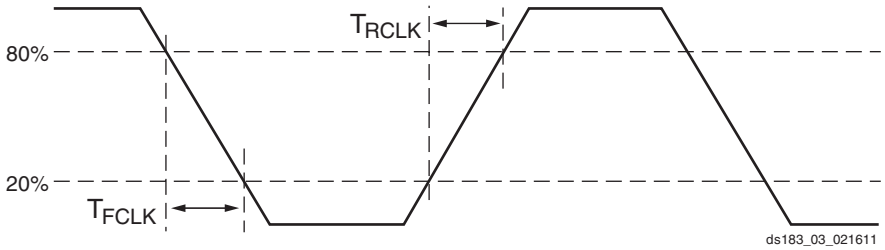

Figure 6: **Reference Clock Timing Parameters**

Table 71: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 73: **GTH Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$TJ_{8.0\_CPLL}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$DJ_{8.0\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$TJ_{6.6\_QPLL}$	Total jitter(2)(4)	6.6 Gb/s	–	–	0.28	UI
$DJ_{6.6\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{6.6\_CPLL}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$DJ_{6.6\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$TJ_{5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$TJ_{4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$TJ_{3.75}$	Total jitter(3)(4)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$TJ_{3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.2	UI
$DJ_{3.20}$	Deterministic jitter(3)(4)		–	–	0.1	UI
$TJ_{3.20L}$	Total jitter(3)(4)	3.20 Gb/s(6)	–	–	0.32	UI
$DJ_{3.20L}$	Deterministic jitter(3)(4)		–	–	0.16	UI
$TJ_{2.5}$	Total jitter(3)(4)	2.5 Gb/s(7)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic jitter(3)(4)		–	–	0.08	UI
$TJ_{1.25}$	Total jitter(3)(4)	1.25 Gb/s(8)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic jitter(3)(4)		–	–	0.06	UI
TJ_{500}	Total jitter(3)(4)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTH Quads).
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of $1e^{-12}$.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

GTH Transceiver Protocol Jitter Characteristics

For Table 75 through Table 80, the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476)contains recommended settings for optimal usage of protocol specific characteristics.

Table 75: **Gigabit Ethernet Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 76: **XAUI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 77: **PCI Express Protocol Characteristics (GTH Transceivers)(1)**

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3(2)	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2(3)	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3(2)	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 82: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference(5)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for new BitGen option XADCEnhancedLinearity = ON.
3. For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
4. For a detailed description, see the Timing chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 83: **Configuration Switching Characteristics**

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Power-up Timing Characteristics						
T_{PL}(1)	Program latency		5	5	5	ms, Max
T_{POR}(1)	Power-on reset (50ms ramp rate time)		10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1ms ramp rate time)		10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width		250	250	250	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay		150	150	150	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle		40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle		40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency		100	100	100	MHz, Max
	Master CCLK frequency for AES encrypted x16		50	50	50	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration		3	3	3	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK.		±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time		2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time		2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave CCLK frequency		100	100	100	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time		2.5	2.5	2.5	ns, Min
T_{EMCCKH}	External master CCLK High time		2.5	2.5	2.5	ns, Min
F_{EMCCK}	External master CCLK frequency		100	100	100	MHz, Max
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2)		100.00	100.00	100.00	MHz, Max

Date	Version	Description
08/03/2012	1.5	Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 12 and Note 13. Updated parameters in Table 3. Added Table 4 and Table 5. Updated the values for in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11. Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.2 speed specifications throughout the document with appropriate changes to Table 15 and Table 16 including production release of the XC7VX485T in the -2 and -1 speed designations. Added notes and specifications to Table 18. Updated the IOB Pad Input/Output/3-State discussion and changed Table 21 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 28. Rearranged Table 51 including moving some parameters to Table 1. Added Table 56. Updated Table 57. In Table 59, updated SJ Jitter Tolerance with Stressed Eye section, page 48 and Note 8. Added Note 1, Note 2, and Note 3 to Table 62. Added Note 1 and Note 2 to Table 63, and line rate ranges. Updated Table 64 including adding Note 1. Updated Table 65 including adding Note 1. In Table 82 updated Note 1 and added Note 4. In Table 83, updated T_{POR} and F_{EMCCK}.
09/20/2012	1.6	Removed the XC7V1500T device from data sheet. In Table 2, revised V_{CCINT} and V_{CCBRAM} and added Note 3. Updated some of the values in Table 7. Revised Table 15 and Table 16 to include production release of the XC7V585T in the -2 and -1 speed designations. Added values for the XC7V585T in Table 50. Updated Note 2 in Table 58.
09/26/2012	1.7	Revised Table 15 and Table 16 to include production release of the XC7VX485T in the -3 speed designation.
10/19/2012	1.8	Revised Table 15 and Table 16 to include production release of the XC7VX485T in the -2L (1.0V) speed designation. Removed -2L (0.9V) speed specifications from data sheet, this change includes edits to V_{CCINT} and V_{CCBRAM} in Table 2, editing Note 1 and removing Note 2 in Table 53. Also in Table 53, updated the F_{GTXMAX}, $F_{GTXQRANGE1}$, and $F_{GQPLLRANGE1}$ specification for -1 speed grade from 6.6 Gb/s to 8.0 Gb/s. Edited Note 4 in Table 57 and Note 3 in Table 72.
12/12/2012	1.9	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.3 speed specifications throughout the document. Revised Table 15 and Table 16 to include production release of the XC7V585T in the -3 and -2L(1.0V) speed designations. Updated the notes in Table 50. Updated GTH Transceiver Specifications including removal of GTH Transceiver DC Characteristics section (use the XPE (download at http://www.xilinx.com/power). Updated Table 68 and added Table 71, Table 73, and Table 74. Removed Note 4 from Table 82.
12/24/2012	1.10	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.4 and Vivado 2012.4 speed specifications throughout the document. Revised the XC7V2000T in the -1 and -2 speed designations Table 15 to preliminary. Added the GTH Transceiver Protocol Jitter Characteristics section. Updated T_{TCKTDO} and added Internal Configuration Access Port section to Table 83.
01/31/2013	1.11	Added Note 2 to Table 2. Revised Table 15 and Table 16 to include production release of the XC7V2000T in the -1 and -2 speed specifications. Updated Note 1 in Table 35. Updated the notes in Table 37, Table 40 through Table 43, Table 46, and Table 47. In Table 66, updated D_{VPPIN}. In Table 67, updated V_{IDIFF}. Removed T_{LOCK} and T_{PHASE} from Table 70. Updated T_{DLOCK} in Table 71.
03/07/2013	1.12	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.5 and Vivado 2013.1 speed specifications throughout the document. Revised Table 15 and Table 16 to include production release of the XC7VX690T. Revised D_{VPPOUT} in Table 66. Updated values in Table 67 and Table 74. Removed Note 1 from Table 68. Updated MMCM_F_{PFDMAX} in Table 38 and PLL_F_{PFDMAX} in Table 39. Added skew values to Table 50.