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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	32200
Number of Logic Elements/Cells	412160
Total RAM Bits	32440320
Number of I/O	350
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1158-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx415t-l2ffg1158e

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX/GTH transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to $0.3 \times T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to $0.3 \times T_{VCCINT}$ (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: SelectIO DC Input and Output Levels⁽¹⁾⁽²⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8	-8
HSTL_I_12	-0.300	$V_{REF} - 0.080$	$V_{REF} + 0.080$	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	6.3	-6.3
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8	-8
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16	-16
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16	-16
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% V_{CCO}	80% V_{CCO}	0.1	-0.1
LVC MOS12	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS15, LVDCI_15	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVC MOS18, LVDCI_18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS25	-0.300	0.700	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 6	Note 6
LVC MOS33	-0.300	0.800	2.000	3.450	0.400	$V_{CCO} - 0.400$	Note 6	Note 6
LV TTL	-0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	-0.300	20% V_{CCO}	80% V_{CCO}	$V_{CCO} + 0.300$	10% V_{CCO}	90% V_{CCO}	0.1	-0.1
PCI33_3	-0.400	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.500$	10% V_{CCO}	90% V_{CCO}	1.5	-0.5
SSTL12	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	14.25	-14.25
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.0	-13.0
SSTL135_R	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.9	-8.9
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.0	-13.0
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.9	-8.9
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8	-8
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.4	-13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)).

LVDS DC Specifications (LVDS_25)

The LVDS standard is available in the HR I/O banks.

Table 12: LVDS_25 DC Specifications⁽¹⁾

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks.

Table 13: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		1.710	1.800	1.890	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ± 350 mV	0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-7 T and XT devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 12](#). In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 17: Networking Applications Interface Performances

Description	I/O Bank Type	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS receiver (SPI-4.2) ⁽¹⁾	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and **Table 20** (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVTTTL_S4	1.31	1.42	1.64	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVTTTL_S8	1.31	1.42	1.64	3.50	3.64	3.73	4.26	4.50	4.72	ns
LVTTTL_S12	1.31	1.42	1.64	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVTTTL_S16	1.31	1.42	1.64	3.03	3.17	3.26	3.79	4.03	4.25	ns
LVTTTL_S24	1.31	1.42	1.64	3.25	3.39	3.48	4.01	4.25	4.47	ns
LVTTTL_F4	1.31	1.42	1.64	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVTTTL_F8	1.31	1.42	1.64	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVTTTL_F12	1.31	1.42	1.64	2.69	2.82	2.92	3.45	3.68	3.91	ns
LVTTTL_F16	1.31	1.42	1.64	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVTTTL_F24	1.31	1.42	1.64	2.41	2.64	2.89	3.17	3.50	3.88	ns
LVDS_25 ⁽¹⁾	0.64	0.68	0.80	1.36	1.47	1.55	2.12	2.33	2.54	ns
MINI_LVDS_25	0.68	0.70	0.79	1.36	1.47	1.55	2.12	2.33	2.54	ns
BLVDS_25 ⁽¹⁾	0.65	0.69	0.80	1.83	2.02	2.20	2.59	2.88	3.19	ns
RSDS_25 (point to point) ⁽¹⁾	0.63	0.68	0.79	1.36	1.48	1.55	2.12	2.34	2.54	ns
PPDS_25 ⁽¹⁾	0.65	0.69	0.80	1.36	1.49	1.58	2.12	2.35	2.57	ns
TMDS_33 ⁽¹⁾	0.72	0.76	0.86	1.43	1.54	1.60	2.19	2.40	2.59	ns
PCI33_3 ⁽¹⁾	1.28	1.41	1.65	2.71	3.08	3.52	3.47	3.94	4.51	ns
HSUL_12	0.63	0.64	0.71	1.77	1.90	2.00	2.53	2.76	2.99	ns
DIFF_HSUL_12	0.58	0.61	0.70	1.55	1.68	1.78	2.31	2.54	2.77	ns
HSTL_I_S	0.61	0.64	0.73	1.55	1.69	1.80	2.31	2.55	2.79	ns
HSTL_II_S	0.61	0.64	0.73	1.21	1.34	1.43	1.97	2.20	2.42	ns
HSTL_I_18_S	0.64	0.67	0.76	1.28	1.39	1.45	2.04	2.25	2.44	ns
HSTL_II_18_S	0.64	0.67	0.76	1.18	1.31	1.40	1.94	2.17	2.39	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	1.42	1.54	1.61	2.18	2.40	2.60	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	1.15	1.24	1.27	1.91	2.10	2.26	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	1.27	1.38	1.43	2.03	2.24	2.42	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	1.14	1.23	1.26	1.90	2.09	2.25	ns
HSTL_I_F	0.61	0.64	0.73	1.10	1.19	1.23	1.86	2.05	2.22	ns

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
HSTL_II_F	0.61	0.64	0.73	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_I_18_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_II_18_F	0.64	0.67	0.76	1.03	1.14	1.23	1.79	2.00	2.22	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	1.09	1.18	1.22	1.85	2.04	2.21	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	1.02	1.11	1.14	1.78	1.97	2.13	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	1.08	1.17	1.21	1.84	2.03	2.20	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	1.01	1.10	1.13	1.77	1.96	2.12	ns
LVC MOS33_S4	1.31	1.40	1.60	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVC MOS33_S8	1.31	1.40	1.60	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVC MOS33_S12	1.31	1.40	1.60	3.05	3.18	3.28	3.81	4.04	4.27	ns
LVC MOS33_S16	1.31	1.40	1.60	3.06	3.43	3.88	3.82	4.29	4.87	ns
LVC MOS33_F4	1.31	1.40	1.60	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVC MOS33_F8	1.31	1.40	1.60	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVC MOS33_F12	1.31	1.40	1.60	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVC MOS33_F16	1.31	1.40	1.60	2.44	2.69	2.96	3.20	3.55	3.95	ns
LVC MOS25_S4	1.08	1.16	1.32	3.08	3.22	3.31	3.84	4.08	4.30	ns
LVC MOS25_S8	1.08	1.16	1.32	2.85	2.98	3.07	3.61	3.84	4.06	ns
LVC MOS25_S12	1.08	1.16	1.32	2.44	2.57	2.67	3.20	3.43	3.66	ns
LVC MOS25_S16	1.08	1.16	1.32	2.79	2.92	3.01	3.55	3.78	4.00	ns
LVC MOS25_F4	1.08	1.16	1.32	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVC MOS25_F8	1.08	1.16	1.32	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS25_F12	1.08	1.16	1.32	2.15	2.29	2.52	2.91	3.15	3.51	ns
LVC MOS25_F16	1.08	1.16	1.32	1.92	2.17	2.45	2.68	3.03	3.44	ns
LVC MOS18_S4	0.64	0.66	0.74	1.55	1.68	1.78	2.31	2.54	2.77	ns
LVC MOS18_S8	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS18_S12	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVC MOS18_S16	0.64	0.66	0.74	1.49	1.62	1.72	2.25	2.48	2.71	ns
LVC MOS18_S24 ⁽¹⁾	0.64	0.66	0.74	1.74	1.92	2.08	2.50	2.78	3.07	ns
LVC MOS18_F4	0.64	0.66	0.74	1.38	1.51	1.61	2.14	2.37	2.60	ns
LVC MOS18_F8	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVC MOS18_F12	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVC MOS18_F16	0.64	0.66	0.74	1.52	1.68	1.81	2.28	2.54	2.80	ns
LVC MOS18_F24 ⁽¹⁾	0.64	0.66	0.74	1.34	1.46	1.55	2.10	2.32	2.54	ns
LVC MOS15_S4	0.66	0.69	0.81	1.86	2.00	2.09	2.62	2.86	3.08	ns
LVC MOS15_S8	0.66	0.69	0.81	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVC MOS15_S12	0.66	0.69	0.81	1.83	2.03	2.23	2.59	2.89	3.22	ns
LVC MOS15_S16	0.66	0.69	0.81	1.76	1.95	2.13	2.52	2.81	3.12	ns

Table 23: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{ODCK} /T _{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.45/−0.13	0.50/−0.13	0.58/−0.13	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T _{OSRCK} /T _{OCKSR}	SR pin setup/hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.49/−0.16	0.56/−0.16	0.68/−0.16	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Combinatorial					
T _{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	ns
Sequential Delays					
T _{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	ns
T _{RQ_OLOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	ns
T _{GSRQ_OLOGICE2}	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
T _{RQ_OLOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	ns
T _{GSRQ_OLOGICE3}	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
T _{RPW_OLOGICE2}	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	ns, Min
T _{RPW_OLOGICE3}	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	ns, Min

Output Serializer/Deserializer Switching Characteristics

Table 25: OSERDES Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{OSDCK_D} /T _{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input setup/hold with respect to CLK	0.49/−0.15	0.56/−0.15	0.68/−0.15	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input setup/hold with respect to CLKDIV	0.27/−0.15	0.30/−0.15	0.34/−0.15	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T _{OSCCK_S}	SR (Reset) input setup with respect to CLKDIV	0.41	0.46	0.75	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Sequential Delays					
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	ns
Combinatorial					
T _{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

CLB Distributed RAM Switching Characteristics (SLICEM Only)*Table 29: CLB Distributed RAM Switching Characteristics*

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T _{SHCKO} ⁽¹⁾	Clock to A – B outputs	0.68	0.70	0.85	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	ns, Min
T _{CECK_LRAM} /T _{CKCE_LRAM}	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	ns, Min
Clock CLK					
T _{MPW}	Minimum pulse width	0.68	0.77	0.91	ns, Min
T _{MCP}	Minimum clock period	1.35	1.54	1.82	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)*Table 30: CLB Shift Register Switching Characteristics*

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Sequential Delays					
T _{REG}	Clock to A – D outputs	0.96	0.98	1.20	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK					
T _{WS_SHFREG} /T _{WH_SHFREG}	WE input	0.26/0.09	0.27/0.09	0.33/0.09	ns, Min
T _{CECK_SHFREG} /T _{CKCE_SHFREG}	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	ns, Min
T _{DS_SHFREG} /T _{DH_SHFREG}	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	ns, Min
Clock CLK					
T _{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	ns, Min

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 51 summarizes the DC specifications of the GTX transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

Table 51: GTX Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
V _{CMOUTDC}	DC common mode output voltage.	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–200	–	$V_{MGTAVTT}$	mV
V _{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–	$2/3 V_{MGTAVTT}$	–	mV
R _{IN}	Differential input resistance		–	100	–	Ω
C _{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476), and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

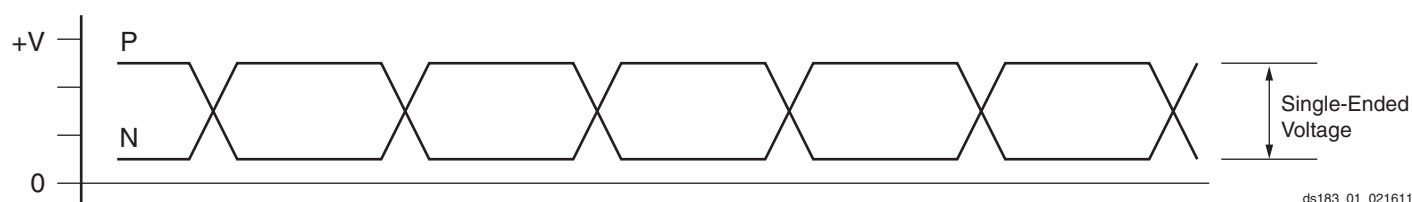


Figure 1: Single-Ended Peak-to-Peak Voltage

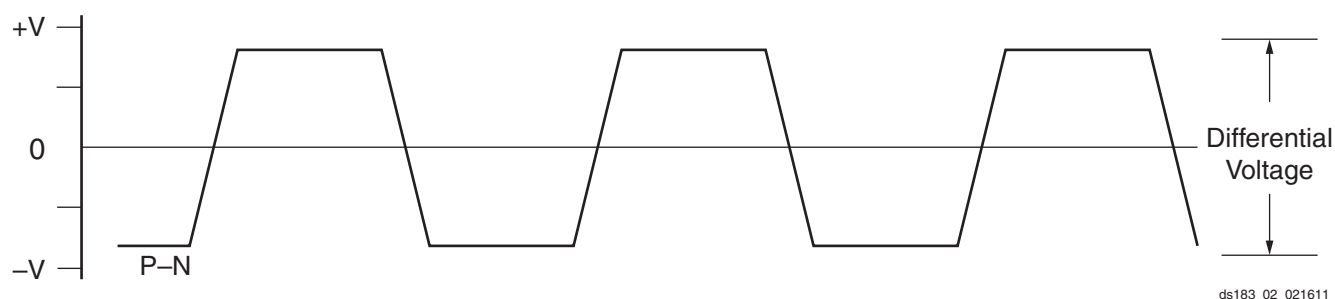


Figure 2: Differential Peak-to-Peak Voltage

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further details.

Table 52: GTX Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further information.

Table 53: GTX Transceiver Performance

Symbol	Description	Output Divider	Speed Grade			Units
			-3/-2G	-2/-2L	-1 ⁽¹⁾	
F _{GTXMAX} ⁽²⁾	Maximum GTX transceiver data rate		12.5	10.3125	8.0	Gb/s
F _{GTXMIN} ⁽²⁾	Minimum GTX transceiver data rate		0.500	0.500	0.500	Gb/s
F _{GTXCRANGE}	CPLL line rate range	1	3.2–6.6			Gb/s
		2	1.6–3.3			Gb/s
		4	0.8–1.65			Gb/s
		8	0.5–0.825			Gb/s
		16	N/A			Gb/s
F _{GTXQRANGE1}	QPLL line rate range 1	1	5.93–8.0	5.93–8.0	5.93–8.0	Gb/s
		2	2.965–4.0	2.965–4.0	2.965–4.0	Gb/s
		4	1.4825–2.0	1.4825–2.0	1.4825–2.0	Gb/s
		8	0.74125–1.0	0.74125–1.0	0.74125–1.0	Gb/s
		16	N/A	N/A	N/A	Gb/s
F _{GTXQRANGE2}	QPLL line rate range 2 ⁽³⁾	1	9.8–12.5	9.8–10.3125	N/A	Gb/s
		2	4.9–6.25	4.9–5.15625	N/A	Gb/s
		4	2.45–3.125	2.45–2.578125	N/A	Gb/s
		8	1.225–1.5625	1.225–1.2890625	N/A	Gb/s
		16	0.6125–0.78125	0.6125–0.64453125	N/A	Gb/s
F _{GCPLLRANGE}	GTX transceiver CPLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	GHz
F _{GQPLLRange1}	GTX transceiver QPLL frequency range 1		5.93–8.0	5.93–8.0	5.93–8.0	GHz
F _{GQPLLRange2}	GTX transceiver QPLL frequency range 2		9.8–12.5	9.8–10.3125	N/A	GHz

Notes:

- The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), requires a 4-byte internal data width for operation above 3.8 Gb/s.
- Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
- For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3/-2G	-2/-2L	-1	
F _{GTXDRPCLK}	GTXDRPCLK maximum frequency	175.01	175.01	156.25	MHz

Table 59: GTX Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTXRX}	Serial data rate	RX oversampler not enabled	0.500	–	F _{GTXMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm
RX _{RL}	Run length (CID)		–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.3	–	–	UI
JT_SJ _{11.18}	Sinusoidal jitter (QPLL) ⁽³⁾	11.18 Gb/s	0.3	–	–	UI
JT_SJ _{10.32}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.95}	Sinusoidal jitter (QPLL) ⁽³⁾	9.95 Gb/s	0.3	–	–	UI
JT_SJ _{9.8}	Sinusoidal jitter (QPLL) ⁽³⁾	9.8 Gb/s	0.3	–	–	UI
JT_SJ _{8.0}	Sinusoidal jitter (QPLL) ⁽³⁾	8.0 Gb/s	0.44	–	–	UI
JT_SJ _{6.6_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	6.6 Gb/s	0.48	–	–	UI
JT_SJ _{6.6_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal jitter (CPLL) ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{3.2L}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁵⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁷⁾	0.5	–	–	UI
JT_SJ ₅₀₀	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
JT_TJSE _{6.6}		6.6 Gb/s	0.70	–	–	UI
JT_SJSE _{3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.1	–	–	UI
JT_SJSE _{6.6}		6.6 Gb/s	0.1	–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of $1e^{-12}$.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the 7 Series FPGAs GTX/GTH Transceiver User Guide ([UG476](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: Gigabit Ethernet Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: XAUI Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: PCI Express Protocol Characteristics (GTX Transceivers)⁽¹⁾

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 ⁽³⁾	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 63: CEI-6G and CEI-11G Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter ⁽²⁾	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽²⁾	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 64: SFP+ Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40 ⁽¹⁾	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40 ⁽¹⁾	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 65: CPRI Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see [Table 64](#).

Table 72: GTH Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3E/-2GE ⁽²⁾	-2(C&I)/-2LE ⁽²⁾	-1(C&I) ⁽³⁾	
F _{TXOUT}	TXUSERCLKOUT maximum frequency			412.500	412.500	312.500	MHz
F _{RXOUT}	RXUSERCLKOUT maximum frequency			412.500	412.500	312.500	MHz
F _{TXIN}	TXUSERCLKIN maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	409.375	353.125	265.625	MHz
F _{RXIN}	RXUSERCLKIN maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	409.375	353.125	265.625	MHz
F _{TXIN2}	TXUSERCLKIN2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	409.375	353.125	265.625	MHz
		64-bit	64-bit	204.688	176.563	132.813	MHz
F _{RXIN2}	RXUSERCLKIN2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	409.375	353.125	265.625	MHz
		64-bit	64-bit	204.688	176.563	132.813	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
2. For speed grades -3E, -2GE, -2C, -2I, and -2LE, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
3. For speed grade -1 (and when V_{CCINT} = 0.9V), a 16-bit data path can only be used for speeds less than 5.0 Gb/s.

Table 73: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	—	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	—	40	—	ps
T _{FTX}	TX fall time	80%–20%	—	40	—	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		—	—	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		—	—	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		—	—	140	ns
TJ _{13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	—	—	0.3	UI
DJ _{13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{12.5}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	—	—	0.28	UI
DJ _{12.5}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{11.3}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	—	—	0.28	UI
DJ _{11.3}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	—	—	0.28	UI
DJ _{10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	—	—	0.33	UI
DJ _{10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		—	—	0.17	UI
TJ _{9.953}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	—	—	0.28	UI
DJ _{9.953}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{9.8}	Total jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	—	—	0.28	UI
DJ _{9.8}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{8.0_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	—	—	0.28	UI
DJ _{8.0_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI

Table 78: CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter ⁽²⁾	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽²⁾	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 79: SFP+ Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40 ⁽¹⁾	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40 ⁽¹⁾	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 80: CPRI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 79.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 81: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	500.00	500.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz

XADC Specifications

Table 82: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, T _j = −40°C to 100°C, Typical values at T _j =+40°C						
ADC Accuracy ⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±6	LSBs
Gain Error		Gain calibration disabled	–	–	±0.5	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio ⁽²⁾	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion ⁽²⁾	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	–	70	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs ⁽³⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T _j = −40°C to 100°C.	–	–	±4	°C
		T _j = −55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −40°C to +100°C	–	–	±1	%
		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −55°C to +125°C	–	–	±2	%
Conversion Rate ⁽⁴⁾						
Conversion Time - Continuous	t _{CONV}	Number of ADCCLK cycles	26	–	32	cycle
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	cycle
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%