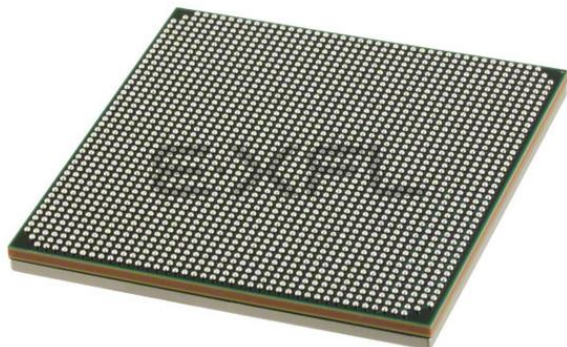




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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### Details

|                                |                                                                                                                                               |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Active                                                                                                                                        |
| Number of LABs/CLBs            | 37950                                                                                                                                         |
| Number of Logic Elements/Cells | 485760                                                                                                                                        |
| Total RAM Bits                 | 37969920                                                                                                                                      |
| Number of I/O                  | 700                                                                                                                                           |
| Number of Gates                | -                                                                                                                                             |
| Voltage - Supply               | 0.97V ~ 1.03V                                                                                                                                 |
| Mounting Type                  | Surface Mount                                                                                                                                 |
| Operating Temperature          | 0°C ~ 85°C (TJ)                                                                                                                               |
| Package / Case                 | 1924-BBGA, FCBGA                                                                                                                              |
| Supplier Device Package        | 1930-FCBGA (45x45)                                                                                                                            |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/xilinx/xc7vx485t-1ffg1930c">https://www.e-xfl.com/product-detail/xilinx/xc7vx485t-1ffg1930c</a> |

Table 1: Absolute Maximum Ratings<sup>(1)</sup> (Cont'd)

| Symbol             | Description                                                                                  | Min  | Max  | Units |
|--------------------|----------------------------------------------------------------------------------------------|------|------|-------|
| $V_{MGTAVTTRCAL}$  | Analog supply voltage for the resistor calibration circuit of the GTX/GTH transceiver column | -0.5 | 1.32 | V     |
| $V_{IN}$           | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage                          | -0.5 | 1.26 | V     |
| $I_{DCIN}$         | DC input current for receiver input pins DC coupled $V_{MGTAVTT} = 1.2V$                     | –    | 14   | mA    |
| $I_{DCOUT}$        | DC output current for transmitter pins DC coupled $V_{MGTAVTT} = 1.2V$                       | –    | 14   | mA    |
| <b>XADC</b>        |                                                                                              |      |      |       |
| $V_{CCADC}$        | XADC supply relative to GNDADC                                                               | -0.5 | 2.0  | V     |
| $V_{REFP}$         | XADC reference input relative to GNDADC                                                      | -0.5 | 2.0  | V     |
| <b>Temperature</b> |                                                                                              |      |      |       |
| $T_{STG}$          | Storage temperature (ambient)                                                                | -65  | 150  | °C    |
| $T_{SOL}$          | Maximum soldering temperature for Pb/Sn component bodies <sup>(6)</sup>                      | –    | +220 | °C    |
|                    | Maximum soldering temperature for Pb-free component bodies <sup>(6)</sup>                    | –    | +260 | °C    |
| $T_j$              | Maximum junction temperature <sup>(6)</sup>                                                  | –    | +125 | °C    |

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- The lower absolute voltage specification always applies.
- For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)).
- The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see [Table 4](#) and [Table 5](#).
- See [Table 10](#) for TMD5\_33 specifications.
- For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* ([UG475](#)).

Table 2: Recommended Operating Conditions<sup>(1)(2)</sup>

| Symbol              | Description                                                                                                                       | Min   | Typ  | Max             | Units |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------|-------|------|-----------------|-------|
| <b>FPGA Logic</b>   |                                                                                                                                   |       |      |                 |       |
| $V_{CCINT}^{(3)}$   | Internal supply voltage                                                                                                           | 0.97  | 1.00 | 1.03            | V     |
|                     | Internal supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical <sup>(4)</sup> .  | 0.87  | 0.90 | 0.93            | V     |
| $V_{CCBRAM}^{(3)}$  | Block RAM supply voltage                                                                                                          | 0.97  | 1.00 | 1.03            | V     |
|                     | Block RAM supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical <sup>(4)</sup> . | 0.87  | 0.90 | 1.03            | V     |
| $V_{CCAUX}$         | Auxiliary supply voltage                                                                                                          | 1.71  | 1.80 | 1.89            | V     |
| $V_{CCO}^{(5)(6)}$  | Supply voltage for 3.3V HR I/O banks                                                                                              | 1.14  | –    | 3.465           | V     |
|                     | Supply voltage for 1.8V HP I/O banks                                                                                              | 1.14  | –    | 1.89            | V     |
| $V_{CCAUX\_IO}$     | Auxiliary supply voltage when set to 1.8V                                                                                         | 1.71  | 1.80 | 1.89            | V     |
|                     | Auxiliary supply voltage when set to 2.0V                                                                                         | 1.94  | 2.00 | 2.06            | V     |
| $V_{IN}^{(7)}$      | I/O input voltage                                                                                                                 | -0.20 | –    | $V_{CCO} + 0.2$ | V     |
|                     | I/O input voltage (when $V_{CCO} = 3.3V$ ) for $V_{REF}$ and differential I/O standards except TMD5_33 <sup>(8)</sup>             | -0.20 | –    | 2.625           | V     |
| $I_{IN}^{(9)}$      | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.                              | –     | –    | 10              | mA    |
| $V_{CCBATT}^{(10)}$ | Battery voltage                                                                                                                   | 1.0   | –    | 1.89            | V     |

Table 2: Recommended Operating Conditions<sup>(1)(2)</sup> (Cont'd)

| Symbol                          | Description                                                                                                   | Min  | Typ  | Max  | Units |
|---------------------------------|---------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| <b>GTX and GTH Transceivers</b> |                                                                                                               |      |      |      |       |
| $V_{MGTAVCC}^{(11)}$            | Analog supply voltage for the GTX/GTH transceiver QPLL frequency range $\leq 10.3125$ GHz <sup>(12)(13)</sup> | 0.97 | 1.0  | 1.08 | V     |
|                                 | Analog supply voltage for the GTX/GTH transceiver QPLL frequency range $> 10.3125$ GHz                        | 1.02 | 1.05 | 1.08 | V     |
| $V_{MGTAVTT}^{(11)}$            | Analog supply voltage for the GTX/GTH transmitter and receiver termination circuits                           | 1.17 | 1.2  | 1.23 | V     |
| $V_{MGTVCCAUX}^{(11)}$          | Auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers                                          | 1.75 | 1.80 | 1.85 | V     |
| $V_{MGTAVTTRCAL}^{(11)}$        | Analog supply voltage for the resistor calibration circuit of the GTX/GTH transceiver column                  | 1.17 | 1.2  | 1.23 | V     |
| <b>XADC</b>                     |                                                                                                               |      |      |      |       |
| $V_{CCADC}$                     | XADC supply relative to GNDADC                                                                                | 1.71 | 1.80 | 1.89 | V     |
| $V_{REFP}$                      | Externally supplied reference voltage                                                                         | 1.20 | 1.25 | 1.30 | V     |
| <b>Temperature</b>              |                                                                                                               |      |      |      |       |
| $T_j$                           | Junction temperature operating range for commercial (C) temperature devices                                   | 0    | –    | 85   | °C    |
|                                 | Junction temperature operating range for extended (E) temperature devices                                     | 0    | –    | 100  | °C    |
|                                 | Junction temperature operating range for industrial (I) temperature devices                                   | –40  | –    | 100  | °C    |

**Notes:**

- All voltages are relative to ground.
- For the design of the power distribution system, consult the *7 Series FPGAs PCB Design and Pin Planning Guide* (UG483).
- $V_{CCINT}$  and  $V_{CCBRAM}$  should be connected to the same supply.
- For more information on the VID bit see the *Lowering Power using the Voltage Identification Bit* application note (XAPP555).
- Configuration data is retained even if  $V_{CCO}$  drops to 0V.
- Includes  $V_{CCO}$  of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
- The lower absolute voltage specification always applies.
- See Table 10 for TMD5\_33 specifications.
- A total of 200 mA per bank should not be exceeded.
- $V_{CCBATT}$  is required only when using bitstream encryption. If battery is not used, connect  $V_{CCBATT}$  to either ground or  $V_{CCAUX}$ .
- Each voltage listed requires the filter circuit described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476).
- For data rates  $\leq 10.3125$  Gb/s,  $V_{MGTAVCC}$  should be  $1.0V \pm 3\%$  for lower power consumption.
- For lower power consumption,  $V_{MGTAVCC}$  should be  $1.0V \pm 3\%$  over the entire CPLL frequency range.

Table 3: DC Characteristics Over Recommended Operating Conditions

| Symbol         | Description                                                                       | Min  | Typ <sup>(1)</sup> | Max | Units   |
|----------------|-----------------------------------------------------------------------------------|------|--------------------|-----|---------|
| $V_{DRINT}$    | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | –                  | –   | V       |
| $V_{DRI}$      | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 1.5  | –                  | –   | V       |
| $I_{REF}$      | $V_{REF}$ leakage current per pin                                                 | –    | –                  | 15  | $\mu A$ |
| $I_L$          | Input or output leakage current per pin (sample-tested)                           | –    | –                  | 15  | $\mu A$ |
| $C_{IN}^{(2)}$ | Die input capacitance at the pad                                                  | –    | –                  | 8   | pF      |
| $I_{RPU}$      | Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 3.3V$                    | 90   | –                  | 330 | $\mu A$ |
|                | Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 2.5V$                    | 68   | –                  | 250 | $\mu A$ |
|                | Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 1.8V$                    | 34   | –                  | 220 | $\mu A$ |
|                | Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 1.5V$                    | 23   | –                  | 150 | $\mu A$ |
|                | Pad pull-up (when selected) @ $V_{IN} = 0V$ , $V_{CCO} = 1.2V$                    | 12   | –                  | 120 | $\mu A$ |

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

| Symbol                        | Description                                                                                                                                                                 | Min | Typ <sup>(1)</sup> | Max | Units    |
|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------------|-----|----------|
| $I_{RPD}$                     | Pad pull-down (when selected) @ $V_{IN} = 3.3V$                                                                                                                             | 68  | –                  | 330 | $\mu A$  |
|                               | Pad pull-down (when selected) @ $V_{IN} = 1.8V$                                                                                                                             | 45  | –                  | 180 | $\mu A$  |
| $I_{CCADC}$                   | Analog supply current, analog circuits in powered up state                                                                                                                  | –   | –                  | 25  | mA       |
| $I_{BATT}$ <sup>(3)</sup>     | Battery supply current                                                                                                                                                      | –   | –                  | 150 | nA       |
| $R_{IN\_TERM}$ <sup>(4)</sup> | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices | 28  | 40                 | 55  | $\Omega$ |
|                               | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices | 35  | 50                 | 65  | $\Omega$ |
|                               | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices | 44  | 60                 | 83  | $\Omega$ |
| n                             | Temperature diode ideality factor                                                                                                                                           | –   | 1.010              | –   | –        |
| r                             | Temperature diode series resistance                                                                                                                                         | –   | 2                  | –   | $\Omega$ |

**Notes:**

- Typical values are specified at nominal voltage, 25°C.
- This measurement represents the die capacitance at the pad, not including the package.
- Maximum value specified for worst case process at 25°C.
- Termination resistance to a  $V_{CCO}/2$  level.

Table 4:  $V_{IN}$  Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks<sup>(1)</sup>

| AC Voltage Overshoot | % of UI @–40°C to 100°C | AC Voltage Undershoot | % of UI @–40°C to 100°C |
|----------------------|-------------------------|-----------------------|-------------------------|
| $V_{CCO} + 0.55$     | 100                     | –0.40                 | 100                     |
|                      |                         | –0.45                 | 61.7                    |
|                      |                         | –0.50                 | 25.8                    |
|                      |                         | –0.55                 | 11.0                    |
| $V_{CCO} + 0.60$     | 46.6                    | –0.60                 | 4.77                    |
| $V_{CCO} + 0.65$     | 21.2                    | –0.65                 | 2.10                    |
| $V_{CCO} + 0.70$     | 9.75                    | –0.70                 | 0.94                    |
| $V_{CCO} + 0.75$     | 4.55                    | –0.75                 | 0.43                    |
| $V_{CCO} + 0.80$     | 2.15                    | –0.80                 | 0.20                    |
| $V_{CCO} + 0.85$     | 1.02                    | –0.85                 | 0.09                    |
| $V_{CCO} + 0.90$     | 0.49                    | –0.90                 | 0.04                    |
| $V_{CCO} + 0.95$     | 0.24                    | –0.95                 | 0.02                    |

**Notes:**

- A total of 200 mA per bank should not be exceeded.

Table 10: Differential SelectIO DC Input and Output Levels

| I/O Standard | $V_{ICM}^{(1)}$ |        |             | $V_{ID}^{(2)}$ |        |        | $V_{OCM}^{(3)}$ |                 |                 | $V_{OD}^{(4)}$ |        |        |
|--------------|-----------------|--------|-------------|----------------|--------|--------|-----------------|-----------------|-----------------|----------------|--------|--------|
|              | V, Min          | V, Typ | V, Max      | V, Min         | V, Typ | V, Max | V, Min          | V, Typ          | V, Max          | V, Min         | V, Typ | V, Max |
| BLVDS_25     | 0.300           | 1.200  | 1.425       | 0.100          | —      | —      | —               | 1.250           | —               | Note 5         |        |        |
| MINI_LVDS_25 | 0.300           | 1.200  | $V_{CCAUX}$ | 0.200          | 0.400  | 0.600  | 1.000           | 1.200           | 1.400           | 0.300          | 0.450  | 0.600  |
| PPDS_25      | 0.200           | 0.900  | $V_{CCAUX}$ | 0.100          | 0.250  | 0.400  | 0.500           | 0.950           | 1.400           | 0.100          | 0.250  | 0.400  |
| RSDS_25      | 0.300           | 0.900  | 1.500       | 0.100          | 0.350  | 0.600  | 1.000           | 1.200           | 1.400           | 0.100          | 0.350  | 0.600  |
| TMDS_33      | 2.700           | 2.965  | 3.230       | 0.150          | 0.675  | 1.200  | $V_{CCO}-0.405$ | $V_{CCO}-0.300$ | $V_{CCO}-0.190$ | 0.400          | 0.600  | 0.800  |

**Notes:**

- $V_{ICM}$  is the input common mode voltage.
- $V_{ID}$  is the input differential voltage ( $Q - \bar{Q}$ ).
- $V_{OCM}$  is the output common mode voltage.
- $V_{OD}$  is the output differential voltage ( $Q - \bar{Q}$ ).
- $V_{OD}$  for BLVDS will vary significantly depending on topology and loading.
- LVDS\_25 is specified in Table 12.
- LVDS is specified in Table 13.

Table 11: Complementary Differential SelectIO DC Input and Output Levels

| I/O Standard    | $V_{ICM}^{(1)}$ |        |        | $V_{ID}^{(2)}$ |        | $V_{OL}^{(3)}$        | $V_{OH}^{(4)}$        | $I_{OL}$ | $I_{OH}$ |
|-----------------|-----------------|--------|--------|----------------|--------|-----------------------|-----------------------|----------|----------|
|                 | V, Min          | V, Typ | V, Max | V, Min         | V, Max | V, Max                | V, Min                | mA, Max  | mA, Min  |
| DIFF_HSTL_I     | 0.300           | 0.750  | 1.125  | 0.100          | —      | 0.400                 | $V_{CCO}-0.400$       | 8.00     | –8.00    |
| DIFF_HSTL_I_18  | 0.300           | 0.900  | 1.425  | 0.100          | —      | 0.400                 | $V_{CCO}-0.400$       | 8.00     | –8.00    |
| DIFF_HSTL_II    | 0.300           | 0.750  | 1.125  | 0.100          | —      | 0.400                 | $V_{CCO}-0.400$       | 16.00    | –16.00   |
| DIFF_HSTL_II_18 | 0.300           | 0.900  | 1.425  | 0.100          | —      | 0.400                 | $V_{CCO}-0.400$       | 16.00    | –16.00   |
| DIFF_HSUL_12    | 0.300           | 0.600  | 0.850  | 0.100          | —      | 20% $V_{CCO}$         | 80% $V_{CCO}$         | 0.100    | –0.100   |
| DIFF_MOBILE_DDR | 0.300           | 0.900  | 1.425  | 0.100          | —      | 10% $V_{CCO}$         | 90% $V_{CCO}$         | 0.100    | –0.100   |
| DIFF_SSTL12     | 0.300           | 0.600  | 0.850  | 0.100          | —      | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 14.25    | –14.25   |
| DIFF_SSTL135    | 0.300           | 0.675  | 1.000  | 0.100          | —      | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 13.0     | –13.0    |
| DIFF_SSTL135_R  | 0.300           | 0.675  | 1.000  | 0.100          | —      | $(V_{CCO}/2) - 0.150$ | $(V_{CCO}/2) + 0.150$ | 8.9      | –8.9     |
| DIFF_SSTL15     | 0.300           | 0.750  | 1.125  | 0.100          | —      | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 13.0     | –13.0    |
| DIFF_SSTL15_R   | 0.300           | 0.750  | 1.125  | 0.100          | —      | $(V_{CCO}/2) - 0.175$ | $(V_{CCO}/2) + 0.175$ | 8.9      | –8.9     |
| DIFF_SSTL18_I   | 0.300           | 0.900  | 1.425  | 0.100          | —      | $(V_{CCO}/2) - 0.470$ | $(V_{CCO}/2) + 0.470$ | 8.00     | –8.00    |
| DIFF_SSTL18_II  | 0.300           | 0.900  | 1.425  | 0.100          | —      | $(V_{CCO}/2) - 0.600$ | $(V_{CCO}/2) + 0.600$ | 13.4     | –13.4    |

**Notes:**

- $V_{ICM}$  is the input common mode voltage.
- $V_{ID}$  is the input differential voltage ( $Q - \bar{Q}$ ).
- $V_{OL}$  is the single-ended low-output voltage.
- $V_{OH}$  is the single-ended high-output voltage.

## IOB Pad Input/Output/3-State

**Table 19** (3.3V high-range IOB (HR)) and **Table 20** (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{IOPI}$  is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$  is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than  $T_{IOTP}$  when the DCITERMDISABLE pin is used. In HR I/O banks, the IN\_TERM termination turn-on time is always faster than  $T_{IOTP}$  when the INTERMDISABLE pin is used.

**Table 19: 3.3V IOB High Range (HR) Switching Characteristics**

| I/O Standard                            | T <sub>IOPI</sub> |            |      | T <sub>IOOP</sub> |            |      | T <sub>IOTP</sub> |            |      | Units |
|-----------------------------------------|-------------------|------------|------|-------------------|------------|------|-------------------|------------|------|-------|
|                                         | Speed Grade       |            |      | Speed Grade       |            |      | Speed Grade       |            |      |       |
|                                         | -3                | -2/-2L/-2G | -1   | -3                | -2/-2L/-2G | -1   | -3                | -2/-2L/-2G | -1   |       |
| LVTTTL_S4                               | 1.31              | 1.42       | 1.64 | 3.77              | 3.90       | 4.00 | 4.53              | 4.76       | 4.99 | ns    |
| LVTTTL_S8                               | 1.31              | 1.42       | 1.64 | 3.50              | 3.64       | 3.73 | 4.26              | 4.50       | 4.72 | ns    |
| LVTTTL_S12                              | 1.31              | 1.42       | 1.64 | 3.49              | 3.62       | 3.72 | 4.25              | 4.48       | 4.71 | ns    |
| LVTTTL_S16                              | 1.31              | 1.42       | 1.64 | 3.03              | 3.17       | 3.26 | 3.79              | 4.03       | 4.25 | ns    |
| LVTTTL_S24                              | 1.31              | 1.42       | 1.64 | 3.25              | 3.39       | 3.48 | 4.01              | 4.25       | 4.47 | ns    |
| LVTTTL_F4                               | 1.31              | 1.42       | 1.64 | 3.22              | 3.36       | 3.45 | 3.98              | 4.22       | 4.44 | ns    |
| LVTTTL_F8                               | 1.31              | 1.42       | 1.64 | 2.71              | 2.84       | 2.93 | 3.47              | 3.70       | 3.92 | ns    |
| LVTTTL_F12                              | 1.31              | 1.42       | 1.64 | 2.69              | 2.82       | 2.92 | 3.45              | 3.68       | 3.91 | ns    |
| LVTTTL_F16                              | 1.31              | 1.42       | 1.64 | 2.57              | 2.85       | 3.15 | 3.33              | 3.71       | 4.14 | ns    |
| LVTTTL_F24                              | 1.31              | 1.42       | 1.64 | 2.41              | 2.64       | 2.89 | 3.17              | 3.50       | 3.88 | ns    |
| LVDS_25 <sup>(1)</sup>                  | 0.64              | 0.68       | 0.80 | 1.36              | 1.47       | 1.55 | 2.12              | 2.33       | 2.54 | ns    |
| MINI_LVDS_25                            | 0.68              | 0.70       | 0.79 | 1.36              | 1.47       | 1.55 | 2.12              | 2.33       | 2.54 | ns    |
| BLVDS_25 <sup>(1)</sup>                 | 0.65              | 0.69       | 0.80 | 1.83              | 2.02       | 2.20 | 2.59              | 2.88       | 3.19 | ns    |
| RSDS_25 (point to point) <sup>(1)</sup> | 0.63              | 0.68       | 0.79 | 1.36              | 1.48       | 1.55 | 2.12              | 2.34       | 2.54 | ns    |
| PPDS_25 <sup>(1)</sup>                  | 0.65              | 0.69       | 0.80 | 1.36              | 1.49       | 1.58 | 2.12              | 2.35       | 2.57 | ns    |
| TMDS_33 <sup>(1)</sup>                  | 0.72              | 0.76       | 0.86 | 1.43              | 1.54       | 1.60 | 2.19              | 2.40       | 2.59 | ns    |
| PCI33_3 <sup>(1)</sup>                  | 1.28              | 1.41       | 1.65 | 2.71              | 3.08       | 3.52 | 3.47              | 3.94       | 4.51 | ns    |
| HSUL_12                                 | 0.63              | 0.64       | 0.71 | 1.77              | 1.90       | 2.00 | 2.53              | 2.76       | 2.99 | ns    |
| DIFF_HSUL_12                            | 0.58              | 0.61       | 0.70 | 1.55              | 1.68       | 1.78 | 2.31              | 2.54       | 2.77 | ns    |
| HSTL_I_S                                | 0.61              | 0.64       | 0.73 | 1.55              | 1.69       | 1.80 | 2.31              | 2.55       | 2.79 | ns    |
| HSTL_II_S                               | 0.61              | 0.64       | 0.73 | 1.21              | 1.34       | 1.43 | 1.97              | 2.20       | 2.42 | ns    |
| HSTL_I_18_S                             | 0.64              | 0.67       | 0.76 | 1.28              | 1.39       | 1.45 | 2.04              | 2.25       | 2.44 | ns    |
| HSTL_II_18_S                            | 0.64              | 0.67       | 0.76 | 1.18              | 1.31       | 1.40 | 1.94              | 2.17       | 2.39 | ns    |
| DIFF_HSTL_I_S                           | 0.63              | 0.67       | 0.77 | 1.42              | 1.54       | 1.61 | 2.18              | 2.40       | 2.60 | ns    |
| DIFF_HSTL_II_S                          | 0.63              | 0.67       | 0.77 | 1.15              | 1.24       | 1.27 | 1.91              | 2.10       | 2.26 | ns    |
| DIFF_HSTL_I_18_S                        | 0.65              | 0.69       | 0.78 | 1.27              | 1.38       | 1.43 | 2.03              | 2.24       | 2.42 | ns    |
| DIFF_HSTL_II_18_S                       | 0.65              | 0.69       | 0.78 | 1.14              | 1.23       | 1.26 | 1.90              | 2.09       | 2.25 | ns    |
| HSTL_I_F                                | 0.61              | 0.64       | 0.73 | 1.10              | 1.19       | 1.23 | 1.86              | 2.05       | 2.22 | ns    |

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

| I/O Standard                 | T <sub>IOPI</sub> |            |      | T <sub>IOOP</sub> |            |      | T <sub>IOTP</sub> |            |      | Units |
|------------------------------|-------------------|------------|------|-------------------|------------|------|-------------------|------------|------|-------|
|                              | Speed Grade       |            |      | Speed Grade       |            |      | Speed Grade       |            |      |       |
|                              | -3                | -2/-2L/-2G | -1   | -3                | -2/-2L/-2G | -1   | -3                | -2/-2L/-2G | -1   |       |
| LVC MOS15_F4                 | 0.66              | 0.69       | 0.81 | 1.63              | 1.76       | 1.86 | 2.39              | 2.62       | 2.85 | ns    |
| LVC MOS15_F8                 | 0.66              | 0.69       | 0.81 | 1.79              | 1.99       | 2.18 | 2.55              | 2.85       | 3.17 | ns    |
| LVC MOS15_F12                | 0.66              | 0.69       | 0.81 | 1.40              | 1.54       | 1.65 | 2.16              | 2.40       | 2.64 | ns    |
| LVC MOS15_F16                | 0.66              | 0.69       | 0.81 | 1.37              | 1.51       | 1.61 | 2.13              | 2.37       | 2.60 | ns    |
| LVC MOS12_S4                 | 0.88              | 0.91       | 1.00 | 2.53              | 2.67       | 2.76 | 3.29              | 3.53       | 3.75 | ns    |
| LVC MOS12_S8                 | 0.88              | 0.91       | 1.00 | 2.05              | 2.18       | 2.28 | 2.81              | 3.04       | 3.27 | ns    |
| LVC MOS12_S12 <sup>(1)</sup> | 0.88              | 0.91       | 1.00 | 1.75              | 1.89       | 1.98 | 2.51              | 2.75       | 2.97 | ns    |
| LVC MOS12_F4                 | 0.88              | 0.91       | 1.00 | 1.94              | 2.07       | 2.17 | 2.70              | 2.93       | 3.16 | ns    |
| LVC MOS12_F8                 | 0.88              | 0.91       | 1.00 | 1.50              | 1.64       | 1.73 | 2.26              | 2.50       | 2.72 | ns    |
| LVC MOS12_F12 <sup>(1)</sup> | 0.88              | 0.91       | 1.00 | 1.54              | 1.71       | 1.87 | 2.30              | 2.57       | 2.86 | ns    |
| SSTL135_S                    | 0.61              | 0.64       | 0.73 | 1.27              | 1.40       | 1.50 | 2.03              | 2.26       | 2.49 | ns    |
| SSTL15_S                     | 0.61              | 0.64       | 0.73 | 1.24              | 1.37       | 1.47 | 2.00              | 2.23       | 2.46 | ns    |
| SSTL18_I_S                   | 0.64              | 0.67       | 0.76 | 1.59              | 1.74       | 1.85 | 2.35              | 2.60       | 2.84 | ns    |
| SSTL18_II_S                  | 0.64              | 0.67       | 0.76 | 1.27              | 1.40       | 1.50 | 2.03              | 2.26       | 2.49 | ns    |
| DIFF_SSTL135_S               | 0.59              | 0.61       | 0.73 | 1.27              | 1.40       | 1.50 | 2.03              | 2.26       | 2.49 | ns    |
| DIFF_SSTL15_S                | 0.63              | 0.67       | 0.77 | 1.24              | 1.37       | 1.47 | 2.00              | 2.23       | 2.46 | ns    |
| DIFF_SSTL18_I_S              | 0.65              | 0.69       | 0.78 | 1.50              | 1.63       | 1.72 | 2.26              | 2.49       | 2.71 | ns    |
| DIFF_SSTL18_II_S             | 0.65              | 0.69       | 0.78 | 1.13              | 1.22       | 1.25 | 1.89              | 2.08       | 2.24 | ns    |
| SSTL135_F                    | 0.61              | 0.64       | 0.73 | 1.04              | 1.17       | 1.26 | 1.80              | 2.03       | 2.25 | ns    |
| SSTL15_F                     | 0.61              | 0.64       | 0.73 | 1.04              | 1.17       | 1.26 | 1.80              | 2.03       | 2.25 | ns    |
| SSTL18_I_F                   | 0.64              | 0.67       | 0.76 | 1.12              | 1.22       | 1.26 | 1.88              | 2.08       | 2.25 | ns    |
| SSTL18_II_F                  | 0.64              | 0.67       | 0.76 | 1.05              | 1.18       | 1.28 | 1.81              | 2.04       | 2.27 | ns    |
| DIFF_SSTL135_F               | 0.59              | 0.61       | 0.73 | 1.04              | 1.17       | 1.26 | 1.80              | 2.03       | 2.25 | ns    |
| DIFF_SSTL15_F                | 0.63              | 0.67       | 0.77 | 1.04              | 1.17       | 1.26 | 1.80              | 2.03       | 2.25 | ns    |
| DIFF_SSTL18_I_F              | 0.65              | 0.69       | 0.78 | 1.10              | 1.19       | 1.23 | 1.86              | 2.05       | 2.22 | ns    |
| DIFF_SSTL18_II_F             | 0.65              | 0.69       | 0.78 | 1.02              | 1.10       | 1.14 | 1.78              | 1.96       | 2.13 | ns    |

**Notes:**

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

| I/O Standard            | T <sub>IOPI</sub> |            |      | T <sub>IOOP</sub> |            |      | T <sub>IOTP</sub> |            |      | Units |
|-------------------------|-------------------|------------|------|-------------------|------------|------|-------------------|------------|------|-------|
|                         | Speed Grade       |            |      | Speed Grade       |            |      | Speed Grade       |            |      |       |
|                         | -3                | -2/-2L/-2G | -1   | -3                | -2/-2L/-2G | -1   | -3                | -2/-2L/-2G | -1   |       |
| DIFF_HSTL_I_18_F        | 0.75              | 0.79       | 0.92 | 1.04              | 1.16       | 1.24 | 1.68              | 1.91       | 2.06 | ns    |
| DIFF_HSTL_II_18_F       | 0.75              | 0.79       | 0.92 | 0.98              | 1.09       | 1.16 | 1.62              | 1.85       | 1.98 | ns    |
| DIFF_HSTL_I_DCI_18_F    | 0.75              | 0.79       | 0.92 | 1.04              | 1.16       | 1.24 | 1.67              | 1.91       | 2.06 | ns    |
| DIFF_HSTL_II_DCI_18_F   | 0.75              | 0.79       | 0.92 | 0.98              | 1.09       | 1.16 | 1.61              | 1.85       | 1.98 | ns    |
| DIFF_HSTL_II_T_DCI_18_F | 0.75              | 0.79       | 0.92 | 1.04              | 1.16       | 1.24 | 1.67              | 1.91       | 2.06 | ns    |
| LVC MOS18_S2            | 0.47              | 0.50       | 0.60 | 3.95              | 4.28       | 4.85 | 4.59              | 5.04       | 5.67 | ns    |
| LVC MOS18_S4            | 0.47              | 0.50       | 0.60 | 2.67              | 2.98       | 3.43 | 3.31              | 3.73       | 4.26 | ns    |
| LVC MOS18_S6            | 0.47              | 0.50       | 0.60 | 2.14              | 2.38       | 2.72 | 2.77              | 3.14       | 3.54 | ns    |
| LVC MOS18_S8            | 0.47              | 0.50       | 0.60 | 1.98              | 2.21       | 2.52 | 2.61              | 2.97       | 3.35 | ns    |
| LVC MOS18_S12           | 0.47              | 0.50       | 0.60 | 1.70              | 1.91       | 2.17 | 2.34              | 2.67       | 2.99 | ns    |
| LVC MOS18_S16           | 0.47              | 0.50       | 0.60 | 1.57              | 1.75       | 1.97 | 2.20              | 2.51       | 2.79 | ns    |
| LVC MOS18_F2            | 0.47              | 0.50       | 0.60 | 3.50              | 3.87       | 4.48 | 4.14              | 4.63       | 5.30 | ns    |
| LVC MOS18_F4            | 0.47              | 0.50       | 0.60 | 2.23              | 2.50       | 2.87 | 2.87              | 3.25       | 3.69 | ns    |
| LVC MOS18_F6            | 0.47              | 0.50       | 0.60 | 1.80              | 2.00       | 2.26 | 2.43              | 2.76       | 3.08 | ns    |
| LVC MOS18_F8            | 0.47              | 0.50       | 0.60 | 1.46              | 1.72       | 2.04 | 2.10              | 2.47       | 2.86 | ns    |
| LVC MOS18_F12           | 0.47              | 0.50       | 0.60 | 1.26              | 1.40       | 1.53 | 1.89              | 2.16       | 2.35 | ns    |
| LVC MOS18_F16           | 0.47              | 0.50       | 0.60 | 1.19              | 1.33       | 1.44 | 1.83              | 2.08       | 2.26 | ns    |
| LVC MOS15_S2            | 0.59              | 0.62       | 0.73 | 3.55              | 3.89       | 4.45 | 4.19              | 4.65       | 5.27 | ns    |
| LVC MOS15_S4            | 0.59              | 0.62       | 0.73 | 2.45              | 2.70       | 3.06 | 3.08              | 3.45       | 3.89 | ns    |
| LVC MOS15_S6            | 0.59              | 0.62       | 0.73 | 2.24              | 2.51       | 2.88 | 2.88              | 3.26       | 3.71 | ns    |
| LVC MOS15_S8            | 0.59              | 0.62       | 0.73 | 1.91              | 2.16       | 2.49 | 2.55              | 2.91       | 3.31 | ns    |
| LVC MOS15_S12           | 0.59              | 0.62       | 0.73 | 1.77              | 1.98       | 2.23 | 2.41              | 2.73       | 3.05 | ns    |
| LVC MOS15_S16           | 0.59              | 0.62       | 0.73 | 1.62              | 1.81       | 2.02 | 2.26              | 2.56       | 2.84 | ns    |
| LVC MOS15_F2            | 0.59              | 0.62       | 0.73 | 3.38              | 3.69       | 4.18 | 4.02              | 4.44       | 5.00 | ns    |
| LVC MOS15_F4            | 0.59              | 0.62       | 0.73 | 2.04              | 2.21       | 2.44 | 2.68              | 2.97       | 3.26 | ns    |
| LVC MOS15_F6            | 0.59              | 0.62       | 0.73 | 1.47              | 1.74       | 2.09 | 2.10              | 2.50       | 2.91 | ns    |
| LVC MOS15_F8            | 0.59              | 0.62       | 0.73 | 1.31              | 1.46       | 1.61 | 1.95              | 2.22       | 2.43 | ns    |
| LVC MOS15_F12           | 0.59              | 0.62       | 0.73 | 1.21              | 1.34       | 1.45 | 1.84              | 2.10       | 2.27 | ns    |
| LVC MOS15_F16           | 0.59              | 0.62       | 0.73 | 1.18              | 1.31       | 1.41 | 1.82              | 2.07       | 2.23 | ns    |
| LVC MOS12_S2            | 0.64              | 0.67       | 0.78 | 3.38              | 3.80       | 4.48 | 4.02              | 4.55       | 5.30 | ns    |
| LVC MOS12_S4            | 0.64              | 0.67       | 0.78 | 2.62              | 2.94       | 3.43 | 3.26              | 3.70       | 4.25 | ns    |
| LVC MOS12_S6            | 0.64              | 0.67       | 0.78 | 2.05              | 2.33       | 2.72 | 2.69              | 3.08       | 3.54 | ns    |
| LVC MOS12_S8            | 0.64              | 0.67       | 0.78 | 1.94              | 2.18       | 2.51 | 2.58              | 2.94       | 3.33 | ns    |
| LVC MOS12_F2            | 0.64              | 0.67       | 0.78 | 2.84              | 3.15       | 3.62 | 3.48              | 3.90       | 4.44 | ns    |
| LVC MOS12_F4            | 0.64              | 0.67       | 0.78 | 1.97              | 2.18       | 2.44 | 2.61              | 2.93       | 3.26 | ns    |
| LVC MOS12_F6            | 0.64              | 0.67       | 0.78 | 1.33              | 1.51       | 1.70 | 1.96              | 2.26       | 2.52 | ns    |
| LVC MOS12_F8            | 0.64              | 0.67       | 0.78 | 1.27              | 1.42       | 1.55 | 1.91              | 2.18       | 2.37 | ns    |
| LVDCI_18                | 0.47              | 0.50       | 0.60 | 1.99              | 2.15       | 2.35 | 2.62              | 2.91       | 3.17 | ns    |

Table 23: OLOGIC Switching Characteristics

| Symbol                                   | Description                                        | Speed Grade |            |            | Units   |
|------------------------------------------|----------------------------------------------------|-------------|------------|------------|---------|
|                                          |                                                    | -3          | -2/-2L/-2G | -1         |         |
| Setup/Hold                               |                                                    |             |            |            |         |
| T <sub>ODCK</sub> /T <sub>OCKD</sub>     | D1/D2 pins setup/hold with respect to CLK          | 0.45/−0.13  | 0.50/−0.13 | 0.58/−0.13 | ns      |
| T <sub>OOCECK</sub> /T <sub>OCKOCE</sub> | OCE pin setup/hold with respect to CLK             | 0.28/0.03   | 0.29/0.03  | 0.45/0.03  | ns      |
| T <sub>OSRCK</sub> /T <sub>OCKSR</sub>   | SR pin setup/hold with respect to CLK              | 0.32/0.18   | 0.38/0.18  | 0.70/0.18  | ns      |
| T <sub>OTCK</sub> /T <sub>OCKT</sub>     | T1/T2 pins setup/hold with respect to CLK          | 0.49/−0.16  | 0.56/−0.16 | 0.68/−0.16 | ns      |
| T <sub>OTCECK</sub> /T <sub>OCKTCE</sub> | TCE pin setup/hold with respect to CLK             | 0.28/0.01   | 0.30/0.01  | 0.45/0.01  | ns      |
| Combinatorial                            |                                                    |             |            |            |         |
| T <sub>ODQ</sub>                         | D1 to OQ out or T1 to TQ out                       | 0.73        | 0.81       | 0.97       | ns      |
| Sequential Delays                        |                                                    |             |            |            |         |
| T <sub>OCKQ</sub>                        | CLK to OQ/TQ out                                   | 0.41        | 0.43       | 0.49       | ns      |
| T <sub>RQ_OLOGICE2</sub>                 | SR pin to OQ/TQ out (HP I/O banks only)            | 0.63        | 0.70       | 0.83       | ns      |
| T <sub>GSRQ_OLOGICE2</sub>               | Global set/reset to Q outputs (HP I/O banks only)  | 7.60        | 7.60       | 10.51      | ns      |
| T <sub>RQ_OLOGICE3</sub>                 | SR pin to OQ/TQ out (HR I/O banks only)            | 0.63        | 0.70       | 0.83       | ns      |
| T <sub>GSRQ_OLOGICE3</sub>               | Global set/reset to Q outputs (HR I/O banks only)  | 7.60        | 7.60       | 10.51      | ns      |
| Set/Reset                                |                                                    |             |            |            |         |
| T <sub>RPW_OLOGICE2</sub>                | Minimum pulse width, SR inputs (HP I/O banks only) | 0.54        | 0.54       | 0.63       | ns, Min |
| T <sub>RPW_OLOGICE3</sub>                | Minimum pulse width, SR inputs (HR I/O banks only) | 0.54        | 0.54       | 0.63       | ns, Min |

## Input/Output Delay Switching Characteristics

Table 26: Input/Output Delay Switching Characteristics

| Symbol                                                       | Description                                                                                     | Speed Grade                    |            |           | Units      |
|--------------------------------------------------------------|-------------------------------------------------------------------------------------------------|--------------------------------|------------|-----------|------------|
|                                                              |                                                                                                 | -3                             | -2/-2L/-2G | -1        |            |
| IDELAYCTRL                                                   |                                                                                                 |                                |            |           |            |
| T <sub>DLYCCO_RDY</sub>                                      | Reset to ready for IDELAYCTRL                                                                   | 3.22                           | 3.22       | 3.22      | μs         |
| F <sub>IDELAYCTRL_REF</sub>                                  | Attribute REFCLK frequency = 200.0 <sup>(1)</sup>                                               | 200                            | 200        | 200       | MHz        |
|                                                              | Attribute REFCLK frequency = 300.0 <sup>(1)</sup>                                               | 300                            | 300        | N/A       | MHz        |
| IDELAYCTRL_REF_PRECISION                                     | REFCLK precision                                                                                | ±10                            | ±10        | ±10       | MHz        |
| T <sub>IDELAYCTRL_RPW</sub>                                  | Minimum reset pulse width                                                                       | 52.00                          | 52.00      | 52.00     | ns         |
| IDELAY/ODELAY                                                |                                                                                                 |                                |            |           |            |
| T <sub>IDELAYRESOLUTION</sub>                                | IDELAY/ODELAY chain delay resolution                                                            | 1/(32 x 2 x F <sub>REF</sub> ) |            |           | ps         |
| T <sub>IDELAYPAT_JIT</sub> and T <sub>ODELAYPAT_JIT</sub>    | Pattern dependent period jitter in delay chain for clock pattern. <sup>(2)</sup>                | 0                              | 0          | 0         | ps per tap |
|                                                              | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) <sup>(3)</sup> | ±5                             | ±5         | ±5        | ps per tap |
|                                                              | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) <sup>(4)</sup> | ±9                             | ±9         | ±9        | ps per tap |
| T <sub>IDELAY_CLK_MAX</sub> /<br>T <sub>ODELAY_CLK_MAX</sub> | Maximum frequency of CLK input to IDELAY/ODELAY                                                 | 800                            | 800        | 710       | MHz        |
| T <sub>IDCCK_CE</sub> / T <sub>IDCKC_CE</sub>                | CE pin setup/hold with respect to C for IDELAY                                                  | 0.11/0.10                      | 0.14/0.12  | 0.18/0.14 | ns         |
| T <sub>ODCCK_CE</sub> / T <sub>ODCKC_CE</sub>                | CE pin setup/hold with respect to C for ODELAY                                                  | 0.14/0.03                      | 0.16/0.04  | 0.19/0.05 | ns         |
| T <sub>IDCCK_INC</sub> / T <sub>IDCKC_INC</sub>              | INC pin setup/hold with respect to C for IDELAY                                                 | 0.10/0.14                      | 0.12/0.16  | 0.14/0.20 | ns         |
| T <sub>ODCCK_INC</sub> / T <sub>ODCKC_INC</sub>              | INC pin setup/hold with respect to C for ODELAY                                                 | 0.10/0.07                      | 0.12/0.08  | 0.13/0.09 | ns         |
| T <sub>IDCCK_RST</sub> / T <sub>IDCKC_RST</sub>              | RST pin setup/hold with respect to C for IDELAY                                                 | 0.13/0.08                      | 0.14/0.10  | 0.16/0.12 | ns         |
| T <sub>ODCCK_RST</sub> / T <sub>ODCKC_RST</sub>              | RST pin setup/hold with respect to C for ODELAY                                                 | 0.16/0.04                      | 0.19/0.06  | 0.24/0.08 | ns         |
| T <sub>IDDO_IDATAIN</sub>                                    | Propagation delay through IDELAY                                                                | Note 5                         | Note 5     | Note 5    | ps         |
| T <sub>ODDO_ODATAIN</sub>                                    | Propagation delay through ODELAY                                                                | Note 5                         | Note 5     | Note 5    | ps         |

### Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH\_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH\_PERFORMANCE mode is set to TRUE.
4. When HIGH\_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

## Clock Buffers and Networks

Table 33: Global Clock Switching Characteristics (Including BUFGCTRL)

| Symbol                              | Description                  | Speed Grade |            |           | Units |
|-------------------------------------|------------------------------|-------------|------------|-----------|-------|
|                                     |                              | -3          | -2/-2L/-2G | -1        |       |
| $T_{BCCCK\_CE}/T_{BCCCK\_CE}^{(1)}$ | CE pins setup/hold           | 0.12/0.30   | 0.14/0.38  | 0.26/0.38 | ns    |
| $T_{BCCCK\_S}/T_{BCCCK\_S}^{(1)}$   | S pins setup/hold            | 0.12/0.30   | 0.14/0.38  | 0.26/0.38 | ns    |
| $T_{BCKO\_O}^{(2)}$                 | BUFGCTRL delay from I/O to O | 0.08        | 0.10       | 0.12      | ns    |
| <b>Maximum Frequency</b>            |                              |             |            |           |       |
| $F_{MAX\_BUFG}$                     | Global clock tree (BUFG)     | 741.00      | 710.00     | 625.00    | MHz   |

**Notes:**

1.  $T_{BCCCK\_CE}$  and  $T_{BCCCK\_S}$  must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2.  $T_{BCKO\_O}$  (BUFG delay from I/O to O) values are the same as  $T_{BCKO\_O}$  values.

Table 34: Input/Output Clock Switching Characteristics (BUFIO)

| Symbol                   | Description                    | Speed Grade |            |        | Units |
|--------------------------|--------------------------------|-------------|------------|--------|-------|
|                          |                                | -3          | -2/-2L/-2G | -1     |       |
| $T_{BIOCKO\_O}$          | Clock to out delay from I to O | 1.04        | 1.14       | 1.32   | ns    |
| <b>Maximum Frequency</b> |                                |             |            |        |       |
| $F_{MAX\_BUFIO}$         | I/O clock tree (BUFIO)         | 800.00      | 800.00     | 710.00 | MHz   |

Table 35: Regional Clock Buffer Switching Characteristics (BUFR)

| Symbol                   | Description                                                     | Speed Grade |            |        | Units |
|--------------------------|-----------------------------------------------------------------|-------------|------------|--------|-------|
|                          |                                                                 | -3          | -2/-2L/-2G | -1     |       |
| $T_{BRCKO\_O}$           | Clock to out delay from I to O                                  | 0.60        | 0.65       | 0.77   | ns    |
| $T_{BRCKO\_O\_BYP}$      | Clock to out delay from I to O with Divide Bypass attribute set | 0.30        | 0.32       | 0.38   | ns    |
| $T_{BRDO\_O}$            | Propagation delay from CLR to O                                 | 0.71        | 0.75       | 0.96   | ns    |
| <b>Maximum Frequency</b> |                                                                 |             |            |        |       |
| $F_{MAX\_BUFR}^{(1)}$    | Regional clock tree (BUFR)                                      | 600.00      | 540.00     | 450.00 | MHz   |

**Notes:**

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO  $F_{MAX}$  frequency.

Table 36: Horizontal Clock Buffer Switching Characteristics (BUFH)

| Symbol                          | Description                    | Speed Grade |            |           | Units |
|---------------------------------|--------------------------------|-------------|------------|-----------|-------|
|                                 |                                | -3          | -2/-2L/-2G | -1        |       |
| $T_{BHCKO\_O}$                  | BUFH delay from I to O         | 0.10        | 0.11       | 0.13      | ns    |
| $T_{BHCKCK\_CE}/T_{BHCKCK\_CE}$ | CE pin setup and hold          | 0.20/0.16   | 0.23/0.20  | 0.38/0.21 | ns    |
| <b>Maximum Frequency</b>        |                                |             |            |           |       |
| $F_{MAX\_BUFH}$                 | Horizontal clock buffer (BUFH) | 741.00      | 710.00     | 625.00    | MHz   |

## Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

**Table 45: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD\_DELAY on HR I/O Banks (only)**

| Symbol                                                                                              | Description                                                                                                                                  | Device     | Speed Grade |            |            | Units |
|-----------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|------------|-------------|------------|------------|-------|
|                                                                                                     |                                                                                                                                              |            | -3          | -2/-2L/-2G | -1         |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. <sup>(1)</sup> |                                                                                                                                              |            |             |            |            |       |
| T <sub>PSFD</sub> / T <sub>PHFD</sub>                                                               | Full delay (legacy delay or default delay)<br>Global clock Input and IFF <sup>(2)</sup> without MMCM/PLL<br>with ZHOLD_DELAY on HR I/O banks | XC7V585T   | 3.12/−0.37  | 3.19/−0.37 | 3.42/−0.37 | ns    |
|                                                                                                     |                                                                                                                                              | XC7V2000T  | N/A         | N/A        | N/A        | ns    |
|                                                                                                     |                                                                                                                                              | XC7VX330T  | 2.90/−0.31  | 2.96/−0.31 | 3.16/−0.31 | ns    |
|                                                                                                     |                                                                                                                                              | XC7VX415T  | N/A         | N/A        | N/A        | ns    |
|                                                                                                     |                                                                                                                                              | XC7VX485T  | N/A         | N/A        | N/A        | ns    |
|                                                                                                     |                                                                                                                                              | XC7VX550T  | N/A         | N/A        | N/A        | ns    |
|                                                                                                     |                                                                                                                                              | XC7VX690T  | N/A         | N/A        | N/A        | ns    |
|                                                                                                     |                                                                                                                                              | XC7VX980T  | N/A         | N/A        | N/A        | ns    |
|                                                                                                     |                                                                                                                                              | XC7VX1140T | N/A         | N/A        | N/A        | ns    |

### Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch

**Table 46: Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol                                                                                                 | Description                                                         | Device     | Speed Grade |            |            | Units |
|--------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|------------|-------------|------------|------------|-------|
|                                                                                                        |                                                                     |            | -3          | -2/-2L/-2G | -1         |       |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. <sup>(1)(2)</sup> |                                                                     |            |             |            |            |       |
| T <sub>PSMMCMCC</sub> /<br>T <sub>PHMMCMCC</sub>                                                       | No delay clock-capable clock input and IFF <sup>(3)</sup> with MMCM | XC7V585T   | 2.71/−0.10  | 3.00/−0.10 | 3.33/−0.10 | ns    |
|                                                                                                        |                                                                     | XC7V2000T  | N/A         | 2.60/−0.24 | 2.87/−0.24 | ns    |
|                                                                                                        |                                                                     | XC7VX330T  | 2.58/−0.15  | 2.87/−0.15 | 3.18/−0.15 | ns    |
|                                                                                                        |                                                                     | XC7VX415T  | 2.73/0.01   | 3.03/0.01  | 3.36/0.01  | ns    |
|                                                                                                        |                                                                     | XC7VX485T  | 2.58/−0.15  | 2.87/−0.15 | 3.18/−0.15 | ns    |
|                                                                                                        |                                                                     | XC7VX550T  | 2.72/−0.09  | 3.01/−0.09 | 3.34/−0.09 | ns    |
|                                                                                                        |                                                                     | XC7VX690T  | 2.72/0.01   | 3.01/0.01  | 3.34/0.01  | ns    |
|                                                                                                        |                                                                     | XC7VX980T  | N/A         | 3.01/−0.10 | 3.36/−0.10 | ns    |
|                                                                                                        |                                                                     | XC7VX1140T | N/A         | 2.61/−0.24 | 2.88/−0.24 | ns    |

### Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 47: Clock-Capable Clock Input Setup and Hold With PLL

| Symbol                                                                                                        | Description                                                        | Device     | Speed Grade |            |            | Units |
|---------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|------------|-------------|------------|------------|-------|
|                                                                                                               |                                                                    |            | -3          | -2/-2L/-2G | -1         |       |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. <sup>(1)(2)</sup> |                                                                    |            |             |            |            |       |
| T <sub>PSPLLCC</sub> /<br>T <sub>PHPLLCC</sub>                                                                | No delay clock-capable clock input and IFF <sup>(3)</sup> with PLL | XC7V585T   | 3.07/−0.21  | 3.40/−0.21 | 3.72/−0.21 | ns    |
|                                                                                                               |                                                                    | XC7V2000T  | N/A         | 2.99/−0.35 | 3.27/−0.35 | ns    |
|                                                                                                               |                                                                    | XC7VX330T  | 2.94/−0.26  | 3.26/−0.26 | 3.57/−0.26 | ns    |
|                                                                                                               |                                                                    | XC7VX415T  | 3.09/−0.10  | 3.42/−0.10 | 3.75/−0.10 | ns    |
|                                                                                                               |                                                                    | XC7VX485T  | 2.95/−0.26  | 3.26/−0.26 | 3.58/−0.26 | ns    |
|                                                                                                               |                                                                    | XC7VX550T  | 3.08/−0.20  | 3.40/−0.20 | 3.74/−0.20 | ns    |
|                                                                                                               |                                                                    | XC7VX690T  | 3.08/−0.10  | 3.40/−0.10 | 3.74/−0.10 | ns    |
|                                                                                                               |                                                                    | XC7VX980T  | N/A         | 3.39/−0.21 | 3.72/−0.21 | ns    |
|                                                                                                               |                                                                    | XC7VX1140T | N/A         | 3.00/−0.35 | 3.27/−0.35 | ns    |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. IFF = Input Flip-Flop or Latch
4. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

| Symbol                                                                                             | Description                              | Speed Grade |            |            | Units |
|----------------------------------------------------------------------------------------------------|------------------------------------------|-------------|------------|------------|-------|
|                                                                                                    |                                          | -3          | -2/-2L/-2G | -1         |       |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. |                                          |             |            |            |       |
| T <sub>PSCS</sub> /T <sub>PHCS</sub>                                                               | Setup/hold of I/O clock for HR I/O banks | –0.36/1.36  | –0.36/1.50 | –0.36/1.70 | ns    |
|                                                                                                    | Setup/hold of I/O clock for HP I/O banks | –0.34/1.39  | –0.34/1.53 | –0.34/1.73 | ns    |

Table 49: Sample Window

| Symbol                  | Description                                                | Speed Grade |            |      | Units |
|-------------------------|------------------------------------------------------------|-------------|------------|------|-------|
|                         |                                                            | -3          | -2/-2L/-2G | -1   |       |
| T <sub>SAMP</sub>       | Sampling error at receiver pins <sup>(1)</sup>             | 0.51        | 0.56       | 0.61 | ns    |
| T <sub>SAMP_BUFIO</sub> | Sampling error at receiver pins using BUFIO <sup>(2)</sup> | 0.30        | 0.35       | 0.40 | ns    |

**Notes:**

1. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
  - CLK0 MMCM jitter
  - MMCM accuracy (phase offset)
  - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further details.

Table 52: GTX Transceiver Clock DC Input Level Specification

| Symbol             | DC Parameter                            | Min | Typ | Max  | Units |
|--------------------|-----------------------------------------|-----|-----|------|-------|
| V <sub>IDIFF</sub> | Differential peak-to-peak input voltage | 250 | –   | 2000 | mV    |
| R <sub>IN</sub>    | Differential input resistance           | –   | 100 | –    | Ω     |
| C <sub>EXT</sub>   | Required external AC coupling capacitor | –   | 100 | –    | nF    |

## GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further information.

Table 53: GTX Transceiver Performance

| Symbol                             | Description                            | Output Divider | Speed Grade    |                   |                   | Units |
|------------------------------------|----------------------------------------|----------------|----------------|-------------------|-------------------|-------|
|                                    |                                        |                | -3/-2G         | -2/-2L            | -1 <sup>(1)</sup> |       |
| F <sub>GTXMAX</sub> <sup>(2)</sup> | Maximum GTX transceiver data rate      |                | 12.5           | 10.3125           | 8.0               | Gb/s  |
| F <sub>GTXMIN</sub> <sup>(2)</sup> | Minimum GTX transceiver data rate      |                | 0.500          | 0.500             | 0.500             | Gb/s  |
| F <sub>GTXCRANGE</sub>             | CPLL line rate range                   | 1              | 3.2–6.6        |                   |                   | Gb/s  |
|                                    |                                        | 2              | 1.6–3.3        |                   |                   | Gb/s  |
|                                    |                                        | 4              | 0.8–1.65       |                   |                   | Gb/s  |
|                                    |                                        | 8              | 0.5–0.825      |                   |                   | Gb/s  |
|                                    |                                        | 16             | N/A            |                   |                   | Gb/s  |
| F <sub>GTXQRANGE1</sub>            | QPLL line rate range 1                 | 1              | 5.93–8.0       | 5.93–8.0          | 5.93–8.0          | Gb/s  |
|                                    |                                        | 2              | 2.965–4.0      | 2.965–4.0         | 2.965–4.0         | Gb/s  |
|                                    |                                        | 4              | 1.4825–2.0     | 1.4825–2.0        | 1.4825–2.0        | Gb/s  |
|                                    |                                        | 8              | 0.74125–1.0    | 0.74125–1.0       | 0.74125–1.0       | Gb/s  |
|                                    |                                        | 16             | N/A            | N/A               | N/A               | Gb/s  |
| F <sub>GTXQRANGE2</sub>            | QPLL line rate range 2 <sup>(3)</sup>  | 1              | 9.8–12.5       | 9.8–10.3125       | N/A               | Gb/s  |
|                                    |                                        | 2              | 4.9–6.25       | 4.9–5.15625       | N/A               | Gb/s  |
|                                    |                                        | 4              | 2.45–3.125     | 2.45–2.578125     | N/A               | Gb/s  |
|                                    |                                        | 8              | 1.225–1.5625   | 1.225–1.2890625   | N/A               | Gb/s  |
|                                    |                                        | 16             | 0.6125–0.78125 | 0.6125–0.64453125 | N/A               | Gb/s  |
| F <sub>GCPLLRANGE</sub>            | GTX transceiver CPLL frequency range   |                | 1.6–3.3        | 1.6–3.3           | 1.6–3.3           | GHz   |
| F <sub>GQPLLRange1</sub>           | GTX transceiver QPLL frequency range 1 |                | 5.93–8.0       | 5.93–8.0          | 5.93–8.0          | GHz   |
| F <sub>GQPLLRange2</sub>           | GTX transceiver QPLL frequency range 2 |                | 9.8–12.5       | 9.8–10.3125       | N/A               | GHz   |

### Notes:

- The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V<sub>CCINT</sub> = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), requires a 4-byte internal data width for operation above 3.8 Gb/s.
- Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
- For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol                 | Description                 | Speed Grade |        |        | Units |
|------------------------|-----------------------------|-------------|--------|--------|-------|
|                        |                             | -3/-2G      | -2/-2L | -1     |       |
| F <sub>GTXDRPCLK</sub> | GTXDRPCLK maximum frequency | 175.01      | 175.01 | 156.25 | MHz   |

Table 59: GTX Transceiver Receiver Switching Characteristics

| Symbol                                               | Description                                                   |                                     | Min   | Typ | Max                 | Units |
|------------------------------------------------------|---------------------------------------------------------------|-------------------------------------|-------|-----|---------------------|-------|
| F <sub>GTXRX</sub>                                   | Serial data rate                                              | RX oversampler not enabled          | 0.500 | –   | F <sub>GTXMAX</sub> | Gb/s  |
| T <sub>RXELECIDLE</sub>                              | Time for RXELECIDLE to respond to loss or restoration of data |                                     | –     | 10  | –                   | ns    |
| RX <sub>OOBVDPP</sub>                                | OOB detect threshold peak-to-peak                             |                                     | 60    | –   | 150                 | mV    |
| RX <sub>SST</sub>                                    | Receiver spread-spectrum tracking <sup>(1)</sup>              | Modulated @ 33 KHz                  | –5000 | –   | 0                   | ppm   |
| RX <sub>RL</sub>                                     | Run length (CID)                                              |                                     | –     | –   | 512                 | UI    |
| RX <sub>PPMTOL</sub>                                 | Data/REFCLK PPM offset tolerance                              | Bit rates ≤ 6.6 Gb/s                | –1250 | –   | 1250                | ppm   |
|                                                      |                                                               | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700  | –   | 700                 | ppm   |
|                                                      |                                                               | Bit rates > 8.0 Gb/s                | –200  | –   | 200                 | ppm   |
| SJ Jitter Tolerance <sup>(2)</sup>                   |                                                               |                                     |       |     |                     |       |
| JT_SJ <sub>12.5</sub>                                | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 12.5 Gb/s                           | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>11.18</sub>                               | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 11.18 Gb/s                          | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>10.32</sub>                               | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 10.32 Gb/s                          | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>9.95</sub>                                | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 9.95 Gb/s                           | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>9.8</sub>                                 | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 9.8 Gb/s                            | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>8.0</sub>                                 | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 8.0 Gb/s                            | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>6.6_QPLL</sub>                            | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 6.6 Gb/s                            | 0.48  | –   | –                   | UI    |
| JT_SJ <sub>6.6_CPLL</sub>                            | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 6.6 Gb/s                            | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>5.0</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 5.0 Gb/s                            | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>4.25</sub>                                | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 4.25 Gb/s                           | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>3.75</sub>                                | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 3.75 Gb/s                           | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>3.2</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 3.2 Gb/s <sup>(4)</sup>             | 0.45  | –   | –                   | UI    |
| JT_SJ <sub>3.2L</sub>                                | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 3.2 Gb/s <sup>(5)</sup>             | 0.45  | –   | –                   | UI    |
| JT_SJ <sub>2.5</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 2.5 Gb/s <sup>(6)</sup>             | 0.5   | –   | –                   | UI    |
| JT_SJ <sub>1.25</sub>                                | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 1.25 Gb/s <sup>(7)</sup>            | 0.5   | –   | –                   | UI    |
| JT_SJ <sub>500</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 500 Mb/s                            | 0.4   | –   | –                   | UI    |
| SJ Jitter Tolerance with Stressed Eye <sup>(2)</sup> |                                                               |                                     |       |     |                     |       |
| JT_TJSE <sub>3.2</sub>                               | Total jitter with stressed eye <sup>(8)</sup>                 | 3.2 Gb/s                            | 0.70  | –   | –                   | UI    |
| JT_TJSE <sub>6.6</sub>                               |                                                               | 6.6 Gb/s                            | 0.70  | –   | –                   | UI    |
| JT_SJSE <sub>3.2</sub>                               | Sinusoidal jitter with stressed eye <sup>(8)</sup>            | 3.2 Gb/s                            | 0.1   | –   | –                   | UI    |
| JT_SJSE <sub>6.6</sub>                               |                                                               | 6.6 Gb/s                            | 0.1   | –   | –                   | UI    |

**Notes:**

- Using RXOUT\_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of  $1e^{-12}$ .
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 1.6 GHz and RXOUT\_DIV = 1.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

Table 65: CPRI Protocol Characteristics (GTX Transceivers)

| Description                                     | Line Rate (Mb/s) | Min    | Max    | Units |
|-------------------------------------------------|------------------|--------|--------|-------|
| <b>CPRI Transmitter Jitter Generation</b>       |                  |        |        |       |
| Total transmitter jitter                        | 614.4            | –      | 0.35   | UI    |
|                                                 | 1228.8           | –      | 0.35   | UI    |
|                                                 | 2457.6           | –      | 0.35   | UI    |
|                                                 | 3072.0           | –      | 0.35   | UI    |
|                                                 | 4915.2           | –      | 0.3    | UI    |
|                                                 | 6144.0           | –      | 0.3    | UI    |
|                                                 | 9830.4           | –      | Note 1 | UI    |
| <b>CPRI Receiver Frequency Jitter Tolerance</b> |                  |        |        |       |
| Total receiver jitter tolerance                 | 614.4            | 0.65   | –      | UI    |
|                                                 | 1228.8           | 0.65   | –      | UI    |
|                                                 | 2457.6           | 0.65   | –      | UI    |
|                                                 | 3072.0           | 0.65   | –      | UI    |
|                                                 | 4915.2           | 0.95   | –      | UI    |
|                                                 | 6144.0           | 0.95   | –      | UI    |
|                                                 | 9830.4           | Note 1 | –      | UI    |

**Notes:**

1. Tested per SFP+ specification, see Table 64.

Table 67 summarizes the DC specifications of the clock input of the GTH transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further details.

Table 67: GTH Transceiver Clock DC Input Level Specification

| Symbol             | DC Parameter                            | Min | Typ | Max  | Units |
|--------------------|-----------------------------------------|-----|-----|------|-------|
| V <sub>IDIFF</sub> | Differential peak-to-peak input voltage | 350 | –   | 2000 | mV    |
| R <sub>IN</sub>    | Differential input resistance           | –   | 100 | –    | Ω     |
| C <sub>EXT</sub>   | Required external AC coupling capacitor | –   | 100 | –    | nF    |

## GTH Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further information.

Table 68: GTH Transceiver Performance

| Symbol                   | Description                            | Output Divider | Speed Grade |              |                        | Units |
|--------------------------|----------------------------------------|----------------|-------------|--------------|------------------------|-------|
|                          |                                        |                | -3E/-2GE    | -2(C&I)/-2LE | -1(C&I) <sup>(1)</sup> |       |
| F <sub>GTHMAX</sub>      | Maximum GTH transceiver data rate      |                | 13.1        | 11.3         | 8.5                    | Gb/s  |
| F <sub>GTHMIN</sub>      | Minimum GTH transceiver data rate      |                | 0.500       | 0.500        | 0.500                  | Gb/s  |
| F <sub>GTHCRANGE</sub>   | CPLL line rate range                   | 1              | 3.2–10.3125 |              | 3.2–8.0                | Gb/s  |
|                          |                                        | 2              | 1.6–5.16    |              | 1.6–4.0                | Gb/s  |
|                          |                                        | 4              | 0.8–2.58    |              | 0.8–2.0                | Gb/s  |
|                          |                                        | 8              | 0.5–1.29    |              | 0.5–1.0                | Gb/s  |
|                          |                                        | 16             | N/A         |              |                        | Gb/s  |
| F <sub>GTHQRANGE1</sub>  | QPLL line rate range 1                 | 1              | 8.0–11.85   | 8.0–11.3     | 8.0–8.5                | Gb/s  |
|                          |                                        | 2              | 4.0–5.925   | 4.0–5.65     | 4.0–4.25               | Gb/s  |
|                          |                                        | 4              | 2.0–2.9625  | 2.0–2.825    | 2.0–2.125              | Gb/s  |
|                          |                                        | 8              | 1.0–1.48125 | 1.0–1.4125   | 1.0–1.0625             | Gb/s  |
|                          |                                        | 16             | N/A         |              |                        | Gb/s  |
| F <sub>GTHQRANGE2</sub>  | QPLL line rate range 2                 | 1              | 11.85–13.1  | N/A          |                        | Gb/s  |
|                          |                                        | 2              | 5.925–6.55  | N/A          |                        | Gb/s  |
|                          |                                        | 4              | 2.96–3.275  | N/A          |                        | Gb/s  |
|                          |                                        | 8              | 1.48–1.63   | N/A          |                        | Gb/s  |
|                          |                                        | 16             | 0.74–0.81   | N/A          |                        | Gb/s  |
| F <sub>GCPLLRANGE</sub>  | GTH transceiver CPLL frequency range   |                | 1.6–5.16    |              | 1.6–4.0                | GHz   |
| F <sub>GQPLLRange1</sub> | GTH transceiver QPLL frequency range 1 |                | 8.0–11.85   | 8.0–11.3     | 8.0–8.5                | GHz   |
| F <sub>GQPLLRange2</sub> | GTH transceiver QPLL frequency range 2 |                | 11.85–13.1  | N/A          |                        | GHz   |

### Notes:

- The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V<sub>CCINT</sub> = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), requires a 4-byte internal data width for operation above 3.8 Gb/s.

Table 69: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol                 | Description                 | Speed Grade |     |     |     | Units |
|------------------------|-----------------------------|-------------|-----|-----|-----|-------|
|                        |                             | -3/-2G      | -2L | -2  | -1  |       |
| F <sub>GTHDRPCLK</sub> | GTHDRPCLK maximum frequency | 175         | 175 | 175 | 156 | MHz   |

Table 72: GTH Transceiver User Clock Switching Characteristics<sup>(1)</sup>

| Symbol             | Description                    | Data Width Conditions |                    | Speed Grade             |                             |                        | Units |
|--------------------|--------------------------------|-----------------------|--------------------|-------------------------|-----------------------------|------------------------|-------|
|                    |                                | Internal Logic        | Interconnect Logic | -3E/-2GE <sup>(2)</sup> | -2(C&I)/-2LE <sup>(2)</sup> | -1(C&I) <sup>(3)</sup> |       |
| F <sub>TXOUT</sub> | TXUSERCLKOUT maximum frequency |                       |                    | 412.500                 | 412.500                     | 312.500                | MHz   |
| F <sub>RXOUT</sub> | RXUSERCLKOUT maximum frequency |                       |                    | 412.500                 | 412.500                     | 312.500                | MHz   |
| F <sub>TXIN</sub>  | TXUSERCLKIN maximum frequency  | 16-bit                | 16-bit and 32-bit  | 412.500                 | 412.500                     | 312.500                | MHz   |
|                    |                                | 32-bit                | 32-bit             | 409.375                 | 353.125                     | 265.625                | MHz   |
| F <sub>RXIN</sub>  | RXUSERCLKIN maximum frequency  | 16-bit                | 16-bit and 32-bit  | 412.500                 | 412.500                     | 312.500                | MHz   |
|                    |                                | 32-bit                | 32-bit             | 409.375                 | 353.125                     | 265.625                | MHz   |
| F <sub>TXIN2</sub> | TXUSERCLKIN2 maximum frequency | 16-bit                | 16-bit             | 412.500                 | 412.500                     | 312.500                | MHz   |
|                    |                                | 16-bit and 32-bit     | 32-bit             | 409.375                 | 353.125                     | 265.625                | MHz   |
|                    |                                | 64-bit                | 64-bit             | 204.688                 | 176.563                     | 132.813                | MHz   |
| F <sub>RXIN2</sub> | RXUSERCLKIN2 maximum frequency | 16-bit                | 16-bit             | 412.500                 | 412.500                     | 312.500                | MHz   |
|                    |                                | 16-bit and 32-bit     | 32-bit             | 409.375                 | 353.125                     | 265.625                | MHz   |
|                    |                                | 64-bit                | 64-bit             | 204.688                 | 176.563                     | 132.813                | MHz   |

**Notes:**

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
2. For speed grades -3E, -2GE, -2C, -2I, and -2LE, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
3. For speed grade -1 (and when V<sub>CCINT</sub> = 0.9V), a 16-bit data path can only be used for speeds less than 5.0 Gb/s.

Table 73: GTH Transceiver Transmitter Switching Characteristics

| Symbol                       | Description                            | Condition    | Min   | Typ | Max                 | Units |
|------------------------------|----------------------------------------|--------------|-------|-----|---------------------|-------|
| F <sub>GTHTX</sub>           | Serial data rate range                 |              | 0.500 | —   | F <sub>GTHMAX</sub> | Gb/s  |
| T <sub>RTX</sub>             | TX rise time                           | 20%–80%      | —     | 40  | —                   | ps    |
| T <sub>FTX</sub>             | TX fall time                           | 80%–20%      | —     | 40  | —                   | ps    |
| T <sub>LLSKEW</sub>          | TX lane-to-lane skew <sup>(1)</sup>    |              | —     | —   | 500                 | ps    |
| V <sub>TXOOBVDPP</sub>       | Electrical idle amplitude              |              | —     | —   | 15                  | mV    |
| T <sub>TXOOBTRANSITION</sub> | Electrical idle transition time        |              | —     | —   | 140                 | ns    |
| TJ <sub>13.1</sub>           | Total jitter <sup>(2)(4)</sup>         | 13.1 Gb/s    | —     | —   | 0.3                 | UI    |
| DJ <sub>13.1</sub>           | Deterministic jitter <sup>(2)(4)</sup> |              | —     | —   | 0.17                | UI    |
| TJ <sub>12.5</sub>           | Total jitter <sup>(2)(4)</sup>         | 12.5 Gb/s    | —     | —   | 0.28                | UI    |
| DJ <sub>12.5</sub>           | Deterministic jitter <sup>(2)(4)</sup> |              | —     | —   | 0.17                | UI    |
| TJ <sub>11.3</sub>           | Total jitter <sup>(2)(4)</sup>         | 11.3 Gb/s    | —     | —   | 0.28                | UI    |
| DJ <sub>11.3</sub>           | Deterministic jitter <sup>(2)(4)</sup> |              | —     | —   | 0.17                | UI    |
| TJ <sub>10.3125_QPLL</sub>   | Total jitter <sup>(2)(4)</sup>         | 10.3125 Gb/s | —     | —   | 0.28                | UI    |
| DJ <sub>10.3125_QPLL</sub>   | Deterministic jitter <sup>(2)(4)</sup> |              | —     | —   | 0.17                | UI    |
| TJ <sub>10.3125_CPLL</sub>   | Total jitter <sup>(3)(4)</sup>         | 10.3125 Gb/s | —     | —   | 0.33                | UI    |
| DJ <sub>10.3125_CPLL</sub>   | Deterministic jitter <sup>(3)(4)</sup> |              | —     | —   | 0.17                | UI    |
| TJ <sub>9.953</sub>          | Total jitter <sup>(2)(4)</sup>         | 9.953 Gb/s   | —     | —   | 0.28                | UI    |
| DJ <sub>9.953</sub>          | Deterministic jitter <sup>(2)(4)</sup> |              | —     | —   | 0.17                | UI    |
| TJ <sub>9.8</sub>            | Total jitter <sup>(2)(4)</sup>         | 9.8 Gb/s     | —     | —   | 0.28                | UI    |
| DJ <sub>9.8</sub>            | Deterministic jitter <sup>(2)(4)</sup> |              | —     | —   | 0.17                | UI    |
| TJ <sub>8.0_QPLL</sub>       | Total jitter <sup>(2)(4)</sup>         | 8.0 Gb/s     | —     | —   | 0.28                | UI    |
| DJ <sub>8.0_QPLL</sub>       | Deterministic jitter <sup>(2)(4)</sup> |              | —     | —   | 0.17                | UI    |

Table 73: GTH Transceiver Transmitter Switching Characteristics (Cont'd)

| Symbol                 | Description                            | Condition                | Min | Typ | Max  | Units |
|------------------------|----------------------------------------|--------------------------|-----|-----|------|-------|
| TJ <sub>8.0_CPLL</sub> | Total jitter <sup>(3)(4)</sup>         | 8.0 Gb/s                 | –   | –   | 0.32 | UI    |
| DJ <sub>8.0_CPLL</sub> | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.17 | UI    |
| TJ <sub>6.6_QPLL</sub> | Total jitter <sup>(2)(4)</sup>         | 6.6 Gb/s                 | –   | –   | 0.28 | UI    |
| DJ <sub>6.6_QPLL</sub> | Deterministic jitter <sup>(2)(4)</sup> |                          | –   | –   | 0.17 | UI    |
| TJ <sub>6.6_CPLL</sub> | Total jitter <sup>(3)(4)</sup>         | 6.6 Gb/s                 | –   | –   | 0.30 | UI    |
| DJ <sub>6.6_CPLL</sub> | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.15 | UI    |
| TJ <sub>5.0</sub>      | Total jitter <sup>(3)(4)</sup>         | 5.0 Gb/s                 | –   | –   | 0.30 | UI    |
| DJ <sub>5.0</sub>      | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.15 | UI    |
| TJ <sub>4.25</sub>     | Total jitter <sup>(3)(4)</sup>         | 4.25 Gb/s                | –   | –   | 0.30 | UI    |
| DJ <sub>4.25</sub>     | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.15 | UI    |
| TJ <sub>3.75</sub>     | Total jitter <sup>(3)(4)</sup>         | 3.75 Gb/s                | –   | –   | 0.30 | UI    |
| DJ <sub>3.75</sub>     | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.15 | UI    |
| TJ <sub>3.20</sub>     | Total jitter <sup>(3)(4)</sup>         | 3.20 Gb/s <sup>(5)</sup> | –   | –   | 0.2  | UI    |
| DJ <sub>3.20</sub>     | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.1  | UI    |
| TJ <sub>3.20L</sub>    | Total jitter <sup>(3)(4)</sup>         | 3.20 Gb/s <sup>(6)</sup> | –   | –   | 0.32 | UI    |
| DJ <sub>3.20L</sub>    | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.16 | UI    |
| TJ <sub>2.5</sub>      | Total jitter <sup>(3)(4)</sup>         | 2.5 Gb/s <sup>(7)</sup>  | –   | –   | 0.20 | UI    |
| DJ <sub>2.5</sub>      | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.08 | UI    |
| TJ <sub>1.25</sub>     | Total jitter <sup>(3)(4)</sup>         | 1.25 Gb/s <sup>(8)</sup> | –   | –   | 0.15 | UI    |
| DJ <sub>1.25</sub>     | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.06 | UI    |
| TJ <sub>500</sub>      | Total jitter <sup>(3)(4)</sup>         | 500 Mb/s                 | –   | –   | 0.1  | UI    |
| DJ <sub>500</sub>      | Deterministic jitter <sup>(3)(4)</sup> |                          | –   | –   | 0.03 | UI    |

**Notes:**

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTH Quads).
- Using QPLL\_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL\_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e<sup>-12</sup>.
- CPLL frequency at 3.2 GHz and TXOUT\_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT\_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT\_DIV = 4.

Table 74: GTH Transceiver Receiver Switching Characteristics

| Symbol                                               | Description                                                   |                                     | Min   | Typ | Max                 | Units |
|------------------------------------------------------|---------------------------------------------------------------|-------------------------------------|-------|-----|---------------------|-------|
| F <sub>GTHRX</sub>                                   | Serial data rate                                              | RX oversampler not enabled          | 0.500 | –   | F <sub>GTHMAX</sub> | Gb/s  |
| T <sub>RXELECIDLE</sub>                              | Time for RXELECIDLE to respond to loss or restoration of data |                                     | –     | 10  | –                   | ns    |
| RX <sub>OOBVDPP</sub>                                | OOB detect threshold peak-to-peak                             |                                     | 60    | –   | 150                 | mV    |
| RX <sub>SST</sub>                                    | Receiver spread-spectrum tracking <sup>(1)</sup>              | Modulated @ 33 KHz                  | –5000 | –   | 0                   | ppm   |
| RX <sub>RL</sub>                                     | Run length (CID)                                              |                                     | –     | –   | 512                 | UI    |
| RX <sub>PPMTOL</sub>                                 | Data/REFCLK PPM offset tolerance                              | Bit rates ≤ 6.6 Gb/s                | –1250 | –   | 1250                | ppm   |
|                                                      |                                                               | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700  | –   | 700                 | ppm   |
|                                                      |                                                               | Bit rates > 8.0 Gb/s                | –200  | –   | 200                 | ppm   |
| SJ Jitter Tolerance <sup>(2)</sup>                   |                                                               |                                     |       |     |                     |       |
| JT_SJ <sub>13.1</sub>                                | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 13.1 Gb/s                           | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>12.5</sub>                                | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 12.5 Gb/s                           | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>11.3</sub>                                | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 11.3 Gb/s                           | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>10.32_QPLL</sub>                          | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 10.32 Gb/s                          | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>10.32_CPLL</sub>                          | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 10.32 Gb/s                          | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>9.8</sub>                                 | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 9.8 Gb/s                            | 0.3   | –   | –                   | UI    |
| JT_SJ <sub>8.0_QPLL</sub>                            | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 8.0 Gb/s                            | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>8.0_CPLL</sub>                            | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 8.0 Gb/s                            | 0.42  | –   | –                   | UI    |
| JT_SJ <sub>6.6_QPLL</sub>                            | Sinusoidal jitter (QPLL) <sup>(3)</sup>                       | 6.6 Gb/s                            | 0.48  | –   | –                   | UI    |
| JT_SJ <sub>6.6_CPLL</sub>                            | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 6.6 Gb/s                            | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>5.0</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 5.0 Gb/s                            | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>4.25</sub>                                | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 4.25 Gb/s                           | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>3.75</sub>                                | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 3.75 Gb/s                           | 0.44  | –   | –                   | UI    |
| JT_SJ <sub>3.2</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 3.2 Gb/s <sup>(4)</sup>             | 0.45  | –   | –                   | UI    |
| JT_SJ <sub>3.2L</sub>                                | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 3.2 Gb/s <sup>(5)</sup>             | 0.45  | –   | –                   | UI    |
| JT_SJ <sub>2.5</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 2.5 Gb/s <sup>(6)</sup>             | 0.5   | –   | –                   | UI    |
| JT_SJ <sub>1.25</sub>                                | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 1.25 Gb/s <sup>(7)</sup>            | 0.5   | –   | –                   | UI    |
| JT_SJ <sub>500</sub>                                 | Sinusoidal jitter (CPLL) <sup>(3)</sup>                       | 500 Mb/s                            | 0.4   | –   | –                   | UI    |
| SJ Jitter Tolerance with Stressed Eye <sup>(2)</sup> |                                                               |                                     |       |     |                     |       |
| JT_TJSE <sub>3.2</sub>                               | Total jitter with stressed eye <sup>(8)</sup>                 | 3.2 Gb/s                            | 0.70  | –   | –                   | UI    |
| JT_TJSE <sub>6.6</sub>                               |                                                               | 6.6 Gb/s                            | 0.70  | –   | –                   | UI    |
| JT_SJSE <sub>3.2</sub>                               | Sinusoidal jitter with stressed eye <sup>(8)</sup>            | 3.2 Gb/s                            | 0.1   | –   | –                   | UI    |
| JT_SJSE <sub>6.6</sub>                               |                                                               | 6.6 Gb/s                            | 0.1   | –   | –                   | UI    |

**Notes:**

- Using RXOUT\_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e<sup>–12</sup>.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 1.6 GHz and RXOUT\_DIV = 1.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

## GTH Transceiver Protocol Jitter Characteristics

For Table 75 through Table 80, the 7 Series FPGAs GTX/GTH Transceiver User Guide ([UG476](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 75: Gigabit Ethernet Protocol Characteristics (GTH Transceivers)

| Description                                                      | Line Rate (Mb/s) | Min   | Max  | Units |
|------------------------------------------------------------------|------------------|-------|------|-------|
| <b>Gigabit Ethernet Transmitter Jitter Generation</b>            |                  |       |      |       |
| Total transmitter jitter (T <sub>TJ</sub> )                      | 1250             | –     | 0.24 | UI    |
| <b>Gigabit Ethernet Receiver High Frequency Jitter Tolerance</b> |                  |       |      |       |
| Total receiver jitter tolerance                                  | 1250             | 0.749 | –    | UI    |

Table 76: XAUI Protocol Characteristics (GTH Transceivers)

| Description                                          | Line Rate (Mb/s) | Min  | Max  | Units |
|------------------------------------------------------|------------------|------|------|-------|
| <b>XAUI Transmitter Jitter Generation</b>            |                  |      |      |       |
| Total transmitter jitter (T <sub>TJ</sub> )          | 3125             | –    | 0.35 | UI    |
| <b>XAUI Receiver High Frequency Jitter Tolerance</b> |                  |      |      |       |
| Total receiver jitter tolerance                      | 3125             | 0.65 | –    | UI    |

Table 77: PCI Express Protocol Characteristics (GTH Transceivers)<sup>(1)</sup>

| Standard                                             | Description                                   |                  | Line Rate (Mb/s) | Min    | Max   | Units |
|------------------------------------------------------|-----------------------------------------------|------------------|------------------|--------|-------|-------|
| PCI Express Transmitter Jitter Generation            |                                               |                  |                  |        |       |       |
| PCI Express Gen 1                                    | Total transmitter jitter                      |                  | 2500             | –      | 0.25  | UI    |
| PCI Express Gen 2                                    | Total transmitter jitter                      |                  | 5000             | –      | 0.25  | UI    |
| PCI Express Gen 3 <sup>(2)</sup>                     | Total transmitter jitter uncorrelated         |                  | 8000             | –      | 31.25 | ps    |
|                                                      | Deterministic transmitter jitter uncorrelated |                  |                  | –      | 12    | ps    |
| PCI Express Receiver High Frequency Jitter Tolerance |                                               |                  |                  |        |       |       |
| PCI Express Gen 1                                    | Total receiver jitter tolerance               |                  | 2500             | 0.65   | –     | UI    |
| PCI Express Gen 2 <sup>(3)</sup>                     | Receiver inherent timing error                |                  | 5000             | 0.40   | –     | UI    |
|                                                      | Receiver inherent deterministic timing error  |                  |                  | 0.30   | –     | UI    |
| PCI Express Gen 3 <sup>(2)</sup>                     | Receiver sinusoidal jitter tolerance          | 0.03 MHz–1.0 MHz | 8000             | 1.00   | –     | UI    |
|                                                      |                                               | 1.0 MHz–10 MHz   |                  | Note 4 | –     | UI    |
|                                                      |                                               | 10 MHz–100 MHz   |                  | 0.10   | –     | UI    |

### Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.