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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	37950
Number of Logic Elements/Cells	485760
Total RAM Bits	37969920
Number of I/O	700
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1761-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx485t-2ffg1761c

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX/GTH transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to $0.3 \times T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to $0.3 \times T_{VCCINT}$ (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: SelectIO DC Input and Output Levels⁽¹⁾⁽²⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8	-8
HSTL_I_12	-0.300	$V_{REF} - 0.080$	$V_{REF} + 0.080$	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	6.3	-6.3
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8	-8
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16	-16
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16	-16
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% V_{CCO}	80% V_{CCO}	0.1	-0.1
LVC MOS12	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS15, LVDCI_15	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVC MOS18, LVDCI_18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS25	-0.300	0.700	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 6	Note 6
LVC MOS33	-0.300	0.800	2.000	3.450	0.400	$V_{CCO} - 0.400$	Note 6	Note 6
LV TTL	-0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	-0.300	20% V_{CCO}	80% V_{CCO}	$V_{CCO} + 0.300$	10% V_{CCO}	90% V_{CCO}	0.1	-0.1
PCI33_3	-0.400	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.500$	10% V_{CCO}	90% V_{CCO}	1.5	-0.5
SSTL12	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	14.25	-14.25
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.0	-13.0
SSTL135_R	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.9	-8.9
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.0	-13.0
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.9	-8.9
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8	-8
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.4	-13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)).

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and **Table 20** (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVTTTL_S4	1.31	1.42	1.64	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVTTTL_S8	1.31	1.42	1.64	3.50	3.64	3.73	4.26	4.50	4.72	ns
LVTTTL_S12	1.31	1.42	1.64	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVTTTL_S16	1.31	1.42	1.64	3.03	3.17	3.26	3.79	4.03	4.25	ns
LVTTTL_S24	1.31	1.42	1.64	3.25	3.39	3.48	4.01	4.25	4.47	ns
LVTTTL_F4	1.31	1.42	1.64	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVTTTL_F8	1.31	1.42	1.64	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVTTTL_F12	1.31	1.42	1.64	2.69	2.82	2.92	3.45	3.68	3.91	ns
LVTTTL_F16	1.31	1.42	1.64	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVTTTL_F24	1.31	1.42	1.64	2.41	2.64	2.89	3.17	3.50	3.88	ns
LVDS_25 ⁽¹⁾	0.64	0.68	0.80	1.36	1.47	1.55	2.12	2.33	2.54	ns
MINI_LVDS_25	0.68	0.70	0.79	1.36	1.47	1.55	2.12	2.33	2.54	ns
BLVDS_25 ⁽¹⁾	0.65	0.69	0.80	1.83	2.02	2.20	2.59	2.88	3.19	ns
RSDS_25 (point to point) ⁽¹⁾	0.63	0.68	0.79	1.36	1.48	1.55	2.12	2.34	2.54	ns
PPDS_25 ⁽¹⁾	0.65	0.69	0.80	1.36	1.49	1.58	2.12	2.35	2.57	ns
TMDS_33 ⁽¹⁾	0.72	0.76	0.86	1.43	1.54	1.60	2.19	2.40	2.59	ns
PCI33_3 ⁽¹⁾	1.28	1.41	1.65	2.71	3.08	3.52	3.47	3.94	4.51	ns
HSUL_12	0.63	0.64	0.71	1.77	1.90	2.00	2.53	2.76	2.99	ns
DIFF_HSUL_12	0.58	0.61	0.70	1.55	1.68	1.78	2.31	2.54	2.77	ns
HSTL_I_S	0.61	0.64	0.73	1.55	1.69	1.80	2.31	2.55	2.79	ns
HSTL_II_S	0.61	0.64	0.73	1.21	1.34	1.43	1.97	2.20	2.42	ns
HSTL_I_18_S	0.64	0.67	0.76	1.28	1.39	1.45	2.04	2.25	2.44	ns
HSTL_II_18_S	0.64	0.67	0.76	1.18	1.31	1.40	1.94	2.17	2.39	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	1.42	1.54	1.61	2.18	2.40	2.60	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	1.15	1.24	1.27	1.91	2.10	2.26	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	1.27	1.38	1.43	2.03	2.24	2.42	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	1.14	1.23	1.26	1.90	2.09	2.25	ns
HSTL_I_F	0.61	0.64	0.73	1.10	1.19	1.23	1.86	2.05	2.22	ns

Input/Output Logic Switching Characteristics

Table 22: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{ICE1CK} /T _{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	ns
T _{ISRCK} /T _{ICKSR}	SR pin setup/hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	ns
T _{IDOCKE2} /T _{IOCKDE2}	D pin setup/hold with respect to CLK without delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	ns
T _{IDOCKDE2} /T _{IOCKDDE2}	DDL _Y pin setup/hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	ns
T _{IDOCKE3} /T _{IOCKDE3}	D pin setup/hold with respect to CLK without delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	ns
T _{IDOCKDE3} /T _{IOCKDDE3}	DDL _Y pin setup/hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	ns
Combinatorial					
T _{IDIE2}	D pin to O pin propagation delay, no delay (HP I/O banks only)	0.09	0.10	0.12	ns
T _{IDIDE2}	DDL _Y pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	ns
T _{IDIE3}	D pin to O pin propagation delay, no delay (HR I/O banks only)	0.09	0.10	0.12	ns
T _{IDIDE3}	DDL _Y pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	ns
Sequential Delays					
T _{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without delay (HP I/O banks only)	0.36	0.39	0.45	ns
T _{IDLODE2}	DDL _Y pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	ns
T _{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without delay (HR I/O banks only)	0.36	0.39	0.45	ns
T _{IDLODE3}	DDL _Y pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	ns
T _{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	ns
T _{RQ_ILOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	ns
T _{GSRQ_ILOGICE2}	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
T _{RQ_ILOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	ns
T _{GSRQ_ILOGICE3}	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
T _{RPW_ILOGICE2}	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	ns, Min
T _{RPW_ILOGICE3}	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	ns, Min

Table 23: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{ODCK} /T _{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.45/−0.13	0.50/−0.13	0.58/−0.13	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T _{OSRCK} /T _{OCKSR}	SR pin setup/hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.49/−0.16	0.56/−0.16	0.68/−0.16	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Combinatorial					
T _{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	ns
Sequential Delays					
T _{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	ns
T _{RQ_OLOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	ns
T _{GSRQ_OLOGICE2}	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
T _{RQ_OLOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	ns
T _{GSRQ_OLOGICE3}	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
T _{RPW_OLOGICE2}	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	ns, Min
T _{RPW_OLOGICE3}	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	ns, Min

Input/Output Delay Switching Characteristics

Table 26: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IDELAYCTRL					
T _{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.22	3.22	3.22	μs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	MHz
	Attribute REFCLK frequency = 300.0 ⁽¹⁾	300	300	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum reset pulse width	52.00	52.00	52.00	ns
IDELAY/ODELAY					
T _{IDELAYRESOLUTION}	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F _{REF})			ps
T _{IDELAYPAT_JIT} and T _{ODELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽³⁾	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽⁴⁾	±9	±9	±9	ps per tap
T _{IDELAY_CLK_MAX} / T _{ODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY/ODELAY	800	800	710	MHz
T _{IDCCK_CE} / T _{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	ns
T _{ODCCK_CE} / T _{ODCKC_CE}	CE pin setup/hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	ns
T _{IDCCK_INC} / T _{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	ns
T _{ODCCK_INC} / T _{ODCKC_INC}	INC pin setup/hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	ns
T _{IDCCK_RST} / T _{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	ns
T _{ODCCK_RST} / T _{ODCKC_RST}	RST pin setup/hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	ns
T _{IDDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	ps
T _{ODDO_ODATAIN}	Propagation delay through ODELAY	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

Table 27: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IO_FIFO Clock to Out Delays					
T _{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags	0.59	0.62	0.81	ns
Setup/Hold					
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.43/−0.01	0.47/−0.01	0.53/−0.01	ns
T _{IFFCK_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.39/−0.01	0.43/−0.01	0.50/−0.01	ns
T _{OFFCK_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	ns
Minimum Pulse Width					
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
Maximum Frequency					
F _{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	MHz

Table 31: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Maximum Frequency					
F _{MAX_BRAM_WF_NC}	Block RAM (Write first and No change modes) When not in SDP RF mode	601.32	543.77	458.09	MHz
F _{MAX_BRAM_RF_PERFORMANCE}	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601.32	543.77	458.09	MHz
F _{MAX_BRAM_RF_DELAYED_WRITE}	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528.26	477.33	400.80	MHz
F _{MAX_CAS_WF_NC}	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551.27	493.83	408.00	MHz
F _{MAX_CAS_RF_PERFORMANCE}	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551.27	493.83	408.00	MHz
F _{MAX_CAS_RF_DELAYED_WRITE}	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478.24	427.35	350.88	MHz
F _{MAX_FIFO}	FIFO in all modes without ECC	601.32	543.77	458.09	MHz
F _{MAX_ECC}	Block RAM and FIFO in ECC configuration	484.26	430.85	351.12	MHz

Notes:

1. The timing report shows all of these parameters as $T_{\text{RCKO_DO}}$.
2. $T_{\text{RCKO_DOR}}$ includes $T_{\text{RCKO_DOW}}$, $T_{\text{RCKO_DOPR}}$, and $T_{\text{RCKO_DOPW}}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with $\text{DO_REG} = 0$.
4. $T_{\text{RCKO_DO}}$ includes $T_{\text{RCKO_DOP}}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with $\text{DO_REG} = 1$.
6. $T_{\text{RCKO_FLAGS}}$ includes the following parameters: $T_{\text{RCKO_AEMPTY}}$, $T_{\text{RCKO_AFULL}}$, $T_{\text{RCKO_EMPTY}}$, $T_{\text{RCKO_FULL}}$, $T_{\text{RCKO_RDERR}}$, $T_{\text{RCKO_WRERR}}$.
7. $T_{\text{RCKO_POINTERS}}$ includes both $T_{\text{RCKO_RDCOUNT}}$ and $T_{\text{RCKO_WRCOUNT}}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{\text{RCO_FLAGS}}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$T_{\text{DSPDO_A_P}}$	A input to P output not using multiplier	1.30	1.48	1.76	ns
$T_{\text{DSPDO_C_P}}$	C input to P output	1.13	1.30	1.55	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
$T_{\text{DSPDO_}\{A; B\}_ \{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	ns
$T_{\text{DSPDO_}\{A, B\}_ \text{CARRYCASCOUT_MULT}}$	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	ns
$T_{\text{DSPDO_D_CARRYCASCOUT_MULT}}$	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	ns
$T_{\text{DSPDO_}\{A, B\}_ \text{CARRYCASCOUT}}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	ns
$T_{\text{DSPDO_C_CARRYCASCOUT}}$	C input to CARRYCASCOUT output	1.34	1.53	1.83	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
$T_{\text{DSPDO_ACIN_P_MULT}}$	ACIN input to P output using multiplier	3.09	3.55	4.24	ns
$T_{\text{DSPDO_ACIN_P}}$	ACIN input to P output not using multiplier	1.16	1.33	1.59	ns
$T_{\text{DSPDO_ACIN_ACOUT}}$	ACIN input to ACOUT output	0.32	0.37	0.45	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT_MULT}}$	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT}}$	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	ns
$T_{\text{DSPDO_PCIN_P}}$	PCIN input to P output	0.94	1.08	1.29	ns
$T_{\text{DSPDO_PCIN_CARRYCASCOUT}}$	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	ns
Clock to Outs from Output Register Clock to Output Pins					
$T_{\text{DSPCKO_P_PREG}}$	CLK PREG to P output	0.33	0.35	0.39	ns
$T_{\text{DSPCKO_CARRYCASCOUT_PREG}}$	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
$T_{\text{DSPCKO_P_MREG}}$	CLK MREG to P output	1.42	1.64	1.96	ns
$T_{\text{DSPCKO_CARRYCASCOUT_MREG}}$	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	ns
$T_{\text{DSPCKO_P_ADREG_MULT}}$	CLK ADREG to P output using multiplier	2.30	2.63	3.13	ns
$T_{\text{DSPCKO_CARRYCASCOUT_ADREG_MULT}}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	ns
Clock to Outs from Input Register Clock to Output Pins					
$T_{\text{DSPCKO_P_AREG_MULT}}$	CLK AREG to P output using multiplier	3.34	3.83	4.55	ns
$T_{\text{DSPCKO_P_BREG}}$	CLK BREG to P output not using multiplier	1.39	1.59	1.88	ns
$T_{\text{DSPCKO_P_CREG}}$	CLK CREG to P output not using multiplier	1.43	1.64	1.95	ns
$T_{\text{DSPCKO_P_DREG_MULT}}$	CLK DREG to P output using multiplier	3.32	3.80	4.51	ns

Clock Buffers and Networks

Table 33: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$T_{BCCCK_CE}/T_{BCCCK_CE}^{(1)}$	CE pins setup/hold	0.12/0.30	0.14/0.38	0.26/0.38	ns
$T_{BCCCK_S}/T_{BCCCK_S}^{(1)}$	S pins setup/hold	0.12/0.30	0.14/0.38	0.26/0.38	ns
$T_{BCKO_O}^{(2)}$	BUFGCTRL delay from I/O to O	0.08	0.10	0.12	ns
Maximum Frequency					
F_{MAX_BUFG}	Global clock tree (BUFG)	741.00	710.00	625.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCCK_S} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BCKO_O} (BUFG delay from I/O to O) values are the same as T_{BCKO_O} values.

Table 34: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BIOCKO_O}	Clock to out delay from I to O	1.04	1.14	1.32	ns
Maximum Frequency					
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800.00	800.00	710.00	MHz

Table 35: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BRCKO_O}	Clock to out delay from I to O	0.60	0.65	0.77	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.30	0.32	0.38	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.71	0.75	0.96	ns
Maximum Frequency					
$F_{MAX_BUFR}^{(1)}$	Regional clock tree (BUFR)	600.00	540.00	450.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 36: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	ns
$T_{BHCKCK_CE}/T_{BHCKCK_CE}$	CE pin setup and hold	0.20/0.16	0.23/0.20	0.38/0.21	ns
Maximum Frequency					
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	741.00	710.00	625.00	MHz

Table 63: CEI-6G and CEI-11G Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter ⁽²⁾	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽²⁾	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 64: SFP+ Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40 ⁽¹⁾	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40 ⁽¹⁾	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 65: CPRI Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see [Table 64](#).

GTH Transceiver Specifications

GTH Transceiver DC Input and Output Levels

Table 66 summarizes the DC specifications of the GTH transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further details.

Table 66: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Absolute input voltage	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
DV _{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to 1010	–	–	800	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled	Equation based	V _{MGTAVTT} – DV _{PPOUT} /4			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based	V _{MGTAVTT} – DV _{PPOUT} /2			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)), and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

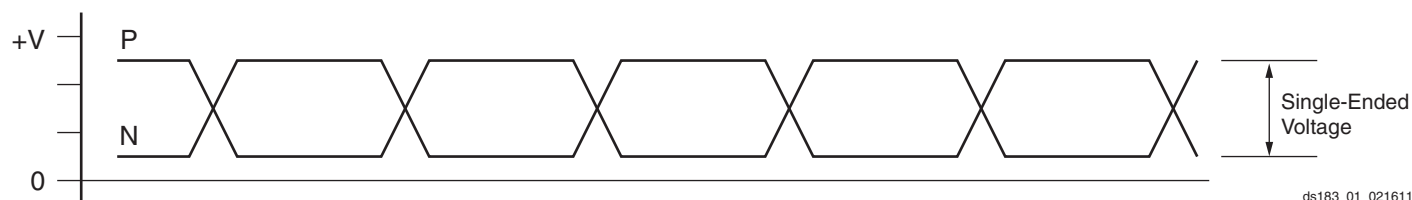


Figure 4: Single-Ended Peak-to-Peak Voltage

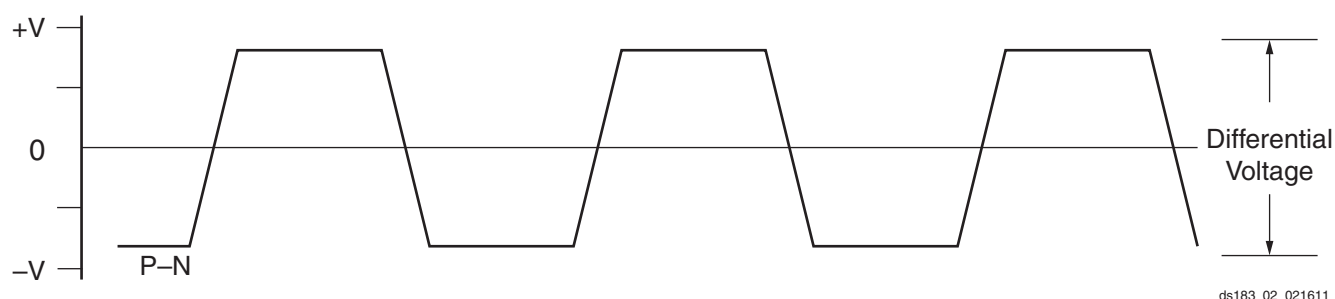


Figure 5: Differential Peak-to-Peak Voltage

Table 73: GTH Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
TJ _{8.0_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
DJ _{8.0_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
TJ _{6.6_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	6.6 Gb/s	–	–	0.28	UI
DJ _{6.6_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{6.6_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
DJ _{6.6_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
DJ _{5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
DJ _{4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.75}	Total jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	–	–	0.30	UI
DJ _{3.75}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.2	UI
DJ _{3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.1	UI
TJ _{3.20L}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁶⁾	–	–	0.32	UI
DJ _{3.20L}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
TJ _{2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁷⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.08	UI
TJ _{1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁸⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
TJ ₅₀₀	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s	–	–	0.1	UI
DJ ₅₀₀	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTH Quads).
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 74: GTH Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTHRX}	Serial data rate	RX oversampler not enabled	0.500	–	F _{GTHMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELEC_IDLE to respond to loss or restoration of data		–	10	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm
RX _{RL}	Run length (CID)		–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{13.1}	Sinusoidal jitter (QPLL) ⁽³⁾	13.1 Gb/s	0.3	–	–	UI
JT_SJ _{12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.3	–	–	UI
JT_SJ _{11.3}	Sinusoidal jitter (QPLL) ⁽³⁾	11.3 Gb/s	0.3	–	–	UI
JT_SJ _{10.32_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{10.32_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.8}	Sinusoidal jitter (QPLL) ⁽³⁾	9.8 Gb/s	0.3	–	–	UI
JT_SJ _{8.0_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	8.0 Gb/s	0.44	–	–	UI
JT_SJ _{8.0_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	8.0 Gb/s	0.42	–	–	UI
JT_SJ _{6.6_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	6.6 Gb/s	0.48	–	–	UI
JT_SJ _{6.6_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal jitter (CPLL) ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{3.2L}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁵⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁷⁾	0.5	–	–	UI
JT_SJ ₅₀₀	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
JT_TJSE _{6.6}		6.6 Gb/s	0.70	–	–	UI
JT_SJSE _{3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.1	–	–	UI
JT_SJSE _{6.6}		6.6 Gb/s	0.1	–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e^{–12}.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

Table 78: CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter ⁽²⁾	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽²⁾	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 79: SFP+ Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40 ⁽¹⁾	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40 ⁽¹⁾	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 80: CPRI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	—	0.35	UI
	1228.8	—	0.35	UI
	2457.6	—	0.35	UI
	3072.0	—	0.35	UI
	4915.2	—	0.3	UI
	6144.0	—	0.3	UI
	9830.4	—	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	—	UI
	1228.8	0.65	—	UI
	2457.6	0.65	—	UI
	3072.0	0.65	—	UI
	4915.2	0.95	—	UI
	6144.0	0.95	—	UI
	9830.4	Note 1	—	UI

Notes:

1. Tested per SFP+ specification, see Table 79.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 81: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	500.00	500.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz

Table 82: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference⁽⁵⁾						
External Reference	V _{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V _{REFP} pin to AGND, T _j = -40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for new BitGen option XADCEnhancedLinearity = ON.
- For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
- For a detailed description, see the Timing chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
- Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 83: Configuration Switching Characteristics

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program latency		5	5	5	ms, Max
T _{POR} ⁽¹⁾	Power-on reset (50ms ramp rate time)		10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1ms ramp rate time)		10/35	10/35	10/35	ms, Min/Max
T _{PROGRAM}	Program pulse width		250	250	250	ns, Min
CCLK Output (Master Mode)						
T _{ICCK}	Master CCLK output delay		150	150	150	ns, Min
T _{MCCKL}	Master CCLK clock Low time duty cycle		40/60	40/60	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle		40/60	40/60	40/60	%, Min/Max
F _{MCCK}	Master CCLK frequency		100	100	100	MHz, Max
	Master CCLK frequency for AES encrypted x16		50	50	50	MHz, Max
F _{MCCK_START}	Master CCLK frequency at start of configuration		3	3	3	MHz, Typ
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK.		±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time		2.5	2.5	2.5	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time		2.5	2.5	2.5	ns, Min
F _{SCCK}	Slave CCLK frequency		100	100	100	MHz, Max
EMCCLK Input (Master Mode)						
T _{EMCCKL}	External master CCLK Low time		2.5	2.5	2.5	ns, Min
T _{EMCCKH}	External master CCLK High time		2.5	2.5	2.5	ns, Min
F _{EMCCK}	External master CCLK frequency		100	100	100	MHz, Max
Internal Configuration Access Port						
F _{ICAPCK}	Internal configuration access port (ICAPE2)		100.00	100.00	100.00	MHz, Max

