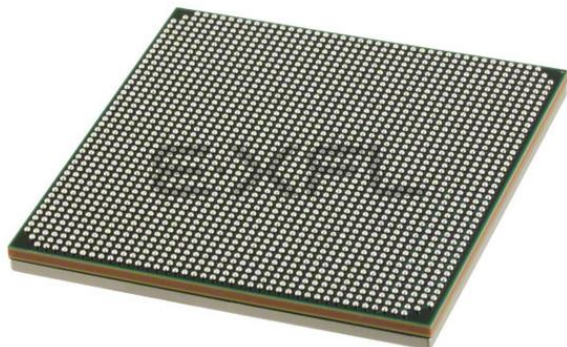




Welcome to [E-XFL.COM](#)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	37950
Number of Logic Elements/Cells	485760
Total RAM Bits	37969920
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1927-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx485t-2ffg1927i

Table 5: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks⁽¹⁾⁽²⁾

AC Voltage Overshoot	% of UI @ -40°C to 100°C	AC Voltage Undershoot	% of UI @ -40°C to 100°C
$V_{CCO} + 0.55$	100	-0.55	100
$V_{CCO} + 0.60$	50.0	-0.60	50.0
$V_{CCO} + 0.65$	50.0	-0.65	50.0
$V_{CCO} + 0.70$	47.0	-0.70	50.0
$V_{CCO} + 0.75$	21.2	-0.75	50.0
$V_{CCO} + 0.80$	9.71	-0.80	50.0
$V_{CCO} + 0.85$	4.51	-0.85	28.4
$V_{CCO} + 0.90$	2.12	-0.90	12.7
$V_{CCO} + 0.95$	1.01	-0.95	5.79

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μ s.

Table 6: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7V585T	1483	1483	1483	mA
		XC7V2000T	N/A	3756	3756	mA
		XC7VX330T	1012	1012	1012	mA
		XC7VX415T	1324	1324	1324	mA
		XC7VX485T	1578	1578	1578	mA
		XC7VX550T	2214	2214	2214	mA
		XC7VX690T	2214	2214	2214	mA
		XC7VX980T	N/A	2580	2580	mA
		XC7VX1140T	N/A	3448	3448	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7V585T	1	1	1	mA
		XC7V2000T	N/A	1	1	mA
		XC7VX330T	1	1	1	mA
		XC7VX415T	1	1	1	mA
		XC7VX485T	1	1	1	mA
		XC7VX550T	1	1	1	mA
		XC7VX690T	1	1	1	mA
		XC7VX980T	N/A	1	1	mA
		XC7VX1140T	N/A	1	1	mA

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX/GTH transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to $0.3 \times T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to $0.3 \times T_{VCCINT}$ (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

LVDS DC Specifications (LVDS_25)

The LVDS standard is available in the HR I/O banks.

Table 12: LVDS_25 DC Specifications⁽¹⁾

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks.

Table 13: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		1.710	1.800	1.890	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ± 350 mV	0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

Table 18: Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator⁽¹⁾⁽²⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO}	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
4:1 Memory Controllers						
DDR3	HP	2.0V	1866	1866	1600	Mb/s
	HP	1.8V	1600	1333	1066	Mb/s
	HR	N/A	1066	1066	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	Mb/s
	HP	1.8V	1333	1066	800	Mb/s
	HR	N/A	800	800	667	Mb/s
DDR2	HP	2.0V	800	800	800	Mb/s
	HP	1.8V	800	800	800	Mb/s
	HR	N/A	800	800	800	Mb/s
RLDRAM III	HP	2.0V	800	667	667	MHz
	HP	1.8V	550	500	450	MHz
	HR	N/A	N/A			
2:1 Memory Controllers						
DDR3	HP	2.0V	1066	1066	800	Mb/s
	HP	1.8V	1066	1066	800	Mb/s
	HR	N/A	1066	1066	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	Mb/s
	HP	1.8V	1066	1066	800	Mb/s
	HR	N/A	800	800	667	Mb/s
DDR2	HP	2.0V	800	800	800	Mb/s
	HP	1.8V				
	HR	N/A				
QDR II+(3)	HP	2.0V	550	500	450	MHz
	HP	1.8V				
	HR	N/A	500	450	400	MHz
RLDRAM II	HP	2.0V	533	500	450	MHz
	HP	1.8V				
	HR	N/A				
LPDDR2	HP	2.0V	667	667	667	Mb/s
	HP	1.8V	667	667	667	Mb/s
	HR	N/A	667	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* ([UG586](#)).
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 23: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{ODCK} /T _{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.45/−0.13	0.50/−0.13	0.58/−0.13	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T _{OSRCK} /T _{OCKSR}	SR pin setup/hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.49/−0.16	0.56/−0.16	0.68/−0.16	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Combinatorial					
T _{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	ns
Sequential Delays					
T _{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	ns
T _{RQ_OLOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	ns
T _{GSRQ_OLOGICE2}	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
T _{RQ_OLOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	ns
T _{GSRQ_OLOGICE3}	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
T _{RPW_OLOGICE2}	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	ns, Min
T _{RPW_OLOGICE3}	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 24: ISERDES Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold for Control Lines					
$T_{ISCK_BITSLIP}/T_{ISCK_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	ns
$T_{ISCK_CE} / T_{ISCK_CE}^{(2)}$	CE pin setup/hold with respect to CLK (for CE1)	0.39/−0.02	0.44/−0.02	0.63/−0.02	ns
$T_{ISCK_CE2} / T_{ISCK_CE2}^{(2)}$	CE pin setup/hold with respect to CLKDIV (for CE2)	−0.12/0.29	−0.12/0.31	−0.12/0.35	ns
Setup/Hold for Data Lines					
T_{ISDCK_D}/T_{ISCKD_D}	D pin setup/hold with respect to CLK	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_DDL}/T_{ISCKD_DDL}$	DDL pin setup/hold with respect to CLK (using IDELAY) ⁽¹⁾	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_D_DDR} / T_{ISCKD_D_DDR}$	D pin setup/hold with respect to CLK at DDR mode	−0.02/0.11	−0.02/0.12	−0.02/0.15	ns
$T_{ISDCK_DDL_DDR}/T_{ISCKD_DDL_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾	0.11/0.11	0.12/0.12	0.15/0.15	ns
Sequential Delays					
T_{ISCO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCK_CE2} and T_{ISCK_CE2} are reported as T_{ISCK_CE}/T_{ISCK_CE} in the timing report.

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$T_{\text{DSPDO_A_P}}$	A input to P output not using multiplier	1.30	1.48	1.76	ns
$T_{\text{DSPDO_C_P}}$	C input to P output	1.13	1.30	1.55	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
$T_{\text{DSPDO_}\{A; B\}_ \{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	ns
$T_{\text{DSPDO_}\{A, B\}_ \text{CARRYCASCOUT_MULT}}$	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	ns
$T_{\text{DSPDO_D_CARRYCASCOUT_MULT}}$	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	ns
$T_{\text{DSPDO_}\{A, B\}_ \text{CARRYCASCOUT}}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	ns
$T_{\text{DSPDO_C_CARRYCASCOUT}}$	C input to CARRYCASCOUT output	1.34	1.53	1.83	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
$T_{\text{DSPDO_ACIN_P_MULT}}$	ACIN input to P output using multiplier	3.09	3.55	4.24	ns
$T_{\text{DSPDO_ACIN_P}}$	ACIN input to P output not using multiplier	1.16	1.33	1.59	ns
$T_{\text{DSPDO_ACIN_ACOUT}}$	ACIN input to ACOUT output	0.32	0.37	0.45	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT_MULT}}$	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT}}$	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	ns
$T_{\text{DSPDO_PCIN_P}}$	PCIN input to P output	0.94	1.08	1.29	ns
$T_{\text{DSPDO_PCIN_CARRYCASCOUT}}$	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	ns
Clock to Outs from Output Register Clock to Output Pins					
$T_{\text{DSPCKO_P_PREG}}$	CLK PREG to P output	0.33	0.35	0.39	ns
$T_{\text{DSPCKO_CARRYCASCOUT_PREG}}$	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
$T_{\text{DSPCKO_P_MREG}}$	CLK MREG to P output	1.42	1.64	1.96	ns
$T_{\text{DSPCKO_CARRYCASCOUT_MREG}}$	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	ns
$T_{\text{DSPCKO_P_ADREG_MULT}}$	CLK ADREG to P output using multiplier	2.30	2.63	3.13	ns
$T_{\text{DSPCKO_CARRYCASCOUT_ADREG_MULT}}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	ns
Clock to Outs from Input Register Clock to Output Pins					
$T_{\text{DSPCKO_P_AREG_MULT}}$	CLK AREG to P output using multiplier	3.34	3.83	4.55	ns
$T_{\text{DSPCKO_P_BREG}}$	CLK BREG to P output not using multiplier	1.39	1.59	1.88	ns
$T_{\text{DSPCKO_P_CREG}}$	CLK CREG to P output not using multiplier	1.43	1.64	1.95	ns
$T_{\text{DSPCKO_P_DREG_MULT}}$	CLK DREG to P output using multiplier	3.32	3.80	4.51	ns

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Clock to Outs from Input Register Clock to Cascading Output Pins					
T_DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	ns
T_DSPCKO_CARRYCASCOUT_{AREG, BREG}_MULT	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	ns
T_DSPCKO_CARRYCASCOUT_ BREG	CLK (BREG) to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	ns
T_DSPCKO_CARRYCASCOUT_ DREG_MULT	CLK (DREG) to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	ns
T_DSPCKO_CARRYCASCOUT_ CREG	CLK (CREG) to CARRYCASCOUT output	1.64	1.88	2.23	ns
Maximum Frequency					
F_MAX	With all registers used	741.84	650.20	547.95	MHz
F_MAX_PATDET	With pattern detector	627.35	549.75	463.61	MHz
F_MAX_MULT_NOMREG	Two register multiply without MREG	412.20	360.75	303.77	MHz
F_MAX_MULT_NOMREG_PATDET	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	MHz
F_MAX_PREADD_MULT_NOADREG	Without ADREG	468.82	408.66	342.70	MHz
F_MAX_PREADD_MULT_NOADREG_PATDET	Without ADREG with pattern detect	468.82	408.66	342.58	MHz
F_MAX_NOPIPELINEREG	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	MHz
F_MAX_NOPIPELINEREG_PATDET	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	MHz

Table 37: Duty Cycle Distortion and Clock Tree Skew

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
T _{DCD_CLK}	Global clock tree duty cycle distortion ⁽¹⁾	All	0.20	0.20	0.20	ns
T _{CKSKEW}	Global clock tree skew ⁽²⁾	XC7V585T	0.75	0.91	0.98	ns
		XC7V2000T	N/A	0.39	0.39	ns
		XC7VX330T	0.60	0.74	0.79	ns
		XC7VX415T	0.76	0.84	0.91	ns
		XC7VX485T	0.60	0.74	0.79	ns
		XC7VX550T	0.73	0.88	0.96	ns
		XC7VX690T	0.73	0.88	0.96	ns
		XC7VX980T	N/A	0.91	0.98	ns
		XC7VX1140T	N/A	0.39	0.39	ns
T _{DCD_BUFIN}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	ns
T _{BUFIOSKEW}	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	ns
T _{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip-flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements in a single SLR. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 38: MMCM Specification

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
MMCM_F _{INMAX}	Maximum input clock frequency	1066.00	933.00	800.00	MHz
MMCM_F _{INMIN}	Minimum input clock frequency	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max			
MMCM_F _{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	550.00	500.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical ⁽¹⁾	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical ⁽¹⁾	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs ⁽²⁾	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter	Note 3			
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision ⁽⁴⁾	0.20	0.20	0.20	ns

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 40: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T _{ICKOF}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7V585T	5.63	6.20	6.97	ns
		XC7V2000T	N/A	5.66	6.35	ns
		XC7VX330T	5.41	5.97	6.71	ns
		XC7VX415T	5.46	5.96	6.70	ns
		XC7VX485T	5.29	5.84	6.57	ns
		XC7VX550T	5.45	6.02	6.76	ns
		XC7VX690T	5.46	6.02	6.76	ns
		XC7VX980T	N/A	6.12	6.87	ns
		XC7VX1140T	N/A	5.59	6.28	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 41: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T _{ICKOFFAR}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7V585T	6.81	7.53	8.44	ns
		XC7V2000T	N/A	6.00	6.73	ns
		XC7VX330T	6.31	6.97	7.83	ns
		XC7VX415T	6.36	6.90	7.69	ns
		XC7VX485T	6.20	6.86	7.69	ns
		XC7VX550T	6.66	7.37	8.27	ns
		XC7VX690T	6.69	7.37	8.27	ns
		XC7VX980T	N/A	7.47	8.37	ns
		XC7VX1140T	N/A	5.93	6.65	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 45: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks (only)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾						
T _{PSFD} / T _{PHFD}	Full delay (legacy delay or default delay) Global clock Input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7V585T	3.12/−0.37	3.19/−0.37	3.42/−0.37	ns
		XC7V2000T	N/A	N/A	N/A	ns
		XC7VX330T	2.90/−0.31	2.96/−0.31	3.16/−0.31	ns
		XC7VX415T	N/A	N/A	N/A	ns
		XC7VX485T	N/A	N/A	N/A	ns
		XC7VX550T	N/A	N/A	N/A	ns
		XC7VX690T	N/A	N/A	N/A	ns
		XC7VX980T	N/A	N/A	N/A	ns
		XC7VX1140T	N/A	N/A	N/A	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch

Table 46: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾⁽²⁾						
T _{PSMMCMCC} / T _{PHMMCMCC}	No delay clock-capable clock input and IFF ⁽³⁾ with MMCM	XC7V585T	2.71/−0.10	3.00/−0.10	3.33/−0.10	ns
		XC7V2000T	N/A	2.60/−0.24	2.87/−0.24	ns
		XC7VX330T	2.58/−0.15	2.87/−0.15	3.18/−0.15	ns
		XC7VX415T	2.73/0.01	3.03/0.01	3.36/0.01	ns
		XC7VX485T	2.58/−0.15	2.87/−0.15	3.18/−0.15	ns
		XC7VX550T	2.72/−0.09	3.01/−0.09	3.34/−0.09	ns
		XC7VX690T	2.72/0.01	3.01/0.01	3.34/0.01	ns
		XC7VX980T	N/A	3.01/−0.10	3.36/−0.10	ns
		XC7VX1140T	N/A	2.61/−0.24	2.88/−0.24	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 51 summarizes the DC specifications of the GTX transceivers in Virtex-7 T and XT FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476) for further details.

Table 51: GTX Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
V _{CMOUTDC}	DC common mode output voltage.	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–200	–	$V_{MGTAVTT}$	mV
V _{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT} = 1.2V$	–	$2/3 V_{MGTAVTT}$	–	mV
R _{IN}	Differential input resistance		–	100	–	Ω
C _{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476), and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

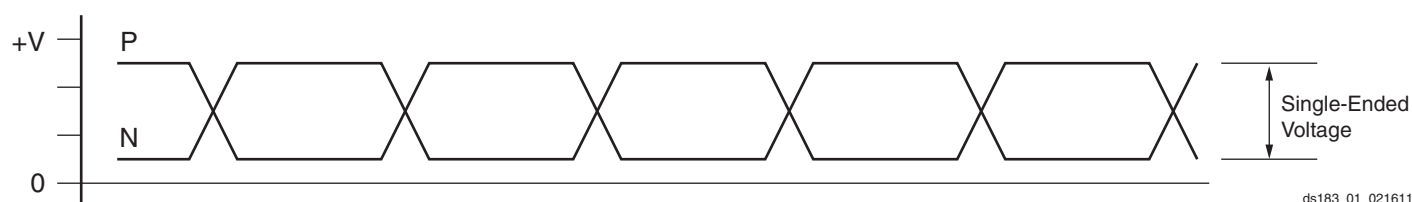


Figure 1: Single-Ended Peak-to-Peak Voltage

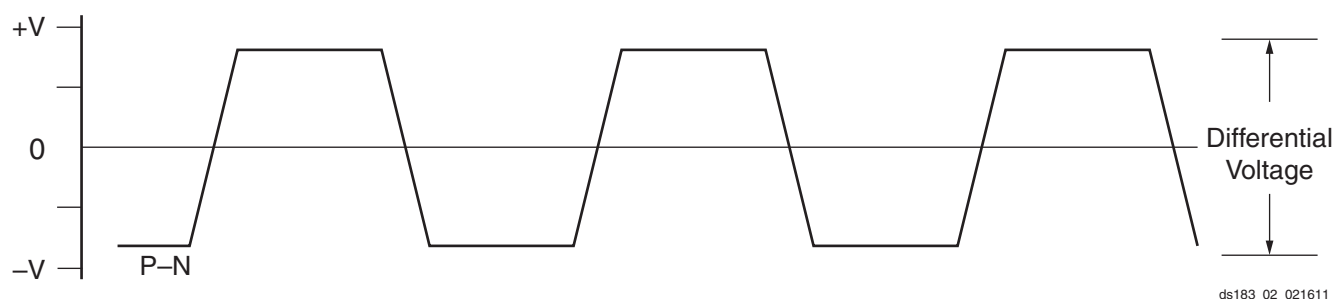


Figure 2: Differential Peak-to-Peak Voltage

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further details.

Table 52: GTX Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further information.

Table 53: GTX Transceiver Performance

Symbol	Description	Output Divider	Speed Grade			Units
			-3/-2G	-2/-2L	-1 ⁽¹⁾	
F _{GTXMAX} ⁽²⁾	Maximum GTX transceiver data rate		12.5	10.3125	8.0	Gb/s
F _{GTXMIN} ⁽²⁾	Minimum GTX transceiver data rate		0.500	0.500	0.500	Gb/s
F _{GTXCRANGE}	CPLL line rate range	1	3.2–6.6			Gb/s
		2	1.6–3.3			Gb/s
		4	0.8–1.65			Gb/s
		8	0.5–0.825			Gb/s
		16	N/A			Gb/s
F _{GTXQRANGE1}	QPLL line rate range 1	1	5.93–8.0	5.93–8.0	5.93–8.0	Gb/s
		2	2.965–4.0	2.965–4.0	2.965–4.0	Gb/s
		4	1.4825–2.0	1.4825–2.0	1.4825–2.0	Gb/s
		8	0.74125–1.0	0.74125–1.0	0.74125–1.0	Gb/s
		16	N/A	N/A	N/A	Gb/s
F _{GTXQRANGE2}	QPLL line rate range 2 ⁽³⁾	1	9.8–12.5	9.8–10.3125	N/A	Gb/s
		2	4.9–6.25	4.9–5.15625	N/A	Gb/s
		4	2.45–3.125	2.45–2.578125	N/A	Gb/s
		8	1.225–1.5625	1.225–1.2890625	N/A	Gb/s
		16	0.6125–0.78125	0.6125–0.64453125	N/A	Gb/s
F _{GCPLLRANGE}	GTX transceiver CPLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	GHz
F _{GQPLLRange1}	GTX transceiver QPLL frequency range 1		5.93–8.0	5.93–8.0	5.93–8.0	GHz
F _{GQPLLRange2}	GTX transceiver QPLL frequency range 2		9.8–12.5	9.8–10.3125	N/A	GHz

Notes:

- The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), requires a 4-byte internal data width for operation above 3.8 Gb/s.
- Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
- For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3/-2G	-2/-2L	-1	
F _{GTXDRPCLK}	GTXDRPCLK maximum frequency	175.01	175.01	156.25	MHz

Table 55: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

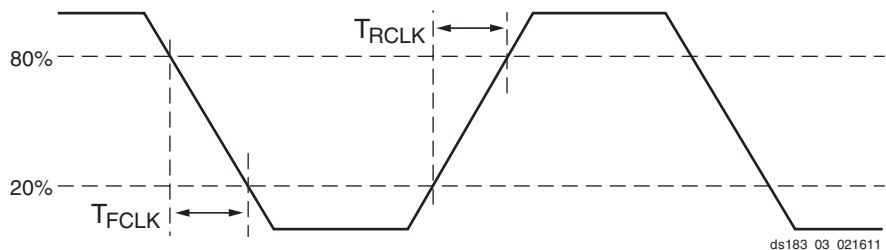


Figure 3: Reference Clock Timing Parameters

Table 56: GTX Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 57: GTX Transceiver User Clock Switching Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3/-2G ⁽³⁾	-2/-2L ⁽³⁾	-1 ⁽⁴⁾	
F _{TXOUT}	TXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F _{RXOUT}	RXOUTCLK maximum frequency			412.500	412.500	312.500	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F _{RXIN}	RXUSRCLK maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	390.625	322.266	250.000	MHz
F _{TXIN2}	TXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz
F _{RXIN2}	RXUSRCLK2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	390.625	322.266	250.000	MHz
		64-bit	64-bit	195.313	161.133	125.000	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L, and -2G, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s. For speed grade -1C with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.500	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	40	–	ps
T _{FTX}	TX fall time	80%–20%	–	40	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	140	ns
TJ _{12.5}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
DJ _{12.5}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{11.18}	Total jitter ⁽²⁾⁽⁴⁾	11.18 Gb/s	–	–	0.28	UI
DJ _{11.18}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{10.3125}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
DJ _{10.3125}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{9.953}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
DJ _{9.953}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{9.8}	Total jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	–	–	0.28	UI
DJ _{9.8}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{8.0}	Total jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	–	–	0.30	UI
DJ _{8.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.15	UI
TJ _{6.6_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	6.6 Gb/s	–	–	0.28	UI
DJ _{6.6_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI

Table 58: GTX Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
TJ _{6.6_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
DJ _{6.6_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
DJ _{5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
DJ _{4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.75}	Total jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	–	–	0.30	UI
DJ _{3.75}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
DJ _{3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
TJ _{3.20L}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁶⁾	–	–	0.32	UI
DJ _{3.20L}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
TJ _{2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁷⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.08	UI
TJ _{1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁸⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
TJ ₅₀₀	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s	–	–	0.10	UI
DJ ₅₀₀	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of $1e^{-12}$.
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the 7 Series FPGAs GTX/GTH Transceiver User Guide ([UG476](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: Gigabit Ethernet Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: XAUI Protocol Characteristics (GTX Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: PCI Express Protocol Characteristics (GTX Transceivers)⁽¹⁾

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 ⁽³⁾	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 73: GTH Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
TJ _{8.0_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
DJ _{8.0_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
TJ _{6.6_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	6.6 Gb/s	–	–	0.28	UI
DJ _{6.6_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{6.6_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
DJ _{6.6_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
DJ _{5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
DJ _{4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.75}	Total jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	–	–	0.30	UI
DJ _{3.75}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.2	UI
DJ _{3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.1	UI
TJ _{3.20L}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁶⁾	–	–	0.32	UI
DJ _{3.20L}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
TJ _{2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁷⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.08	UI
TJ _{1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁸⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
TJ ₅₀₀	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s	–	–	0.1	UI
DJ ₅₀₀	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTH Quads).
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of $1e^{-12}$.
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

GTH Transceiver Protocol Jitter Characteristics

For [Table 75](#) through [Table 80](#), the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) contains recommended settings for optimal usage of protocol specific characteristics.

Table 75: Gigabit Ethernet Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 76: XAUI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 77: PCI Express Protocol Characteristics (GTH Transceivers)⁽¹⁾

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 ⁽³⁾	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Revision History

The following table shows the revision history for this document.

Date	Version	Description
03/01/2011	1.0	Initial Xilinx release.
10/05/2011	1.1	Removed the XC7V285T, XC7V450T, and XC7V855T devices from the entire data sheet. Added the XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T, XC7VX980T, and XC7VX1140T devices to the entire data sheet. Replaced -1L with -2L throughout this data sheet. Added the extended temperature range discussion to page 1. Updated Min/Max values and removed Note 5 from Table 2. Clarified Power-On/Off Power Supply Sequencing power sequencing discussion including adding $T_{VCCO2VCCAUX}$ to Table 8. Added I_{CCAUX_IO} and I_{CCBRAM} to Table 6 and Table 7. Updated V_{ICM} in Table 12 and Table 13. Added Note 1 to Table 12. Updated Table 84 including adding Note 1. Added Table 13. Revised the reference clock maximum frequency (F_{GCLK}) in Table 55. Added Table 57. Added GTH Transceiver Specifications section. Removed erroneous instances of HSTL_III from Table 20. Removed the <i>I/O Standard Adjustment Measurement Methodology</i> section. Use IBIS for more accurate information and measurements. Updated $T_{IDELAYPAT_JIT}$ in Table 26. Added T_{AS}/T_{AH} to Table 28. Added $T_{RDCK_DI_WF_NC}/T_{RDCK_DI_WF_NC}$ and $T_{RDCK_DI_RF}/T_{RDCK_DI_RF}$ to Table 31. Completely updated the specifications in Table 83. Updated $MMCM_F_{INDUTY}$ and added $F_{INJITTER}$, $T_{OUTJITTER}$, and $T_{EXTFVAR}$ and Note 3 to Table 38. Updated the AC Switching Characteristics section. Updated the Table 50 package list. Updated the Notice of Disclaimer.
11/07/2011	1.2	Added -2G speed grade, where appropriate, throughout document. Revised the V_{OCM} specification in Table 12. Updated the AC Switching Characteristics based upon the ISE 13.3 v1.02 speed specification throughout document including Table 19 and Table 20. Added MMCM to the symbol names of a few specifications in Table 38 and PLL to the symbol names in Table 39. In Table 40 through Table 47, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 49.
02/13/2012	1.3	Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Added typical numbers to Table 3. Updated the notes in Table 6. Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to Table 8. Rearranged Table 9, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 10 and Table 11. Revised the specifications in Table 12 and Table 13. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the IO_FIFO Switching Characteristics table. Revised I_{CCADC} and updated Note 1 in Table 82. Revised DDR LVDS transmitter data width in Table 17. Updated the AC Switching Characteristics based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from Table 28 as they are no longer applicable. Updated specifications in Table 83. Updated Note 1 in Table 37. In the GTX Transceiver Specifications section: Revised V_{IN}, and added I_{DCIN} and I_{DCOUT} to Table 51. Updated and added notes to Table 53. In Table 55, revised F_{GCLK}, removed T_{PHASE}, and added T_{DLOCK}. Revised specifications and added Note 2 to Table 57. Added Table 58 and Table 59 along with GTX Transceiver Protocol Jitter Characteristics in Table 60 through Table 65.
05/23/2012	1.4	Reorganized entire data sheet including adding Table 44 and Table 48. Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Added values to Table 6 and Table 7. Updated Power-On/Off Power Supply Sequencing section with regards to GTX/GTH transceivers. Updated many parameters in Table 9, including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 11. Updated V_{OL} in Table 12. Updated Table 17 and removed notes 2 and 3. Updated Table 18. Updated the AC Switching Characteristics section based upon the ISE 14.1 v1.04 for the -3, -2, -2L (1.0V), -1, and v1.05 for the -2L (0.9V) speed specifications throughout the document. In Table 31, updated Reset Delays section including Note 10 and Note 11. Added data for T_{LOCK} and T_{DLOCK} in Table 55. Updated many of the XADC specifications in Table 82 and added Note 2. Updated and moved <i>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</i> section from Table 83 to Table 38 and Table 39.