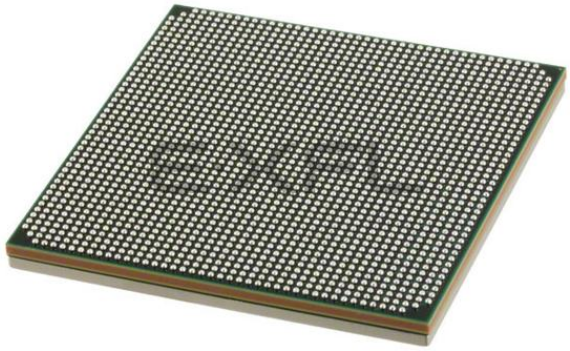
AMD Xilinx - XC7VX485T-2FFG1930I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	37950
Number of Logic Elements/Cells	485760
Total RAM Bits	37969920
Number of I/O	700
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1924-BBGA, FCBGA
Supplier Device Package	1930-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx485t-2ffg1930i

Table 1: **Absolute Maximum Ratings[1] *(Cont'd)***

Symbol	Description	Min	Max	Units
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the GTX/GTH transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
I_{DCIN}	DC input current for receiver input pins DC coupled $V_{MGTAVTT}$ = 1.2V	–	14	mA
I_{DCOUT}	DC output current for transmitter pins DC coupled $V_{MGTAVTT}$ = 1.2V	–	14	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies[6]	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies[6]	–	+260	°C
T_j	Maximum junction temperature[6]	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471).
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4 and Table 5.
5. See Table 10 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475).

Table 2: **Recommended Operating Conditions[1][2]**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}[3]	Internal supply voltage	0.97	1.00	1.03	V
	Internal supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical[4].	0.87	0.90	0.93	V
V_{CCBRAM}[3]	Block RAM supply voltage	0.97	1.00	1.03	V
	Block RAM supply voltage for -1C devices with voltage identification (VID) bit programmed to run at 0.9V typical[4].	0.87	0.90	1.03	V
V_{CCAUX}	Auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCO}[5][6]	Supply voltage for 3.3V HR I/O banks	1.14	–	3.465	V
	Supply voltage for 1.8V HP I/O banks	1.14	–	1.89	V
V_{CCAUX_IO}	Auxiliary supply voltage when set to 1.8V	1.71	1.80	1.89	V
	Auxiliary supply voltage when set to 2.0V	1.94	2.00	2.06	V
V_{IN}[7]	I/O input voltage	–0.20	–	V_{CCO} + 0.2	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33[8]	–0.20	–	2.625	V
I_{IN}[9]	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{CCBATT}[10]	Battery voltage	1.0	–	1.89	V

LVDS DC Specifications (LVDS_25)

The LVDS standard is available in the HR I/O banks.

Table 12: **LVDS_25 DC Specifications(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks.

Table 13: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		1.710	1.800	1.890	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ±350 mV	0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Virtex-7 T and XT device on a per speed grade basis.

Table 15: **Virtex-7 T and XT Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7V585T			-3, -2, -2L, -1
XC7V2000T	-2L, -2G		-2, -1
XC7VX330T			-3, -2, -2L, -1
XC7VX415T			-3, -2, -2L, -1
XC7VX485T			-3, -2, -2L, -1
XC7VX550T			-3, -2, -2L, -1
XC7VX690T			-3, -2, -2L, -1
XC7VX980T	-2, -2L, -1		
XC7VX1140T	-2, -2L, -2G, -1		

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 16 lists the production released Virtex-7 T and XT device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 16: **Virtex-7 T and XT Device Production Software and Speed Specification Release**

Device	Speed Grade Designations				
	-3	-2G	-2	-2L	-1
XC7V585T	Vivado 2012.4 v1.08 or ISE 14.2 v1.06	N/A	Vivado 2012.4 v1.08 or ISE 14.2 v1.06		
XC7V2000T	N/A		Vivado 2012.4 v1.07		Vivado 2012.4 v1.07
XC7VX330T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX415T		N/A			
XC7VX485T	Vivado 2012.4 v1.08 or ISE 14.2 v1.06	N/A	Vivado 2012.4 v1.08 or ISE 14.2 v1.06		
XC7VX550T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX690T	Vivado 2013.1 v1.08 or ISE 14.5 v1.08	N/A	Vivado 2013.1 v1.08 or ISE 14.5 v1.08		
XC7VX980T	N/A	N/A			
XC7VX1140T	N/A				

Notes:

1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-7 T and XT devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 12. In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 17: **Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR	710	710	625	Mb/s
	HP	710	710	625	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR	1250	1250	950	Mb/s
	HP	1600	1400	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and Table 20 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVTTL_S4	1.31	1.42	1.64	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVTTL_S8	1.31	1.42	1.64	3.50	3.64	3.73	4.26	4.50	4.72	ns
LVTTL_S12	1.31	1.42	1.64	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVTTL_S16	1.31	1.42	1.64	3.03	3.17	3.26	3.79	4.03	4.25	ns
LVTTL_S24	1.31	1.42	1.64	3.25	3.39	3.48	4.01	4.25	4.47	ns
LVTTL_F4	1.31	1.42	1.64	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVTTL_F8	1.31	1.42	1.64	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVTTL_F12	1.31	1.42	1.64	2.69	2.82	2.92	3.45	3.68	3.91	ns
LVTTL_F16	1.31	1.42	1.64	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVTTL_F24	1.31	1.42	1.64	2.41	2.64	2.89	3.17	3.50	3.88	ns
LVDS_25(1)	0.64	0.68	0.80	1.36	1.47	1.55	2.12	2.33	2.54	ns
MINI_LVDS_25	0.68	0.70	0.79	1.36	1.47	1.55	2.12	2.33	2.54	ns
BLVDS_25(1)	0.65	0.69	0.80	1.83	2.02	2.20	2.59	2.88	3.19	ns
RSDS_25 (point to point)(1)	0.63	0.68	0.79	1.36	1.48	1.55	2.12	2.34	2.54	ns
PPDS_25(1)	0.65	0.69	0.80	1.36	1.49	1.58	2.12	2.35	2.57	ns
TMDS_33(1)	0.72	0.76	0.86	1.43	1.54	1.60	2.19	2.40	2.59	ns
PCI33_3(1)	1.28	1.41	1.65	2.71	3.08	3.52	3.47	3.94	4.51	ns
HSUL_12	0.63	0.64	0.71	1.77	1.90	2.00	2.53	2.76	2.99	ns
DIFF_HSUL_12	0.58	0.61	0.70	1.55	1.68	1.78	2.31	2.54	2.77	ns
HSTL_I_S	0.61	0.64	0.73	1.55	1.69	1.80	2.31	2.55	2.79	ns
HSTL_II_S	0.61	0.64	0.73	1.21	1.34	1.43	1.97	2.20	2.42	ns
HSTL_I_18_S	0.64	0.67	0.76	1.28	1.39	1.45	2.04	2.25	2.44	ns
HSTL_II_18_S	0.64	0.67	0.76	1.18	1.31	1.40	1.94	2.17	2.39	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	1.42	1.54	1.61	2.18	2.40	2.60	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	1.15	1.24	1.27	1.91	2.10	2.26	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	1.27	1.38	1.43	2.03	2.24	2.42	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	1.14	1.23	1.26	1.90	2.09	2.25	ns
HSTL_I_F	0.61	0.64	0.73	1.10	1.19	1.23	1.86	2.05	2.22	ns

Table 19: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
HSTL_II_F	0.61	0.64	0.73	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_I_18_F	0.64	0.67	0.76	1.05	1.18	1.28	1.81	2.04	2.27	ns
HSTL_II_18_F	0.64	0.67	0.76	1.03	1.14	1.23	1.79	2.00	2.22	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	1.09	1.18	1.22	1.85	2.04	2.21	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	1.02	1.11	1.14	1.78	1.97	2.13	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	1.08	1.17	1.21	1.84	2.03	2.20	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	1.01	1.10	1.13	1.77	1.96	2.12	ns
LVCMOS33_S4	1.31	1.40	1.60	3.77	3.90	4.00	4.53	4.76	4.99	ns
LVCMOS33_S8	1.31	1.40	1.60	3.49	3.62	3.72	4.25	4.48	4.71	ns
LVCMOS33_S12	1.31	1.40	1.60	3.05	3.18	3.28	3.81	4.04	4.27	ns
LVCMOS33_S16	1.31	1.40	1.60	3.06	3.43	3.88	3.82	4.29	4.87	ns
LVCMOS33_F4	1.31	1.40	1.60	3.22	3.36	3.45	3.98	4.22	4.44	ns
LVCMOS33_F8	1.31	1.40	1.60	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVCMOS33_F12	1.31	1.40	1.60	2.57	2.85	3.15	3.33	3.71	4.14	ns
LVCMOS33_F16	1.31	1.40	1.60	2.44	2.69	2.96	3.20	3.55	3.95	ns
LVCMOS25_S4	1.08	1.16	1.32	3.08	3.22	3.31	3.84	4.08	4.30	ns
LVCMOS25_S8	1.08	1.16	1.32	2.85	2.98	3.07	3.61	3.84	4.06	ns
LVCMOS25_S12	1.08	1.16	1.32	2.44	2.57	2.67	3.20	3.43	3.66	ns
LVCMOS25_S16	1.08	1.16	1.32	2.79	2.92	3.01	3.55	3.78	4.00	ns
LVCMOS25_F4	1.08	1.16	1.32	2.71	2.84	2.93	3.47	3.70	3.92	ns
LVCMOS25_F8	1.08	1.16	1.32	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVCMOS25_F12	1.08	1.16	1.32	2.15	2.29	2.52	2.91	3.15	3.51	ns
LVCMOS25_F16	1.08	1.16	1.32	1.92	2.17	2.45	2.68	3.03	3.44	ns
LVCMOS18_S4	0.64	0.66	0.74	1.55	1.68	1.78	2.31	2.54	2.77	ns
LVCMOS18_S8	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVCMOS18_S12	0.64	0.66	0.74	2.14	2.28	2.37	2.90	3.14	3.36	ns
LVCMOS18_S16	0.64	0.66	0.74	1.49	1.62	1.72	2.25	2.48	2.71	ns
LVCMOS18_S24(1)	0.64	0.66	0.74	1.74	1.92	2.08	2.50	2.78	3.07	ns
LVCMOS18_F4	0.64	0.66	0.74	1.38	1.51	1.61	2.14	2.37	2.60	ns
LVCMOS18_F8	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVCMOS18_F12	0.64	0.66	0.74	1.64	1.78	1.87	2.40	2.64	2.86	ns
LVCMOS18_F16	0.64	0.66	0.74	1.52	1.68	1.81	2.28	2.54	2.80	ns
LVCMOS18_F24(1)	0.64	0.66	0.74	1.34	1.46	1.55	2.10	2.32	2.54	ns
LVCMOS15_S4	0.66	0.69	0.81	1.86	2.00	2.09	2.62	2.86	3.08	ns
LVCMOS15_S8	0.66	0.69	0.81	2.05	2.18	2.28	2.81	3.04	3.27	ns
LVCMOS15_S12	0.66	0.69	0.81	1.83	2.03	2.23	2.59	2.89	3.22	ns
LVCMOS15_S16	0.66	0.69	0.81	1.76	1.95	2.13	2.52	2.81	3.12	ns

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
LVDCI_15	0.59	0.62	0.73	1.98	2.23	2.58	2.62	2.99	3.40	ns
LVDCI_DV2_18	0.47	0.50	0.60	1.99	2.15	2.34	2.62	2.90	3.17	ns
LVDCI_DV2_15	0.59	0.62	0.73	1.98	2.23	2.58	2.62	2.99	3.40	ns
HSLVDCI_18	0.68	0.72	0.82	1.99	2.15	2.35	2.62	2.91	3.17	ns
HSLVDCI_15	0.68	0.72	0.82	1.98	2.23	2.58	2.62	2.99	3.40	ns
SSTL18_I_S	0.68	0.72	0.82	1.02	1.15	1.24	1.66	1.90	2.07	ns
SSTL18_II_S	0.68	0.72	0.82	1.17	1.29	1.37	1.81	2.05	2.19	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.92	1.06	1.17	1.56	1.82	1.99	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.88	0.98	1.08	1.51	1.74	1.90	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.92	1.06	1.17	1.56	1.82	1.99	ns
SSTL15_S	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
SSTL135_S	0.69	0.72	0.82	0.97	1.10	1.19	1.60	1.85	2.01	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
SSTL12_S	0.69	0.72	0.82	0.96	1.09	1.18	1.60	1.84	2.00	ns
SSTL12_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	1.02	1.15	1.24	1.66	1.90	2.07	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	1.17	1.29	1.37	1.81	2.05	2.19	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.92	1.06	1.17	1.56	1.82	1.99	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.88	0.98	1.08	1.51	1.74	1.90	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.92	1.06	1.17	1.56	1.82	1.99	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.94	1.06	1.15	1.57	1.82	1.97	ns
DIFF_SSTL135_S	0.69	0.72	0.82	0.97	1.10	1.19	1.60	1.85	2.01	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.97	1.09	1.19	1.60	1.85	2.01	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.96	1.09	1.18	1.60	1.84	2.00	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	1.03	1.17	1.27	1.66	1.92	2.09	ns
SSTL18_I_F	0.68	0.72	0.82	0.94	1.06	1.15	1.58	1.82	1.97	ns
SSTL18_II_F	0.68	0.72	0.82	0.97	1.09	1.16	1.61	1.84	1.99	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.89	1.02	1.10	1.53	1.77	1.92	ns

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	-3	-2/-2L/-2G	-1	
SSTL15_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
SSTL135_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
SSTL12_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.94	1.06	1.15	1.58	1.82	1.97	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.97	1.09	1.16	1.61	1.84	1.99	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.89	1.02	1.10	1.53	1.77	1.92	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.89	1.01	1.09	1.53	1.77	1.91	ns
DIFF_SSTL135_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.89	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.88	1.00	1.08	1.52	1.76	1.90	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	1.03	1.11	1.54	1.79	1.93	ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 21 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 21: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	ns
$T_{IOIBUFDISABLE\_HR}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	ns
$T_{IOIBUFDISABLE\_HP}$	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	ns

Input/Output Logic Switching Characteristics

Table 22: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T_{ICE1CK}/T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	ns
T_{ISRCK}/T_{ICKSR}	SR pin setup/hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	ns
$T_{IDOCKE2}/T_{IOCKDE2}$	D pin setup/hold with respect to CLK without delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	ns
$T_{IDOCKDE2}/T_{IOCKDDE2}$	DDLY pin setup/hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	ns
$T_{IDOCKE3}/T_{IOCKDE3}$	D pin setup/hold with respect to CLK without delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	ns
$T_{IDOCKDE3}/T_{IOCKDDE3}$	DDLY pin setup/hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	ns
Combinatorial					
T_{IDIE2}	D pin to O pin propagation delay, no delay (HP I/O banks only)	0.09	0.10	0.12	ns
T_{IDIDE2}	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	ns
T_{IDIE3}	D pin to O pin propagation delay, no delay (HR I/O banks only)	0.09	0.10	0.12	ns
T_{IDIDE3}	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	ns
Sequential Delays					
T_{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without delay (HP I/O banks only)	0.36	0.39	0.45	ns
$T_{IDLODE2}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	ns
T_{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without delay (HR I/O banks only)	0.36	0.39	0.45	ns
$T_{IDLODE3}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	ns
T_{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	ns
$T_{RQ\_ILOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	ns
$T_{GSRQ\_ILOGICE2}$	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
$T_{RQ\_ILOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	ns
$T_{GSRQ\_ILOGICE3}$	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
$T_{RPW\_ILOGICE2}$	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	ns, Min
$T_{RPW\_ILOGICE3}$	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	ns, Min

Input/Output Delay Switching Characteristics

Table 26: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IDELAYCTRL					
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.22	3.22	3.22	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200	MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width	52.00	52.00	52.00	ns
IDELAY/ODELAY					
$T_{IDELAYRESOLUTION}$	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F_{REF})			ps
$T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$/ $T_{ODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY/ODELAY	800	800	710	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	ns
T_{ODCCK_CE} / T_{ODCKC_CE}	CE pin setup/hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	ns
T_{ODCCK_INC}/ T_{ODCKC_INC}	INC pin setup/hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	ns
T_{ODCCK_RST}/ T_{ODCKC_RST}	RST pin setup/hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	ps
$T_{ODDO\_ODATAIN}$	Propagation delay through ODELAY	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

Table 27: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IO_FIFO Clock to Out Delays					
T_{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags	0.59	0.62	0.81	ns
Setup/Hold					
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.43/–0.01	0.47/–0.01	0.53/–0.01	ns
$T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$	WREN to WRCLK	0.39/–0.01	0.43/–0.01	0.50/–0.01	ns
$T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	ns
Minimum Pulse Width					
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
Maximum Frequency					
F_{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	MHz

Table 47: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)(2)						
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(3) with PLL	XC7V585T	3.07/–0.21	3.40/–0.21	3.72/–0.21	ns
		XC7V2000T	N/A	2.99/–0.35	3.27/–0.35	ns
		XC7VX330T	2.94/–0.26	3.26/–0.26	3.57/–0.26	ns
		XC7VX415T	3.09/–0.10	3.42/–0.10	3.75/–0.10	ns
		XC7VX485T	2.95/–0.26	3.26/–0.26	3.58/–0.26	ns
		XC7VX550T	3.08/–0.20	3.40/–0.20	3.74/–0.20	ns
		XC7VX690T	3.08/–0.10	3.40/–0.10	3.74/–0.10	ns
		XC7VX980T	N/A	3.39/–0.21	3.72/–0.21	ns
		XC7VX1140T	N/A	3.00/–0.35	3.27/–0.35	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. IFF = Input Flip-Flop or Latch
4. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T_{PSCS}/T_{PHCS}	Setup/hold of I/O clock for HR I/O banks	–0.36/1.36	–0.36/1.50	–0.36/1.70	ns
	Setup/hold of I/O clock for HP I/O banks	–0.34/1.39	–0.34/1.53	–0.34/1.73	ns

Table 49: **Sample Window**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T_{SAMP}	Sampling error at receiver pins(1)	0.51	0.56	0.61	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO(2)	0.30	0.35	0.40	ns

Notes:

1. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 63: **CEI-6G and CEI-11G Protocol Characteristics (GTX Transceivers)**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter(2)	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(2)	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 64: **SFP+ Protocol Characteristics (GTX Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40(1)	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40(1)	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 72: **GTH Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3E/-2GE(2)	-2(C&I)/-2LE(2)	-1(C&I)(3)	
F_{TXOUT}	TXUSERCLKOUT maximum frequency			412.500	412.500	312.500	MHz
F_{RXOUT}	RXUSERCLKOUT maximum frequency			412.500	412.500	312.500	MHz
F_{TXIN}	TXUSERCLKIN maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	409.375	353.125	265.625	MHz
F_{RXIN}	RXUSERCLKIN maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	409.375	353.125	265.625	MHz
F_{TXIN2}	TXUSERCLKIN2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	409.375	353.125	265.625	MHz
		64-bit	64-bit	204.688	176.563	132.813	MHz
F_{RXIN2}	RXUSERCLKIN2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	409.375	353.125	265.625	MHz
		64-bit	64-bit	204.688	176.563	132.813	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* (UG476).
2. For speed grades -3E, -2GE, -2C, -2I, and -2LE, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
3. For speed grade -1 (and when V_{CCINT} = 0.9V), a 16-bit data path can only be used for speeds less than 5.0 Gb/s.

Table 73: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHTX}	Serial data rate range		0.500	–	F_{GTHMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	40	–	ps
T_{FTX}	TX fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.3	UI
$DJ_{13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{12.5}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$DJ_{12.5}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{11.3}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$DJ_{11.3}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$DJ_{10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$DJ_{10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$TJ_{9.953}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$DJ_{9.953}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{9.8}$	Total jitter(2)(4)	9.8 Gb/s	–	–	0.28	UI
$DJ_{9.8}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$TJ_{8.0\_QPLL}$	Total jitter(2)(4)	8.0 Gb/s	–	–	0.28	UI
$DJ_{8.0\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI

Table 74: **GTH Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTHRX}	Serial data rate	RX oversampler not enabled	0.500	–	F_{GTHMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)		–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{13.1}$	Sinusoidal jitter (QPLL)(3)	13.1 Gb/s	0.3	–	–	UI
$JT\_SJ_{12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.3	–	–	UI
$JT\_SJ_{11.3}$	Sinusoidal jitter (QPLL)(3)	11.3 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32\_QPLL}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.8}$	Sinusoidal jitter (QPLL)(3)	9.8 Gb/s	0.3	–	–	UI
$JT\_SJ_{8.0\_QPLL}$	Sinusoidal jitter (QPLL)(3)	8.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{8.0\_CPLL}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s	0.42	–	–	UI
$JT\_SJ_{6.6\_QPLL}$	Sinusoidal jitter (QPLL)(3)	6.6 Gb/s	0.48	–	–	UI
$JT\_SJ_{6.6\_CPLL}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal jitter (CPLL)(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{3.2L}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(5)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(6)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(7)	0.5	–	–	UI
JT_SJ_{500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$JT\_TJSE_{6.6}$		6.6 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.1	–	–	UI
$JT\_SJSE_{6.6}$		6.6 Gb/s	0.1	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.

Table 80: **CPRI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 79.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 81: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
$F_{USERCLK}$	User clock maximum frequency	500.00	500.00	250.00	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz

Table 82: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference(5)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for new BitGen option XADCEnhancedLinearity = ON.
3. For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
4. For a detailed description, see the Timing chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 83: **Configuration Switching Characteristics**

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Power-up Timing Characteristics						
T_{PL}(1)	Program latency		5	5	5	ms, Max
T_{POR}(1)	Power-on reset (50ms ramp rate time)		10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1ms ramp rate time)		10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width		250	250	250	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay		150	150	150	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle		40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle		40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency		100	100	100	MHz, Max
	Master CCLK frequency for AES encrypted x16		50	50	50	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration		3	3	3	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK.		±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time		2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time		2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave CCLK frequency		100	100	100	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time		2.5	2.5	2.5	ns, Min
T_{EMCCKH}	External master CCLK High time		2.5	2.5	2.5	ns, Min
F_{EMCCK}	External master CCLK frequency		100	100	100	MHz, Max
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2)		100.00	100.00	100.00	MHz, Max

Table 83: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Virtex-7 T and XT Devices	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T_{CCO}	DOUT clock to out		8.0	8.0	8.0	ns, Max
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	D[31:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B setup/hold		10.0/0.0	10.0/0.0	10.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)		7.0	7.0	7.0	ns, Max
T_{SMCO}	D[31:00] clock to out in readback		8.0	8.0	8.0	ns, Max
F_{RBCCK}	Readback frequency	SLR-based	70	70	70	MHz, Max
		All other devices	100	100	100	MHz, Max
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold	SLR-based	9.0/2.0	9.0/2.0	9.0/2.0	ns, Min
		All other devices	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	SLR-based	17	17	17	ns, Max
		All other devices	7.0	7.0	7.0	ns, Max
F_{TCK}	TCK frequency	SLR-based	20	20	20	MHz, Max
		All other devices	66	66	66	MHz, Max
BPI Master Flash Mode Programming Switching						
T_{BPICCO} (2)	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out		8.5	8.5	8.5	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min
SPI Master Flash Mode Programming Switching						
T_{SPIDCC}/T_{SPICCD}	D[03:00] setup/hold		3.0/0.0	3.0/0.0	3.0/0.0	ns, Min
T_{SPICCM}	MOSI clock to out		8.0	8.0	8.0	ns, Max
$T_{SPICCFC}$	FCS_B clock to out		8.0	8.0	8.0	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 84 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470).

Table 84: **eFUSE Programming Conditions** (1)

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

Date	Version	Description
08/03/2012	1.5	Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 12 and Note 13. Updated parameters in Table 3. Added Table 4 and Table 5. Updated the values for in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11. Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.2 speed specifications throughout the document with appropriate changes to Table 15 and Table 16 including production release of the XC7VX485T in the -2 and -1 speed designations. Added notes and specifications to Table 18. Updated the IOB Pad Input/Output/3-State discussion and changed Table 21 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 28. Rearranged Table 51 including moving some parameters to Table 1. Added Table 56. Updated Table 57. In Table 59, updated SJ Jitter Tolerance with Stressed Eye section, page 48 and Note 8. Added Note 1, Note 2, and Note 3 to Table 62. Added Note 1 and Note 2 to Table 63, and line rate ranges. Updated Table 64 including adding Note 1. Updated Table 65 including adding Note 1. In Table 82 updated Note 1 and added Note 4. In Table 83, updated T_{POR} and F_{EMCCK}.
09/20/2012	1.6	Removed the XC7V1500T device from data sheet. In Table 2, revised V_{CCINT} and V_{CCBRAM} and added Note 3. Updated some of the values in Table 7. Revised Table 15 and Table 16 to include production release of the XC7V585T in the -2 and -1 speed designations. Added values for the XC7V585T in Table 50. Updated Note 2 in Table 58.
09/26/2012	1.7	Revised Table 15 and Table 16 to include production release of the XC7VX485T in the -3 speed designation.
10/19/2012	1.8	Revised Table 15 and Table 16 to include production release of the XC7VX485T in the -2L (1.0V) speed designation. Removed -2L (0.9V) speed specifications from data sheet, this change includes edits to V_{CCINT} and V_{CCBRAM} in Table 2, editing Note 1 and removing Note 2 in Table 53. Also in Table 53, updated the F_{GTXMAX}, $F_{GTXQRANGE1}$, and $F_{GQPLLRANGE1}$ specification for -1 speed grade from 6.6 Gb/s to 8.0 Gb/s. Edited Note 4 in Table 57 and Note 3 in Table 72.
12/12/2012	1.9	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.3 speed specifications throughout the document. Revised Table 15 and Table 16 to include production release of the XC7V585T in the -3 and -2L(1.0V) speed designations. Updated the notes in Table 50. Updated GTH Transceiver Specifications including removal of GTH Transceiver DC Characteristics section (use the XPE (download at http://www.xilinx.com/power). Updated Table 68 and added Table 71, Table 73, and Table 74. Removed Note 4 from Table 82.
12/24/2012	1.10	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.4 and Vivado 2012.4 speed specifications throughout the document. Revised the XC7V2000T in the -1 and -2 speed designations Table 15 to preliminary. Added the GTH Transceiver Protocol Jitter Characteristics section. Updated T_{TCKTDO} and added Internal Configuration Access Port section to Table 83.
01/31/2013	1.11	Added Note 2 to Table 2. Revised Table 15 and Table 16 to include production release of the XC7V2000T in the -1 and -2 speed specifications. Updated Note 1 in Table 35. Updated the notes in Table 37, Table 40 through Table 43, Table 46, and Table 47. In Table 66, updated D_{VPPIN}. In Table 67, updated V_{IDIFF}. Removed T_{LOCK} and T_{PHASE} from Table 70. Updated T_{DLOCK} in Table 71.
03/07/2013	1.12	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.5 and Vivado 2013.1 speed specifications throughout the document. Revised Table 15 and Table 16 to include production release of the XC7VX690T. Revised D_{VPPOUT} in Table 66. Updated values in Table 67 and Table 74. Removed Note 1 from Table 68. Updated MMCM_F_{PFDMAX} in Table 38 and PLL_F_{PFDMAX} in Table 39. Added skew values to Table 50.

Date	Version	Description
03/27/2013	1.13	In Table 7, added values for the XC7VX330T and XC7VX415T devices. Revised Table 15 and Table 16 to include production release of the XC7VX330T and XC7VX415T. In Table 18, updated the table title, LPDDR2 values, and removed Note 3. Removed Note 2: *For QPLL line rate, the maximum line rate with the divider N set to 66 is 10.3125 Gb/s* from Table 68.
04/17/2013	1.14	Updated the AC Switching Characteristics section with production release changes to Table 15 and Table 16 for XC7VX550T for all speed specifications. In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4 and Table 5, and combined Note 4 with old Note 5 and then added new Note 5. Revised V_{IN} description and added Note 8 in Table 2. Updated first 3 rows in Table 4 and Table 5. Updated values and added new values to Table 7. Also revised PCI33_3 voltage minimum in Table 10 to match values in Table 1, Table 4, and Table 5. Added Note 1 to Table 12 and Table 13. Throughout the data sheet (Table 29, Table 30, and Table 45) removed the obvious note “A Zero “0” Hold Time listing indicates no hold time or a negative hold time.” Updated and clarified USRCLK data in Table 57 and Table 72.

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