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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	37950
Number of Logic Elements/Cells	485760
Total RAM Bits	37969920
Number of I/O	350
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1158-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7vx485t-3ffg1158e

Table 5: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks⁽¹⁾⁽²⁾

AC Voltage Overshoot	% of UI @ -40°C to 100°C	AC Voltage Undershoot	% of UI @ -40°C to 100°C
$V_{CCO} + 0.55$	100	-0.55	100
$V_{CCO} + 0.60$	50.0	-0.60	50.0
$V_{CCO} + 0.65$	50.0	-0.65	50.0
$V_{CCO} + 0.70$	47.0	-0.70	50.0
$V_{CCO} + 0.75$	21.2	-0.75	50.0
$V_{CCO} + 0.80$	9.71	-0.80	50.0
$V_{CCO} + 0.85$	4.51	-0.85	28.4
$V_{CCO} + 0.90$	2.12	-0.90	12.7
$V_{CCO} + 0.95$	1.01	-0.95	5.79

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μ s.

Table 6: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7V585T	1483	1483	1483	mA
		XC7V2000T	N/A	3756	3756	mA
		XC7VX330T	1012	1012	1012	mA
		XC7VX415T	1324	1324	1324	mA
		XC7VX485T	1578	1578	1578	mA
		XC7VX550T	2214	2214	2214	mA
		XC7VX690T	2214	2214	2214	mA
		XC7VX980T	N/A	2580	2580	mA
		XC7VX1140T	N/A	3448	3448	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7V585T	1	1	1	mA
		XC7V2000T	N/A	1	1	mA
		XC7VX330T	1	1	1	mA
		XC7VX415T	1	1	1	mA
		XC7VX485T	1	1	1	mA
		XC7VX550T	1	1	1	mA
		XC7VX690T	1	1	1	mA
		XC7VX980T	N/A	1	1	mA
		XC7VX1140T	N/A	1	1	mA

Table 6: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC7V585T	114	114	114	mA
		XC7V2000T	N/A	315	315	mA
		XC7VX330T	73	73	73	mA
		XC7VX415T	88	88	88	mA
		XC7VX485T	104	104	104	mA
		XC7VX550T	147	147	147	mA
		XC7VX690T	147	147	147	mA
		XC7VX980T	N/A	183	183	mA
		XC7VX1140T	N/A	250	250	mA
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current	XC7V585T	2	2	2	mA
		XC7V2000T	N/A	2	2	mA
		XC7VX330T	2	2	2	mA
		XC7VX415T	2	2	2	mA
		XC7VX485T	2	2	2	mA
		XC7VX550T	2	2	2	mA
		XC7VX690T	2	2	2	mA
		XC7VX980T	N/A	2	2	mA
		XC7VX1140T	N/A	2	2	mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7V585T	34	34	34	mA
		XC7V2000T	N/A	56	56	mA
		XC7VX330T	32	32	32	mA
		XC7VX415T	38	38	38	mA
		XC7VX485T	44	44	44	mA
		XC7VX550T	63	63	63	mA
		XC7VX690T	63	63	63	mA
		XC7VX980T	N/A	65	65	mA
		XC7VX1140T	N/A	81	81	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX/GTH transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to $0.3 \times T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$ V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to $0.3 \times T_{VCCINT}$ (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

LVDS DC Specifications (LVDS_25)

The LVDS standard is available in the HR I/O banks.

Table 12: LVDS_25 DC Specifications⁽¹⁾

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage		0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks.

Table 13: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		1.710	1.800	1.890	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output common-mode voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High ($\overline{Q} - Q$), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = $\pm 350\text{ mV}$	0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* ([UG471](#)) for more information.

Input/Output Logic Switching Characteristics

Table 22: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{ICE1CK} /T _{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	ns
T _{ISRCK} /T _{ICKSR}	SR pin setup/hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	ns
T _{IDOCKE2} /T _{IOCKDE2}	D pin setup/hold with respect to CLK without delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	ns
T _{IDOCKDE2} /T _{IOCKDDE2}	DDL _Y pin setup/hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	ns
T _{IDOCKE3} /T _{IOCKDE3}	D pin setup/hold with respect to CLK without delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	ns
T _{IDOCKDE3} /T _{IOCKDDE3}	DDL _Y pin setup/hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	ns
Combinatorial					
T _{IDIE2}	D pin to O pin propagation delay, no delay (HP I/O banks only)	0.09	0.10	0.12	ns
T _{IDIDE2}	DDL _Y pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	ns
T _{IDIE3}	D pin to O pin propagation delay, no delay (HR I/O banks only)	0.09	0.10	0.12	ns
T _{IDIDE3}	DDL _Y pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	ns
Sequential Delays					
T _{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without delay (HP I/O banks only)	0.36	0.39	0.45	ns
T _{IDLODE2}	DDL _Y pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	ns
T _{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without delay (HR I/O banks only)	0.36	0.39	0.45	ns
T _{IDLODE3}	DDL _Y pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	ns
T _{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	ns
T _{RQ_ILOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	ns
T _{GSRQ_ILOGICE2}	Global set/reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	ns
T _{RQ_ILOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	ns
T _{GSRQ_ILOGICE3}	Global set/reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	ns
Set/Reset					
T _{RPW_ILOGICE2}	Minimum pulse width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	ns, Min
T _{RPW_ILOGICE3}	Minimum pulse width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	ns, Min

Output Serializer/Deserializer Switching Characteristics

Table 25: OSERDES Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Setup/Hold					
T _{OSDCK_D} /T _{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input setup/hold with respect to CLK	0.49/−0.15	0.56/−0.15	0.68/−0.15	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input setup/hold with respect to CLKDIV	0.27/−0.15	0.30/−0.15	0.34/−0.15	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input setup/hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	ns
T _{OSCCK_S}	SR (Reset) input setup with respect to CLKDIV	0.41	0.46	0.75	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input setup/hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	ns
Sequential Delays					
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	ns
Combinatorial					
T _{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Table 27: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
IO_FIFO Clock to Out Delays					
T _{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags	0.59	0.62	0.81	ns
Setup/Hold					
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.43/−0.01	0.47/−0.01	0.53/−0.01	ns
T _{IFFCK_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.39/−0.01	0.43/−0.01	0.50/−0.01	ns
T _{OFFCK_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	ns
Minimum Pulse Width					
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	ns
Maximum Frequency					
F _{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	MHz

CLB Switching Characteristics

Table 28: CLB Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Combinatorial Delays					
T _{ILO}	An – Dn LUT address to A	0.05	0.05	0.06	ns, Max
T _{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.15	0.16	0.19	ns, Max
T _{ILO_3}	An – Dn LUT address to BMUX_A	0.24	0.25	0.30	ns, Max
T _{ITO}	An – Dn inputs to A – D Q outputs	0.58	0.61	0.74	ns, Max
T _{AXA}	AX inputs to AMUX output	0.38	0.40	0.49	ns, Max
T _{AXB}	AX inputs to BMUX output	0.40	0.42	0.52	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.41	0.50	ns, Max
T _{AXD}	AX inputs to DMUX output	0.43	0.44	0.52	ns, Max
T _{BXB}	BX inputs to BMUX output	0.31	0.33	0.40	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.39	0.47	ns, Max
T _{CXC}	CX inputs to CMUX output	0.27	0.28	0.34	ns, Max
T _{CXD}	CX inputs to DMUX output	0.33	0.34	0.41	ns, Max
T _{DXD}	DX inputs to DMUX output	0.32	0.33	0.40	ns, Max
Sequential Delays					
T _{CKO}	Clock to AQ – DQ outputs	0.26	0.27	0.32	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.32	0.32	0.39	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T _{AS} /T _{AH}	A _N – D _N input to CLK on A – D flip-flops	0.01/0.12	0.02/0.13	0.03/0.18	ns, Min
T _{DICK} /T _{CKDI}	A _X – D _X input to CLK on A – D flip-flops	0.04/0.14	0.04/0.14	0.05/0.20	ns, Min
	A _X – D _X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.36/0.10	0.37/0.11	0.46/0.16	ns, Min
T _{CECK_CLB} /T _{CKCE_CLB}	CE input to CLK on A – D flip-flops	0.19/0.05	0.20/0.05	0.25/0.05	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D flip-flops	0.30/0.05	0.31/0.07	0.37/0.09	ns, Min
Set/Reset					
T _{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.38	0.38	0.46	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.34	0.35	0.43	ns, Max
F _{TOG}	Toggle frequency (for export control)	1818	1818	1818	MHz

Table 31: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Maximum Frequency					
F _{MAX_BRAM_WF_NC}	Block RAM (Write first and No change modes) When not in SDP RF mode	601.32	543.77	458.09	MHz
F _{MAX_BRAM_RF_PERFORMANCE}	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601.32	543.77	458.09	MHz
F _{MAX_BRAM_RF_DELAYED_WRITE}	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528.26	477.33	400.80	MHz
F _{MAX_CAS_WF_NC}	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551.27	493.83	408.00	MHz
F _{MAX_CAS_RF_PERFORMANCE}	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551.27	493.83	408.00	MHz
F _{MAX_CAS_RF_DELAYED_WRITE}	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478.24	427.35	350.88	MHz
F _{MAX_FIFO}	FIFO in all modes without ECC	601.32	543.77	458.09	MHz
F _{MAX_ECC}	Block RAM and FIFO in ECC configuration	484.26	430.85	351.12	MHz

Notes:

1. The timing report shows all of these parameters as $T_{\text{RCKO_DO}}$.
2. $T_{\text{RCKO_DOR}}$ includes $T_{\text{RCKO_DOW}}$, $T_{\text{RCKO_DOPR}}$, and $T_{\text{RCKO_DOPW}}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with $\text{DO_REG} = 0$.
4. $T_{\text{RCKO_DO}}$ includes $T_{\text{RCKO_DOP}}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with $\text{DO_REG} = 1$.
6. $T_{\text{RCKO_FLAGS}}$ includes the following parameters: $T_{\text{RCKO_AEMPTY}}$, $T_{\text{RCKO_AFULL}}$, $T_{\text{RCKO_EMPTY}}$, $T_{\text{RCKO_FULL}}$, $T_{\text{RCKO_RDERR}}$, $T_{\text{RCKO_WRERR}}$.
7. $T_{\text{RCKO_POINTERS}}$ includes both $T_{\text{RCKO_RDCOUNT}}$ and $T_{\text{RCKO_WRCOUNT}}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{\text{RCO_FLAGS}}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Table 38: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
MMCM_T _{LOCKMAX}	MMCM maximum Lock Time	100	100	100	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency	1066.00	933.00	800.00	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency ⁽⁵⁾⁽⁶⁾	4.69	4.69	4.69	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation	< 20% of clock input period or 1 ns Max			
MMCM_RST _{MINPULSE}	Minimum reset pulse width	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector	10.00	10.00	10.00	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
T _{MMCMDCCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and hold of phase-shift enable	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMDCCK_PSINCDEC} / T _{MMCMCKD_PSINCDEC}	Setup and hold of phase-shift increment/decrement	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMCKO_PSDONE}	Phase shift clock-to-out of PSDONE	0.59	0.68	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
T _{MMCMDCCK_DADDR} / T _{MMCMCKD_DADDR}	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{MMCMDCCK_DI} /T _{MMCMCKD_DI}	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{MMCMDCCK_DEN} /T _{MMCMCKD_DEN}	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	ns, Min
T _{MMCMDCCK_DWE} /T _{MMCMCKD_DWE}	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	ns, Min
T _{MMCMCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 40: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T _{ICKOF}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7V585T	5.63	6.20	6.97	ns
		XC7V2000T	N/A	5.66	6.35	ns
		XC7VX330T	5.41	5.97	6.71	ns
		XC7VX415T	5.46	5.96	6.70	ns
		XC7VX485T	5.29	5.84	6.57	ns
		XC7VX550T	5.45	6.02	6.76	ns
		XC7VX690T	5.46	6.02	6.76	ns
		XC7VX980T	N/A	6.12	6.87	ns
		XC7VX1140T	N/A	5.59	6.28	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 41: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T _{ICKOFFAR}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7V585T	6.81	7.53	8.44	ns
		XC7V2000T	N/A	6.00	6.73	ns
		XC7VX330T	6.31	6.97	7.83	ns
		XC7VX415T	6.36	6.90	7.69	ns
		XC7VX485T	6.20	6.86	7.69	ns
		XC7VX550T	6.66	7.37	8.27	ns
		XC7VX690T	6.69	7.37	8.27	ns
		XC7VX980T	N/A	7.47	8.37	ns
		XC7VX1140T	N/A	5.93	6.65	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 47: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade			Units
			-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾⁽²⁾						
T _{PSPLLCC} / T _{PHPLLCC}	No delay clock-capable clock input and IFF ⁽³⁾ with PLL	XC7V585T	3.07/−0.21	3.40/−0.21	3.72/−0.21	ns
		XC7V2000T	N/A	2.99/−0.35	3.27/−0.35	ns
		XC7VX330T	2.94/−0.26	3.26/−0.26	3.57/−0.26	ns
		XC7VX415T	3.09/−0.10	3.42/−0.10	3.75/−0.10	ns
		XC7VX485T	2.95/−0.26	3.26/−0.26	3.58/−0.26	ns
		XC7VX550T	3.08/−0.20	3.40/−0.20	3.74/−0.20	ns
		XC7VX690T	3.08/−0.10	3.40/−0.10	3.74/−0.10	ns
		XC7VX980T	N/A	3.39/−0.21	3.72/−0.21	ns
		XC7VX1140T	N/A	3.00/−0.35	3.27/−0.35	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. IFF = Input Flip-Flop or Latch
4. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 48: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T _{PSCS} /T _{PHCS}	Setup/hold of I/O clock for HR I/O banks	–0.36/1.36	–0.36/1.50	–0.36/1.70	ns
	Setup/hold of I/O clock for HP I/O banks	–0.34/1.39	–0.34/1.53	–0.34/1.73	ns

Table 49: Sample Window

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
T _{SAMP}	Sampling error at receiver pins ⁽¹⁾	0.51	0.56	0.61	ns
T _{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO ⁽²⁾	0.30	0.35	0.40	ns

Notes:

1. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Virtex-7 T and XT FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further details.

Table 52: GTX Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V _{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R _{IN}	Differential input resistance	–	100	–	Ω
C _{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)) for further information.

Table 53: GTX Transceiver Performance

Symbol	Description	Output Divider	Speed Grade			Units
			-3/-2G	-2/-2L	-1 ⁽¹⁾	
F _{GTXMAX} ⁽²⁾	Maximum GTX transceiver data rate		12.5	10.3125	8.0	Gb/s
F _{GTXMIN} ⁽²⁾	Minimum GTX transceiver data rate		0.500	0.500	0.500	Gb/s
F _{GTXCRANGE}	CPLL line rate range	1	3.2–6.6			Gb/s
		2	1.6–3.3			Gb/s
		4	0.8–1.65			Gb/s
		8	0.5–0.825			Gb/s
		16	N/A			Gb/s
F _{GTXQRANGE1}	QPLL line rate range 1	1	5.93–8.0	5.93–8.0	5.93–8.0	Gb/s
		2	2.965–4.0	2.965–4.0	2.965–4.0	Gb/s
		4	1.4825–2.0	1.4825–2.0	1.4825–2.0	Gb/s
		8	0.74125–1.0	0.74125–1.0	0.74125–1.0	Gb/s
		16	N/A	N/A	N/A	Gb/s
F _{GTXQRANGE2}	QPLL line rate range 2 ⁽³⁾	1	9.8–12.5	9.8–10.3125	N/A	Gb/s
		2	4.9–6.25	4.9–5.15625	N/A	Gb/s
		4	2.45–3.125	2.45–2.578125	N/A	Gb/s
		8	1.225–1.5625	1.225–1.2890625	N/A	Gb/s
		16	0.6125–0.78125	0.6125–0.64453125	N/A	Gb/s
F _{GCPLLRANGE}	GTX transceiver CPLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	GHz
F _{GQPLLRange1}	GTX transceiver QPLL frequency range 1		5.93–8.0	5.93–8.0	5.93–8.0	GHz
F _{GQPLLRange2}	GTX transceiver QPLL frequency range 2		9.8–12.5	9.8–10.3125	N/A	GHz

Notes:

- The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s. A -1 speed grade with V_{CCINT} = 0.9V, as described in the *Lowering Power using the Voltage Identification Bit* application note ([XAPP555](#)), requires a 4-byte internal data width for operation above 3.8 Gb/s.
- Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
- For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3/-2G	-2/-2L	-1	
F _{GTXDRPCLK}	GTXDRPCLK maximum frequency	175.01	175.01	156.25	MHz

Table 55: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

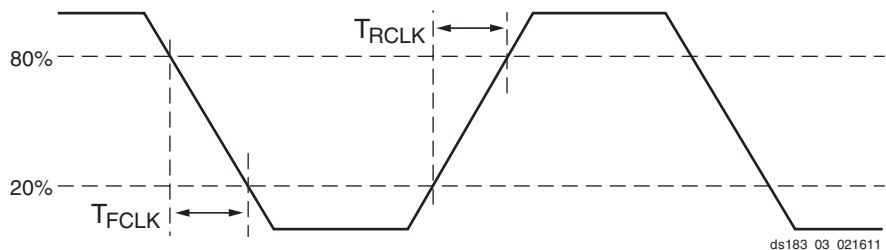


Figure 3: Reference Clock Timing Parameters

Table 56: GTX Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 58: GTX Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
TJ _{6.6_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
DJ _{6.6_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
DJ _{5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
DJ _{4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.75}	Total jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	–	–	0.30	UI
DJ _{3.75}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
TJ _{3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
DJ _{3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
TJ _{3.20L}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁶⁾	–	–	0.32	UI
DJ _{3.20L}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
TJ _{2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁷⁾	–	–	0.20	UI
DJ _{2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.08	UI
TJ _{1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁸⁾	–	–	0.15	UI
DJ _{1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
TJ ₅₀₀	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s	–	–	0.10	UI
DJ ₅₀₀	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 59: GTX Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTXRX}	Serial data rate	RX oversampler not enabled	0.500	–	F _{GTXMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm
RX _{RL}	Run length (CID)		–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance ⁽²⁾						
JT_SJ _{12.5}	Sinusoidal jitter (QPLL) ⁽³⁾	12.5 Gb/s	0.3	–	–	UI
JT_SJ _{11.18}	Sinusoidal jitter (QPLL) ⁽³⁾	11.18 Gb/s	0.3	–	–	UI
JT_SJ _{10.32}	Sinusoidal jitter (QPLL) ⁽³⁾	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.95}	Sinusoidal jitter (QPLL) ⁽³⁾	9.95 Gb/s	0.3	–	–	UI
JT_SJ _{9.8}	Sinusoidal jitter (QPLL) ⁽³⁾	9.8 Gb/s	0.3	–	–	UI
JT_SJ _{8.0}	Sinusoidal jitter (QPLL) ⁽³⁾	8.0 Gb/s	0.44	–	–	UI
JT_SJ _{6.6_QPLL}	Sinusoidal jitter (QPLL) ⁽³⁾	6.6 Gb/s	0.48	–	–	UI
JT_SJ _{6.6_CPLL}	Sinusoidal jitter (CPLL) ⁽³⁾	6.6 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal jitter (CPLL) ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal jitter (CPLL) ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal jitter (CPLL) ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.2}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{3.2L}	Sinusoidal jitter (CPLL) ⁽³⁾	3.2 Gb/s ⁽⁵⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal jitter (CPLL) ⁽³⁾	2.5 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal jitter (CPLL) ⁽³⁾	1.25 Gb/s ⁽⁷⁾	0.5	–	–	UI
JT_SJ ₅₀₀	Sinusoidal jitter (CPLL) ⁽³⁾	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye ⁽²⁾						
JT_TJSE _{3.2}	Total jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.70	–	–	UI
JT_TJSE _{6.6}		6.6 Gb/s	0.70	–	–	UI
JT_SJSE _{3.2}	Sinusoidal jitter with stressed eye ⁽⁸⁾	3.2 Gb/s	0.1	–	–	UI
JT_SJSE _{6.6}		6.6 Gb/s	0.1	–	–	UI

Notes:

- Using RXOUT_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of $1e^{-12}$.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

Table 72: GTH Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Data Width Conditions		Speed Grade			Units
		Internal Logic	Interconnect Logic	-3E/-2GE ⁽²⁾	-2(C&I)/-2LE ⁽²⁾	-1(C&I) ⁽³⁾	
F _{TXOUT}	TXUSERCLKOUT maximum frequency			412.500	412.500	312.500	MHz
F _{RXOUT}	RXUSERCLKOUT maximum frequency			412.500	412.500	312.500	MHz
F _{TXIN}	TXUSERCLKIN maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	409.375	353.125	265.625	MHz
F _{RXIN}	RXUSERCLKIN maximum frequency	16-bit	16-bit and 32-bit	412.500	412.500	312.500	MHz
		32-bit	32-bit	409.375	353.125	265.625	MHz
F _{TXIN2}	TXUSERCLKIN2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	409.375	353.125	265.625	MHz
		64-bit	64-bit	204.688	176.563	132.813	MHz
F _{RXIN2}	RXUSERCLKIN2 maximum frequency	16-bit	16-bit	412.500	412.500	312.500	MHz
		16-bit and 32-bit	32-bit	409.375	353.125	265.625	MHz
		64-bit	64-bit	204.688	176.563	132.813	MHz

Notes:

- Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceiver User Guide* ([UG476](#)).
- For speed grades -3E, -2GE, -2C, -2I, and -2LE, a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
- For speed grade -1 (and when V_{CCINT} = 0.9V), a 16-bit data path can only be used for speeds less than 5.0 Gb/s.

Table 73: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	—	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	—	40	—	ps
T _{FTX}	TX fall time	80%–20%	—	40	—	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		—	—	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		—	—	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		—	—	140	ns
TJ _{13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	—	—	0.3	UI
DJ _{13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{12.5}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	—	—	0.28	UI
DJ _{12.5}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{11.3}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	—	—	0.28	UI
DJ _{11.3}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	—	—	0.28	UI
DJ _{10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	—	—	0.33	UI
DJ _{10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		—	—	0.17	UI
TJ _{9.953}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	—	—	0.28	UI
DJ _{9.953}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{9.8}	Total jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	—	—	0.28	UI
DJ _{9.8}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{8.0_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	—	—	0.28	UI
DJ _{8.0_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI

Table 80: CPRI Protocol Characteristics (GTH Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	—	0.35	UI
	1228.8	—	0.35	UI
	2457.6	—	0.35	UI
	3072.0	—	0.35	UI
	4915.2	—	0.3	UI
	6144.0	—	0.3	UI
	9830.4	—	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	—	UI
	1228.8	0.65	—	UI
	2457.6	0.65	—	UI
	3072.0	0.65	—	UI
	4915.2	0.95	—	UI
	6144.0	0.95	—	UI
	9830.4	Note 1	—	UI

Notes:

1. Tested per SFP+ specification, see Table 79.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 81: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade			Units
		-3	-2/-2L/-2G	-1	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	500.00	500.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	MHz

Table 83: Configuration Switching Characteristics (Cont'd)

Symbol	Description		Virtex-7 T and XT Devices	Speed Grade			Units
				-3	-2/-2L/-2G	-1	
Master/Slave Serial Mode Programming Switching							
T _{DCCK} /T _{CCKD}	DIN setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min	
T _{CCO}	DOUT clock to out		8.0	8.0	8.0	ns, Max	
SelectMAP Mode Programming Switching							
T _{SMDCCK} /T _{SMCCKD}	D[31:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min	
T _{SMCSCCK} /T _{SMCCKCS}	CSI_B setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min	
T _{SMWCCK} /T _{SMCKKW}	RDWR_B setup/hold		10.0/0.0	10.0/0.0	10.0/0.0	ns, Min	
T _{SMCKCSO}	CSO_B clock to out (330 Ω pull-up resistor required)		7.0	7.0	7.0	ns, Max	
T _{SMCO}	D[31:00] clock to out in readback		8.0	8.0	8.0	ns, Max	
F _{RBCK}	Readback frequency	SLR-based	70	70	70	MHz, Max	
		All other devices	100	100	100	MHz, Max	
Boundary-Scan Port Timing Specifications							
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup/hold	SLR-based	9.0/2.0	9.0/2.0	9.0/2.0	ns, Min	
		All other devices	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min	
T _{TCKTDO}	TCK falling edge to TDO output	SLR-based	17	17	17	ns, Max	
		All other devices	7.0	7.0	7.0	ns, Max	
F _{TCK}	TCK frequency	SLR-based	20	20	20	MHz, Max	
		All other devices	66	66	66	MHz, Max	
BPI Master Flash Mode Programming Switching							
T _{BPICCO} ⁽²⁾	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out		8.5	8.5	8.5	ns, Max	
T _{BPIDCC} /T _{BPICCD}	D[15:00] setup/hold		4.0/0.0	4.0/0.0	4.0/0.0	ns, Min	
SPI Master Flash Mode Programming Switching							
T _{SPIDCC} /T _{SPICCD}	D[03:00] setup/hold		3.0/0.0	3.0/0.0	3.0/0.0	ns, Min	
T _{SPICCM}	MOSI clock to out		8.0	8.0	8.0	ns, Max	
T _{SPICFC}	FCS_B clock to out		8.0	8.0	8.0	ns, Max	

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* ([UG470](#)).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 84 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* ([UG470](#)).

Table 84: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

Date	Version	Description
08/03/2012	1.5	Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 12 and Note 13. Updated parameters in Table 3. Added Table 4 and Table 5. Updated the values for in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11. Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.2 speed specifications throughout the document with appropriate changes to Table 15 and Table 16 including production release of the XC7VX485T in the -2 and -1 speed designations. Added notes and specifications to Table 18. Updated the IOB Pad Input/Output/3-State discussion and changed Table 21 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 28. Rearranged Table 51 including moving some parameters to Table 1. Added Table 56. Updated Table 57. In Table 59, updated SJ Jitter Tolerance with Stressed Eye section, page 48 and Note 8. Added Note 1, Note 2, and Note 3 to Table 62. Added Note 1 and Note 2 to Table 63, and line rate ranges. Updated Table 64 including adding Note 1. Updated Table 65 including adding Note 1. In Table 82 updated Note 1 and added Note 4. In Table 83, updated T_{POR} and F_{EMCCK}.
09/20/2012	1.6	Removed the XC7V1500T device from data sheet. In Table 2, revised V_{CCINT} and V_{CCBRAM} and added Note 3. Updated some of the values in Table 7. Revised Table 15 and Table 16 to include production release of the XC7V585T in the -2 and -1 speed designations. Added values for the XC7V585T in Table 50. Updated Note 2 in Table 58.
09/26/2012	1.7	Revised Table 15 and Table 16 to include production release of the XC7VX485T in the -3 speed designation.
10/19/2012	1.8	Revised Table 15 and Table 16 to include production release of the XC7VX485T in the -2L (1.0V) speed designation. Removed -2L (0.9V) speed specifications from data sheet, this change includes edits to V_{CCINT} and V_{CCBRAM} in Table 2, editing Note 1 and removing Note 2 in Table 53. Also in Table 53, updated the F_{GTXM}, $F_{GTXRANGE1}$, and F_{GQPLL} specification for -1 speed grade from 6.6 Gb/s to 8.0 Gb/s. Edited Note 4 in Table 57 and Note 3 in Table 72.
12/12/2012	1.9	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.3 speed specifications throughout the document. Revised Table 15 and Table 16 to include production release of the XC7V585T in the -3 and -2L(1.0V) speed designations. Updated the notes in Table 50. Updated GTH Transceiver Specifications including removal of GTH Transceiver DC Characteristics section (use the XPE (download at http://www.xilinx.com/power). Updated Table 68 and added Table 71, Table 73, and Table 74. Removed Note 4 from Table 82.
12/24/2012	1.10	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.4 and Vivado 2012.4 speed specifications throughout the document. Revised the XC7V2000T in the -1 and -2 speed designations Table 15 to preliminary. Added the GTH Transceiver Protocol Jitter Characteristics section. Updated T_{TCKTDO} and added Internal Configuration Access Port section to Table 83.
01/31/2013	1.11	Added Note 2 to Table 2. Revised Table 15 and Table 16 to include production release of the XC7V2000T in the -1 and -2 speed specifications. Updated Note 1 in Table 35. Updated the notes in Table 37, Table 40 through Table 43, Table 46, and Table 47. In Table 66, updated D_{VPPIN}. In Table 67, updated V_{IDIFF}. Removed T_{LOCK} and T_{PHASE} from Table 70. Updated T_{DLOCK} in Table 71.
03/07/2013	1.12	Updated the AC Switching Characteristics section, based upon Table 14, for the ISE 14.5 and Vivado 2013.1 speed specifications throughout the document. Revised Table 15 and Table 16 to include production release of the XC7VX690T. Revised D_{VPPOUT} in Table 66. Updated values in Table 67 and Table 74. Removed Note 1 from Table 68. Updated $MMCM_F_{PFDMAX}$ in Table 38 and PLL_F_{PFDMAX} in Table 39. Added skew values to Table 50.